

The documentation and process conversion measures necessary to comply with this document shall be completed by 22 May 2020.

INCH-POUND

MIL-PRF-19500/701D
 21 January 2020
 SUPERSEDING
 MIL-PRF-19500/701C
 27 January 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD, EFFECT, N-CHANNEL, SILICON,
 RADIATION HARDENED (TOTAL DOSE AND SINGLE EVENT EFFECTS)
 TYPES 2N7491T2, 2N7492T2, AND 2N7493T2,
 QUALITY LEVELS JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-Channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. These transistors include ratings for avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Two levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. The device package outline is a TO-205AF package in accordance with [figure 1](#).

1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} (3) (4) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>
2N7491T2	25	0.71	5	30	30	±20	12	10	12	48	-55
2N7492T2	25	0.71	5	60	60	±20	12	9.5	12	48	to
2N7493T2	25	0.71	5	100	100	±20	11.7	7.4	11.7	46.8	+150

(1) Derate linearly 0.2 W/°C for $T_C > +25^\circ\text{C}$.

(2) See [figure 2](#), thermal impedance curves.

(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and device construction to 12 amps.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (r_{DS(on)}) \text{ at } T_{JM}}}$$

(4) See [figure 3](#), maximum drain current graphs.

(5) $I_{DM} = 4 \times I_{D1}$; I_{D1} as calculated by note (3).

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1.4 Primary electrical characteristics. Unless otherwise specified at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0 \text{ mA dc}$	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0 \text{ mA dc}$	Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80 \text{ percent}$ of rated V_{DS}	Max $r_{DS(on)} (1)$ $V_{GS} = 12 \text{ V}, I_D = I_{D2}$		E_{AS}	
				$T_J = +25^\circ\text{C}$	$T_J = +150^\circ\text{C}$		
	<u>V dc</u>	<u>V dc</u> Min Max		<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>	<u>mJ</u>
2N7491T2	30	2.0	4.0	10	0.045	0.100	520
2N7492T2	60	2.0	4.0	10	0.048	0.110	270
2N7493T2	100	2.0	4.0	10	0.080	0.184	173

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example, 6.5 for a list of available PINs, and 6.6 for cross-reference information.

1.5.1 JAN certification mark and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are "JANTXV" and "JANS".

1.5.2 RHA designator. The RHA levels that are applicable for this specification sheet from lowest to highest for quality levels JANS and JANKC are as follows: "R", "F", "G", and "H".

1.5.3 Device type. The designation system for the devices covered by this specification sheet is as follows.

1.5.3.1 First number and first letter symbols. The devices of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the devices covered by this specification sheet are as follows: "7491", "7492", and "7493".

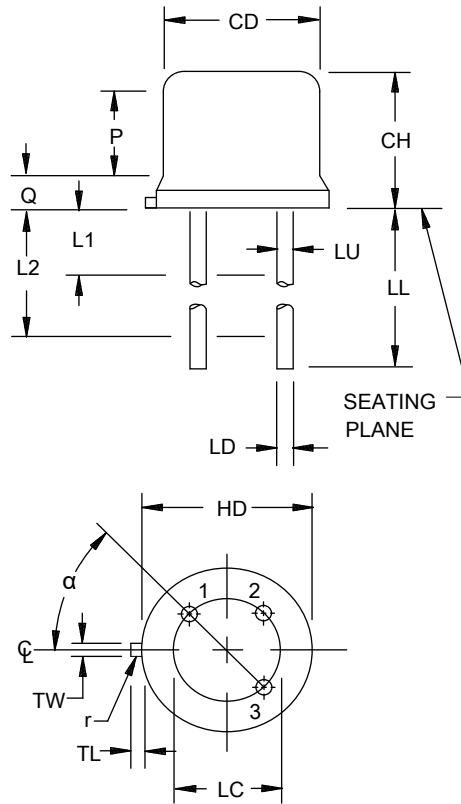
1.5.4 Suffix symbols. The suffix symbols "T2" are incorporated into the PINs for this specification sheet.

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.315	.355	8.00	9.02	4
CH	.160	.180	4.06	4.57	
HD	.340	.370	8.64	9.40	4
LC	.200 BSC		5.08 BSC		5
LD	.016	.021	0.41	0.53	6, 7
LL	.500	.750	12.70	19.05	6, 7, 8
LU	.016	.019	0.41	0.48	6, 7
L1		.050		1.27	6, 7
L2	.250		6.35		6, 7
P	.070		1.78		
Q		.050		1.27	4
TL	.029	.045	0.74	1.14	9
TW	.028	.034	0.71	0.86	10
r		.010		0.25	11
α	45° BSC		45° BSC		5



NOTES:

1. Dimension are in inches. Millimeters are given for general information only.
2. Terminal 1 = source, terminal 2 = gate, and terminal 3 is electrically connected to the case.
3. Terminal 4 is omitted from this outline.
4. Body contour optional within zone defined by dimensions CD, HD, and Q.
5. Leads at gauge plane $.054 +.001 - .000$ inch ($1.37 +0.03 -0.00$ mm) below seating plane shall be within $.007$ inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC. The device may be measured by direct methods.
6. Dimension LU applies between dimensions L1 and L2. Dimension LD applies between dimensions L2 and LL minimum. Diameter is uncontrolled in dimension L1 and beyond dimension LL minimum.
7. All three leads.
8. For "L" suffix devices, dimension LL = 1.5 inches (38.10 mm) minimum and 1.75 inches (44.45 mm) maximum.
9. Dimension TL measured from maximum HD.
10. Beyond r (radius) maximum, dimension TW shall be held for a minimum length of $.011$ inch (0.28 mm).
11. Dimension r (radius) applies to both inside corners of tab.
12. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-205AF.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows:

I_{AS}	Rated avalanche current, nonrepetitive
nC	nano Coulomb
SEE	Single Event Effects

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (TO-205AF).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#). At the option of the manufacturer, marking of the country of origin may be omitted from the body of the transistor but shall be retained on the initial container.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.9 RHA. The RHA requirements and test levels shall be as defined in [MIL-PRF-19500](#).

3.10 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I and II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 SEE. SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see [tables III and IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of [MIL-STD-750](#) that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point electrical measurements shall be in accordance with [table II](#). SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurement	
	JANS	JANTXV
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Single pulse avalanche energy test (see 4.3.2)	Single pulse avalanche energy test (see 4.3.2)
(3) 3c	thermal impedance (see 4.3.3)	thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein I_{DSS1} , I_{GSSF1} , I_{GSSR1} , as a minimum	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater.	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)1}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 10$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; Quality level JANTXV does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 24$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}). The test for single pulse avalanche energy shall be performed in accordance with method 3470 of [MIL-STD-750](#). The following details shall apply:

- a. Peak current, $I_{AS} = I_{D1}$.
- b. Inductance, $L = (2E_{AS}/(I_{D1})^2) * ((V_{BR} - V_{DD})/V_{BR})$ mH minimum.
- c. Gate to source resistor, R_{GS} : $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage, $V_{DD} = 25$ V dc, except $V_{DD} = 50$ V dc for 2N7493T2.
- e. Initial case temperature, $T_C = +25$ °C, -5 °C, $+10$ °C.
- f. Gate voltage, $V_{GS} = 12$ V dc.
- g. Number of pulses to be applied: 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , t_{MD} (and V_H where appropriate). See [table III](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and in table E-VIB (JANTXV) of [MIL-PRF-19500](#), and as follows.

4.4.2.1 Quality level JANS.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM (scanning electron microscope).
B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated; $T_A = +175$ °C, $t = 24$ hours minimum; or $T_A = +150$ °C, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated; $T_A = +175$ °C, $t = 120$ hours minimum; or $T_A = +150$ °C, $t = 240$ hours minimum.

4.4.2.2 Quality level JANTXV.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5		Not applicable.
B6		Not applicable.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; weight = 8 ounces (226 grams), 3 arcs of 90 degrees
C5	3161	See 4.3.3 .
C6	1042	Intermittent operation life, condition D, 6,000 cycles. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E- VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table III](#) herein.

4.4.5.1 SEE. Design capability shall be tested in accordance with table on the initial qualification and thereafter whenever a major die design or process change is introduced. See the design safe operation area figure.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3161	See 4.3.3	$Z_{\theta JC}$			$^{\circ}\text{C/W}$
Breakdown voltage drain to source	3407	Bias condition C, $V_{GS} = 0$, $I_D = 1 \text{ mA dc}$,	$V_{(BR)DSS}$			
2N7491T2				30		V dc
2N7492T2				60		V dc
2N7493T2				100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20 \text{ V dc}$, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -20 \text{ V dc}$, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS1}		10	$\mu\text{A dc}$
Static drain to source on-state resistance	3421	$V_{GS} = 12 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$			
2N7491T2					0.045	Ω
2N7492T2					0.048	Ω
2N7493T2					0.080	Ω
Forward voltage	4011	$V_{GS} = 0$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.5	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation						
$T_C = T_J = +125\text{ }^\circ\text{C}$						
Gate current	3411	$V_{GS} = \pm 20\text{V dc}$, bias condition C, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		25	$\mu\text{A dc}$
Static drain to source on-state resistance 2N7491T2 2N7492T2 2N7493T2	3421	$V_{GS} = 12\text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$		0.090 0.096 0.160	Ω Ω Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation						
$T_C = T_J = -55\text{ }^\circ\text{C}$						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, $I_D = 1\text{ mA dc}$	$V_{GS(TH)3}$		5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance 2N7491T2 2N7492T2 2N7493T2	3475	$I_D = I_{D2}$, $V_{DD} = 15\text{ V dc}$ (see 4.5.1)	g_{FS}	12 12 8.7		S S S
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 12\text{ V dc}$, $R_G = 7.5\ \Omega$, $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$		25	ns
Rise time			t_r		100	ns
Turn-off delay time			$t_{D(off)}$		35	ns
Fall time			t_f		30	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 4 , $t_p = 10$ ms minimum, $V_{DS} = 80$ percent of maximum rated V_{DS}				
Electrical measurements		See table I , subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B; $I_D = I_{D1}$, $V_{GS} = 12$ V dc, $V_{DD} = 50$ percent of rated V_{DS}				
On-state gate charge 2N7491T2 2N7492T2 2N7493T2			$Q_{G(ON)}$	65 40 50	nC nC nC	
Gate to source charge 2N7491T2 2N7492T2 2N7493T2			Q_{GS}	20 10 7.4	nC nC nC	
Gate to drain charge 2N7491T2 2N7492T2 2N7493T2			Q_{GD}	10 15 20	nC nC nC	
Reverse recovery time 2N7491T2 2N7492T2 2N7493T2	3473	$di/dt = -100$ A/ μ s, $V_{DD} \leq V_{(BR)DSS} \leq 50$ V, $I_D = I_{D1}$	t_{rr}	92 100 202	ns ns ns	

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ For end-point electrical measurements, this test is required for the following subgroups:

Group B, subgroups 2 and 3 (JANTXV).

Group B, subgroups 3 and 4 (JANS).

Group C, subgroup 6.

Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
	Method	Conditions		R, F, G, and H		R, F, and G		H 4/		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u>										
Not applicable										
<u>Subgroup 2</u>										
T _C = +25°C										
Steady-state total dose irradiation (V _{GS} bias) 5/	1019	V _{GS} = 12 V; V _{DS} = 0								
Steady-state total dose irradiation (V _{DS} bias) 5/	1019	V _{GS} = 0; V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)								
End-point electricals										
Breakdown voltage, drain to source 2N7491T2 2N7492T2 2N7493T2	3407	V _{GS} = 0; I _D = 1 mA; bias condition C	V _{(BR)DSS}							
				30		30		30		V dc
				60		60		60		V dc
				100		100		100		V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} ; I _D = 1 mA	V _{GS(th)1}	2.0	4.0	2.0	4.0	1.5	4.0	V dc
Gate current	3411	V _{GS} = +20 V; V _{DS} = 0, bias condition C	I _{GSSF1}		100		100		100	nA dc
Gate current	3411	V _{GS} = -20 V; V _{DS} = 0 bias condition C	I _{GSSR1}		-100		-100		-100	nA dc
Drain current	3413	V _{GS} = 0, V _{DS} = 80 percent of rated V _{DS} (pre-irradiation) bias condition C	I _{DSS}		10		10		25	µA dc
Static drain to source on-state voltage 2N7491T2 2N7492T2 2N7493T2	3405	V _{GS} = 12 V; I _D = I _{D2} condition A pulsed (see 4.5.1)	V _{DS(on)}							
					0.240		0.240		0.300	V dc
					0.323		0.323		0.408	V dc
					0.474		0.474		0.592	V dc
Forward voltage source drain diode	4011	V _{GS} = 0; I _D = I _{D1} bias condition C	V _{SD}		1.5		1.5		1.5	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ The H designation represents devices which pass end-point electricals at all 100K, 300K and 500K rads(Si).

5/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal	1071	Fine and gross leak.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2</u> ^{1/}			45 devices, c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours..	
Electrical measurements		See table I , subgroup 2 herein.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 4</u>			Sample size, N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 10</u>			22 devices, c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
<u>Subgroup 11</u>			3 devices
SEE ^{2/} ^{3/}	1080	See MIL-STD-750 method 1080.	

1/ A separate sample for each test shall be pulled.

2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

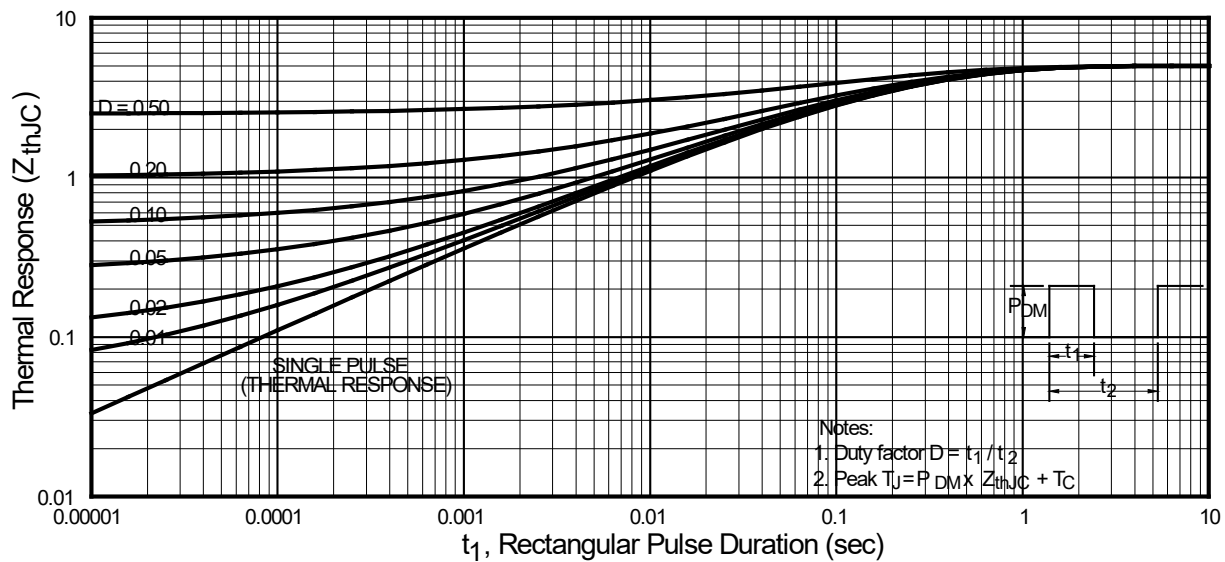


FIGURE 2. Thermal impedance curve.

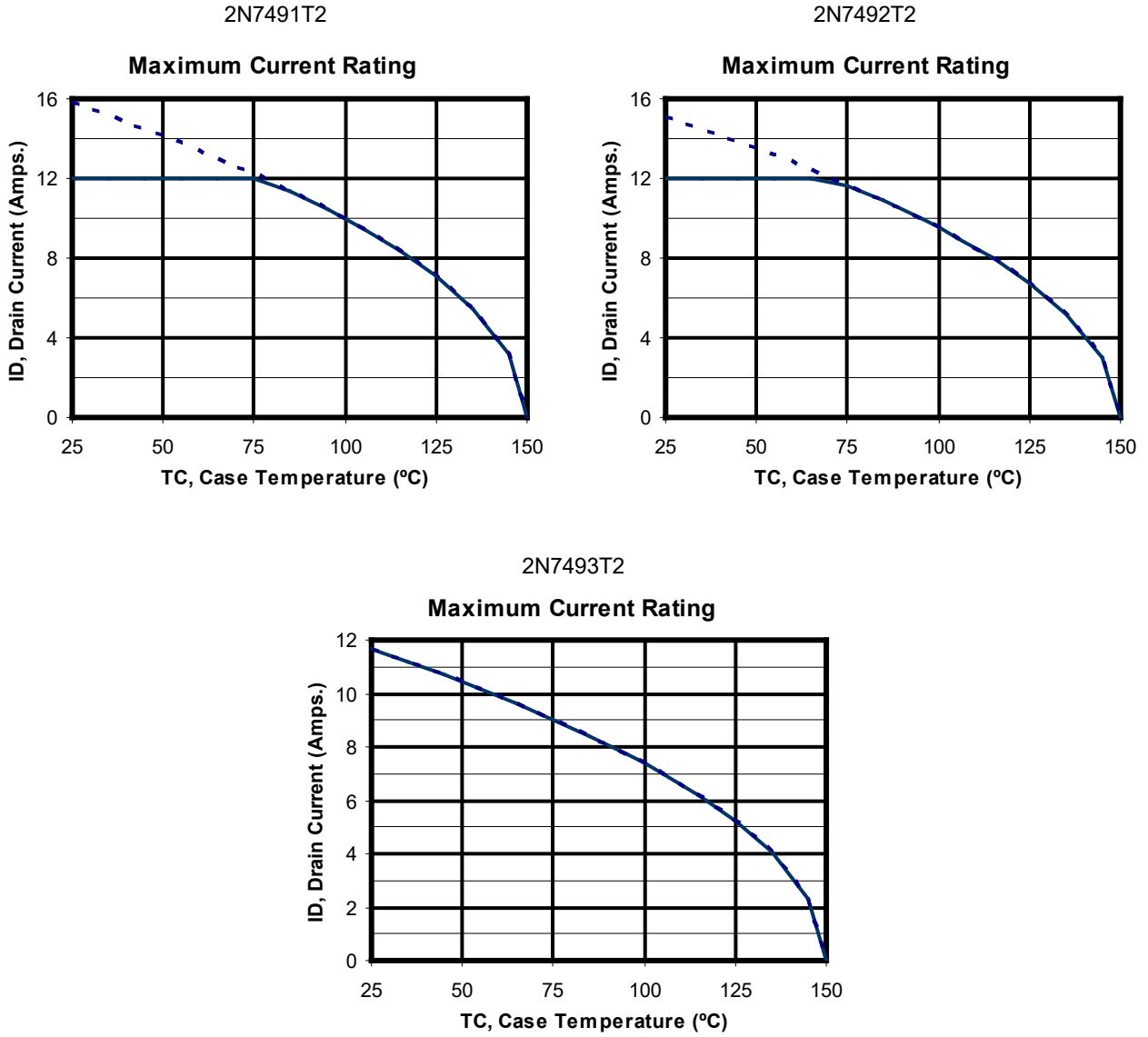
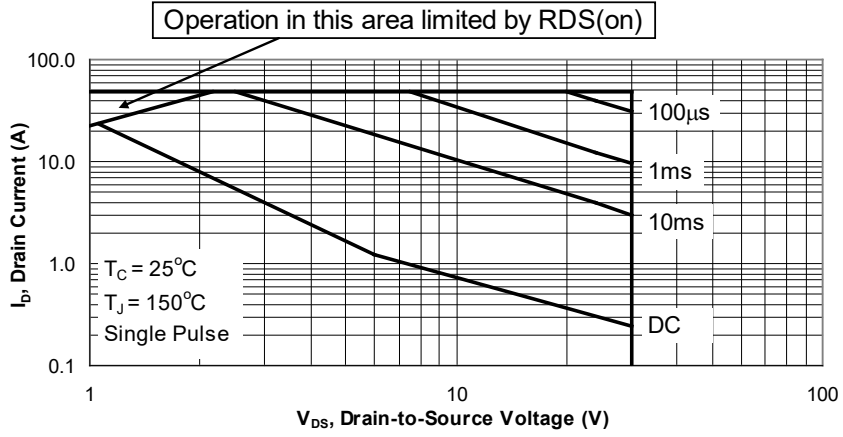


FIGURE 3. Maximum drain current versus case temperature graphs.

2N7491T2



2N7492T2

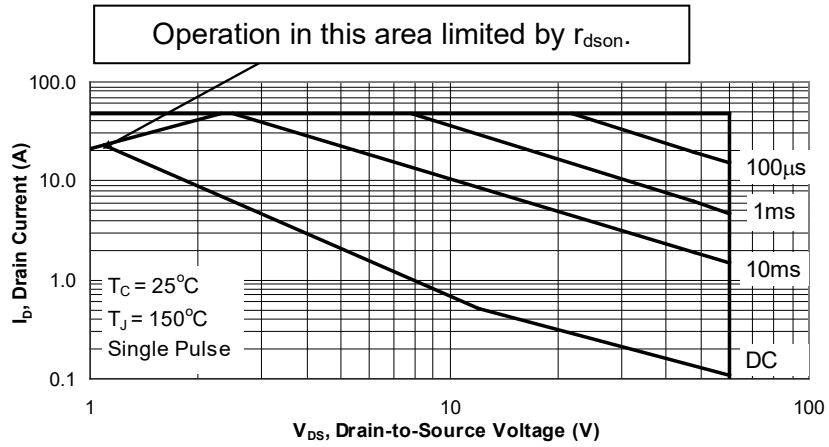


FIGURE 4. Safe operating area graphs.

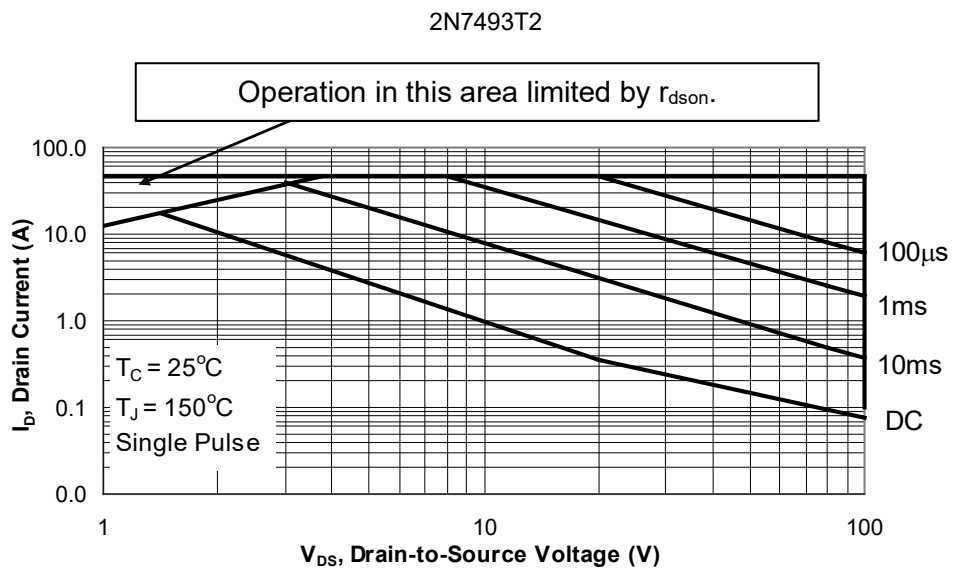


FIGURE 4. Safe operating area graphs - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

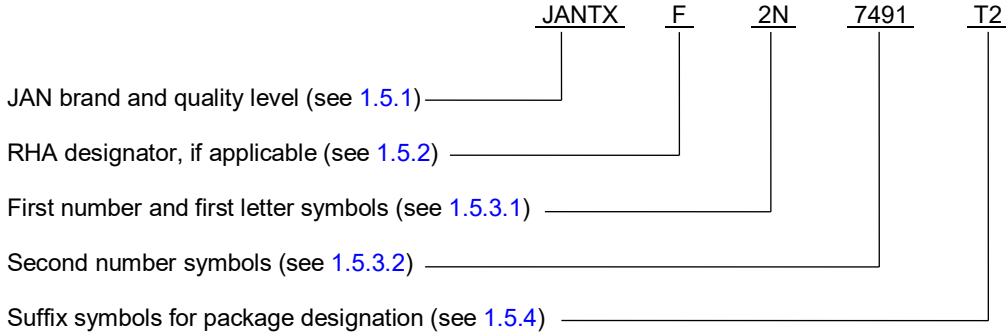
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see [3.4.1](#)).
- d. The complete PIN, see [1.5](#) and [6.4](#).
- e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.
- f. If SEE testing data is desired, it should be specified in the contract or order.
- g. If specific SEE characterization conditions are desired (see section [6.7](#) and [table IV](#)), manufacturer's cage code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "F" RHA level	PINs for devices of the "G" RHA level	PINs for devices of the "H" RHA level	PINs for devices of the "R" RHA level
JANTXVF2N7491T2	JANTXVG2N7491T2	JANTXVH2N7491T2	JANTXVR2N7491T2
JANTXVF2N7492T2	JANTXVG2N7492T2	JANTXVH2N7492T2	JANTXVR2N7492T2
JANTXVF2N7493T2	JANTXVG2N7493T2	JANTXVH2N7493T2	JANTXVR2N7493T2
JANSF2N7491T2	JANSG2N7491T2	JANSH2N7491T2	JANSR2N7491T2
JANSF2N7492T2	JANSG2N7492T2	JANSH2N7492T2	JANSR2N7492T2
JANSF2N7493T2	JANSG2N7493T2	JANSH2N7493T2	JANSR2N7493T2

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHF57Z30	2N7491T2
IRHF57034	2N7492T2
IRHF57130	2N7493T2

6.7 Application data.

6.7.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

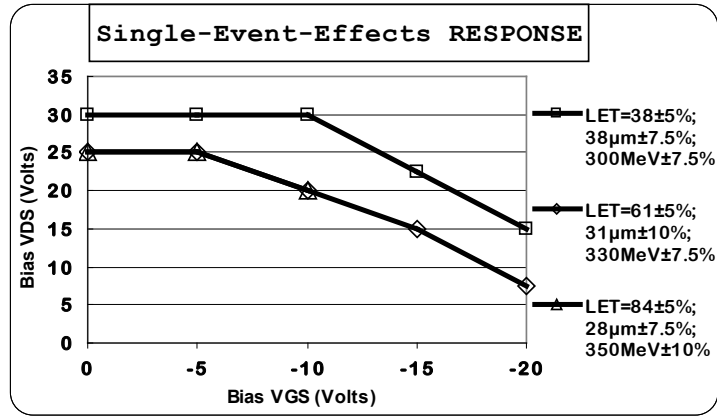
Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 5 .	3 devices
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I , subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $+25 \pm 5$ °C	
	2N7491T2		Surface LET = $38 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $38 \mu\text{m} \pm 7.5\%$, energy = $300 \text{ MeV} \pm 7.5\%$ In-situ bias conditions: $V_{DS} = 30 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 22.5 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 15 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7492T2		In situ bias conditions: $V_{DS} = 60 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 30 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7493T2		In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7491T2		Surface LET = $61 \text{ MeV-cm}^2/\text{mg} \pm 5\%$, range = $31 \mu\text{m} \pm 10\%$, energy = $330 \text{ MeV} \pm 7.5\%$ In-situ bias conditions: $V_{DS} = 25 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 20 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 15 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 7.5 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7492T2		In-situ bias conditions: $V_{DS} = 46 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 35 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 25 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 15 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	
2N7493T2	In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 35 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 25 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)			

See footnotes at end of table.

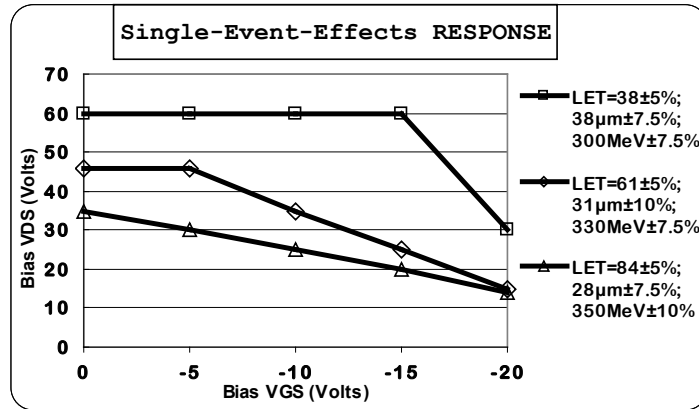
TABLE IV. Manufacturers characterization conditions - Continued.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
	2N7491T2		Surface LET = 84 MeV-cm ² /mg ±5%, range = 28 μm ±7.5%, energy = 350 MeV ±10% In-situ bias conditions: V _{DS} = 25 V and V _{GS} = -5 V V _{DS} = 20 V and V _{GS} = -10 V (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7492T2		In-situ bias conditions: V _{DS} = 35 V and V _{GS} = -5 V V _{DS} = 25 V and V _{GS} = -10 V V _{DS} = 20 V and V _{GS} = -15 V V _{DS} = 15 V and V _{GS} = -20 V (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7493T2		In-situ bias conditions: V _{DS} = 100 V and V _{GS} = -5 V V _{DS} = 80 V and V _{GS} = -10 V V _{DS} = 25 V and V _{GS} = -15 V (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Electrical measurements		I _{GSSF1} , I _{GSSR1} , and I _{DSS1} in accordance with table I , subgroup 2	
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> Upon qualification, all manufacturers should provide the verification test conditions to be added to this table. </div>				

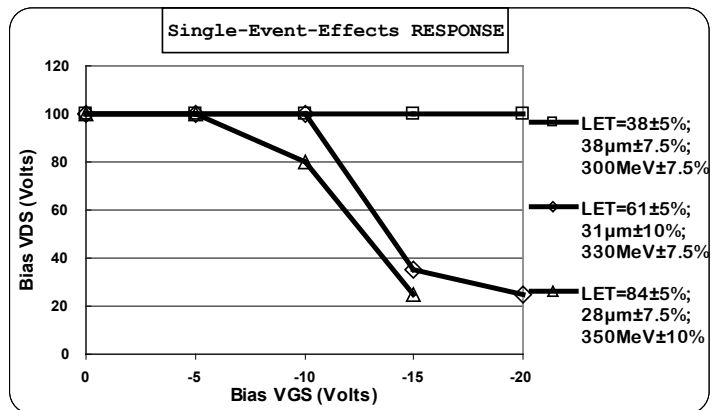
1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table I](#), subgroup 2, may be performed at the manufacturer's option.



2N7491T2



2N7492T2



2N7493T2

FIGURE 5. Cage 68210 typical SEE response graphs.

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

Custodians:

Army – CR
Navy – EC
Air Force – 85
NASA – NA
DLA – CC

Preparing activity:

DLA – CC

(Project 5961–2019–121)

Review activities:

Army – MI
Air Force – 19, 71

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.