

The documentation and process conversion measures necessary to comply with this revision shall be completed by 16 July April 2019.

INCH-POUND

MIL-PRF-19500/698G
w/AMENDMENT 2
16 April 2019
SUPERSEDING
MIL-PRF-19500/698G
w/AMENDMENT 1
21 September 2017

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED, N-CHANNEL, DEVICE TYPES 2N7470T1 AND 2N7471T1, JANTXVR, F, G, AND H AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}) for use in particular power-switching applications. See [6.7](#) for JANHC and JANKC die versions.

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with [figure 1](#) and a modified (tabless) TO-254AA in accordance with [figure 2](#) for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet [MIL-PRF-19500/741](#).

1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} (3) (4) $T_C = +100^\circ\text{C}$	I_S	I_{DM} (5)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C}/\text{W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>$^\circ\text{C}$</u>
2N7470T1, D4	208	3.0	0.6	60	60	± 20	45	45	45	180	-55 to
2N7471T1, D4				100	100		45	45	45	180	+150

- (1) Derate linearly 1.67 W/ $^\circ\text{C}$ for $T_C > +25^\circ\text{C}$.
- (2) See [figure 3](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and device construction to 45 A.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 4](#), maximum drain current graph.
- (5) $I_{DM} = 4 \times I_{D1}$; I_{D1} as calculated by footnote (3).

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1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0\text{mA dc}$	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0\text{ mA dc}$		Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS}	Max $r_{DS(on)} (1)$ $V_{GS} = 12\text{ V}, I_D = I_{D2}$		E_{AS}
					$T_J = +25^\circ\text{C}$	$T_J = +150^\circ\text{C}$	
	<u>V dc</u>	<u>V dc</u>		<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>	<u>mJ</u>
		Min	Max				
2N7470T1, D4	60	2.0	4.0	10	0.0076	0.016	824
2N7471T1, D4	100				0.014	0.028	493

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See 6.2 for unencapsulated devices.

1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANTXV and JANS quality levels are as follows: "R", "F", "G" and "H".

1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

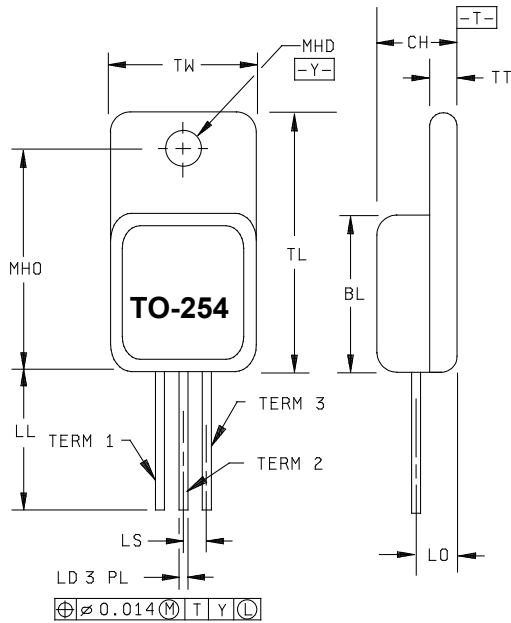
1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7470" and "7471".

1.5.4.3 Suffix letters. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of [figure 1](#). The suffix letters "D4" are used on devices that are packaged in the tabless TO-254AA package of [figure 2](#).

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

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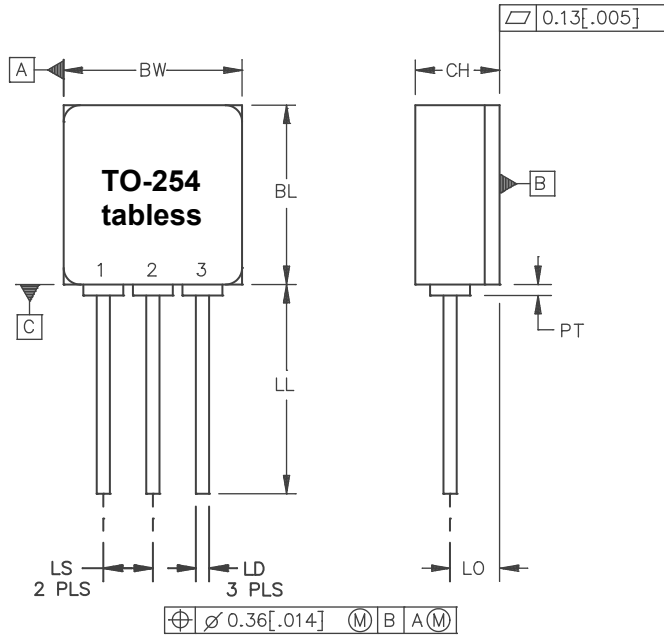
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions for TO-254AA (2N7470T1 and 2N7471T1).

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Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
BW	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.685	12.95	17.40	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
PT		.033		0.84	3
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness (PT) of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions for TO-254AA tabless package (2N7470D4 and 2N7471D4).

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2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

* [MIL-STD-750](#) - Test Methods for Semiconductor Devices.
[MIL-STD-883](#) - Test Method Standard Microcircuits

(Copies of these documents are available online at <https://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

I_{AS} - Rated avalanche current, nonrepetitive
nC - nano Coulomb

3.4 Interface and physical dimensions. The Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and [figure 1](#) (TO-254AA) and [figure 2](#) (tabless TO-254AA) herein. Methods used for electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with [MIL-STD-750](#), [MIL-PRF-19500](#) and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see [6.2](#)). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of [MIL-PRF-19500](#) and 100 percent dc testing in accordance with [table I](#), subgroup 2 herein.

* 3.4.2 Silicone die coat. The use of a silicone die coat requires a successful completion of [MIL-STD-883](#), [method 5011](#) on each silicone lot for its intended applications, and as part of the full [MIL-PRF-19500](#) qualification process.

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* 3.5 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.8 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see [table III](#) and [table IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of [MIL-STD-750](#) that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with [table II](#). SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

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* 4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (1) (2)	Measurement	
	JANS level	JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein, I _{GSSF1} , I _{GSSR1} , I _{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} Subgroup 2 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} Subgroup 2 of table I herein
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value ΔV _{GS(TH)1} = ±20 percent of initial value	Subgroup 2 of table I herein ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value ΔV _{GS(TH)1} = ±20 percent of initial value
17	Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.5), Endpoints: Subgroup 2 of table I herein.

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, V_{GS(th)1}, and r_{DS(ON)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

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4.3.1 Gate stress test. Apply $V_{GS} = 24$ V minimum for $t = 250$ μ S, minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current $I_{AS} = I_{D1}$.
- b. Inductance $L = \left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- c. Gate to source resistor R_{GS} $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage $V_{DD} = 25$ V dc, except $V_{DD} = 50$ V dc for 2N7471T1.
- e. Initial case temperature $T_C = +25^\circ$ C, -5° C, $+10^\circ$ C.
- f. Gate voltage $V_{GS} = 12$ V dc.
- g. Number of pulses to be applied 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{sw} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 30 - 60 μ s max. See table III, group E, subgroup 4 herein.

* 4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.3.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage 900 V dc.
- b. Duration of application of test voltage 15 seconds (min).
- c. Points of application of test voltage All leads to case (bunch connection).
- d. Method of connection Mechanical.
- e. Kilovolt-ampere rating of high voltage source 1,200V / 1.0 mA (min).
- f. Maximum leakage current 1.0 mA.
- g. Voltage ramp up time 500V /second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows.

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4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM (scanning electron microscope).
* B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 24$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$; $T_A = +175^\circ\text{C}$, $t = 120$ hours minimum; or $T_A = +150^\circ\text{C}$, $t = 240$ hours minimum.
B5	2037	Bond strength, test condition D.

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A; weight = 10 pounds; $t = 15$ s.
* C3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	See 4.3.3, $R_{\theta JC} = 0.60$ °C/W.
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4	3407	$V_{GS} = 0$, $I_D = 1$ mA dc, bias condition C	$V_{(BR)DSS}$	60 100		V dc V dc
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$, $I_D = 1$ mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -20$ V dc, bias condition C, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS} ,	I_{DSS1}		10	μA dc
Static drain to source on-state resistance 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.0076 0.014	Ω Ω
Forward voltage 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4	4011	$V_{GS} = 0$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.2 1.2	V dc V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation						
Gate current	3411	$T_C = T_J = +125^\circ\text{C}$ $V_{GS} = \pm 20 \text{ V dc}$, bias condition C, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0$, bias condition C, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		25	$\mu\text{A dc}$
Static drain to source on-state resistance 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4	3421	$V_{GS} = 12 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)2}$		0.011 0.023	Ω Ω
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)2}$	1.0		V dc
Low temperature operation						
Gate to source voltage (threshold)	3404	$V_{DS} \geq V_{GS(TH)3}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)3}$		5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4	3475	$I_D = I_{D2}$, $V_{DD} = 15 \text{ V dc}$ (see 4.5.1)	g_{FS}	42 42		S S
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = 12 \text{ V dc}$; $R_G = 2.35 \Omega$, $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			$t_{D(on)}$		35 35	ns ns
Rise time 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			t_r		125 125	ns ns
Turn-off delay time 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			$t_{D(off)}$		70 75	ns ns
Fall time 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			t_f		50 50	ns ns

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 5 $t_p = 10$ ms min. $V_{DS} = 80$ percent of max. rated V_{DS}				
Electrical measurements		See table 1 , subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B, $I_D = I_{D1}$, $V_{GS} = 12$ V dc $V_{DD} = 50$ percent of rated V_{DS}				
On-state gate charge 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			$Q_{G(ON)}$	150 160	nC nC	
Gate to source charge 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			Q_{GS}	75 55	nC nC	
Gate to drain charge 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4			Q_{GD}	50 65	nC nC	
Reverse recovery time 2N7470T1, 2N7470D4 2N7471T1, 2N7471D4	3473	Condition A, $di/dt = -100$ A/ μ s, $V_{DD} \leq 50$ V, $I_D = I_{D1}$	t_{rr}	170 270	ns ns	

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
	Method	Conditions		R, F, G and H		R, F and G		H <u>4/</u>		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u> Not applicable										
<u>Subgroup 2</u>		$T_C = + 25^\circ\text{C}$								
Steady-state total dose irradiation (V_{GS} bias) <u>5/</u>	1019	$V_{GS} = 12 \text{ V};$ $V_{DS} = 0$								
Steady-state total dose irradiation (V_{DS} bias) <u>5/</u>	1019	$V_{GS} = 0; V_{DS} = 80$ percent of rated V_{DS} (preirradiation)								
End-point electricals:										
Breakdown voltage, drain to source 2N7470T1, D4 2N7471T1, D4	3407	$V_{GS} = 0;$ $I_D = 1 \text{ mA};$ bias condition C	$V_{(BR)DSS}$	60 100		60 100		60 100		V dc V dc
Gate to source voltage (threshold) 2N7470T1, D4 2N7471T1, D4	3404	$V_{DS} \geq V_{GS}$ $I_D = 1 \text{ mA}$	$V_{GS(th)1}$	2.0 2.0	4.0 4.0	2.0 2.0	4.0 4.0	1.5 1.5	4.0 4.0	V dc V dc
Gate current	3411	$V_{GS} = +20 \text{ V dc};$ $V_{DS} = 0;$ bias condition C	I_{GSSF1}		100		100		100	nA dc
Gate current	3411	$V_{GS} = -20 \text{ V dc}$ $V_{DS} = 0;$ bias condition C	I_{GSSR1}		-100		-100		-100	nA dc

See footnotes at end of table.

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TABLE II. Group D inspection - Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
	Method	Conditions		R, F, G and H		R, F and G		H <u>4/</u>		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 2</u> - Continued										
Drain current	3413	$V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS} (pre- irradiation); bias condition C	I_{DSS}		10		10		25	μA dc
Static drain to source on-state voltage 2N7470T1, D4 2N7471T1, D4	3405	$V_{GS} = 12 V$; $I_D = I_{D2}$ condition A, pulsed (see 4.5.1)	$V_{DS(on)}$		0.275 0.585		0.275 0.585		0.320 0.630	V dc V dc
Forward voltage source drain diode 2N7470T1, D4 2N7471T1, D4	4011	$V_{GS} = 0$; $I_D = I_{D2}$; bias condition A	V_{SD}		1.2 1.2		1.2 1.2		1.2 1.2	V dc V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheets utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ The "H" designation represents devices which pass end-points at R, F, G, and H designated total-ionizing-dose (TID).

5/ Separate samples shall be pulled for each bias.

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TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			
Temperature cycling	1051	Test condition G, 500 cycles.	45 devices c = 0
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2 1/</u>			
Steady-state gate bias	1042	Test condition B; 1,000 hours.	45 devices c = 0
Electrical measurements		See table I , subgroup 2.	
Steady state reverse bias	1042	Test condition A; 1,000 hours.	
Electrical measurements		See table I , subgroup 2.	Sample size N/A
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10</u>			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	22 devices, c = 0
<u>Subgroup 11</u>			
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2 .	3 devices

1/ A separate sample may be pulled for each test condition.

2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

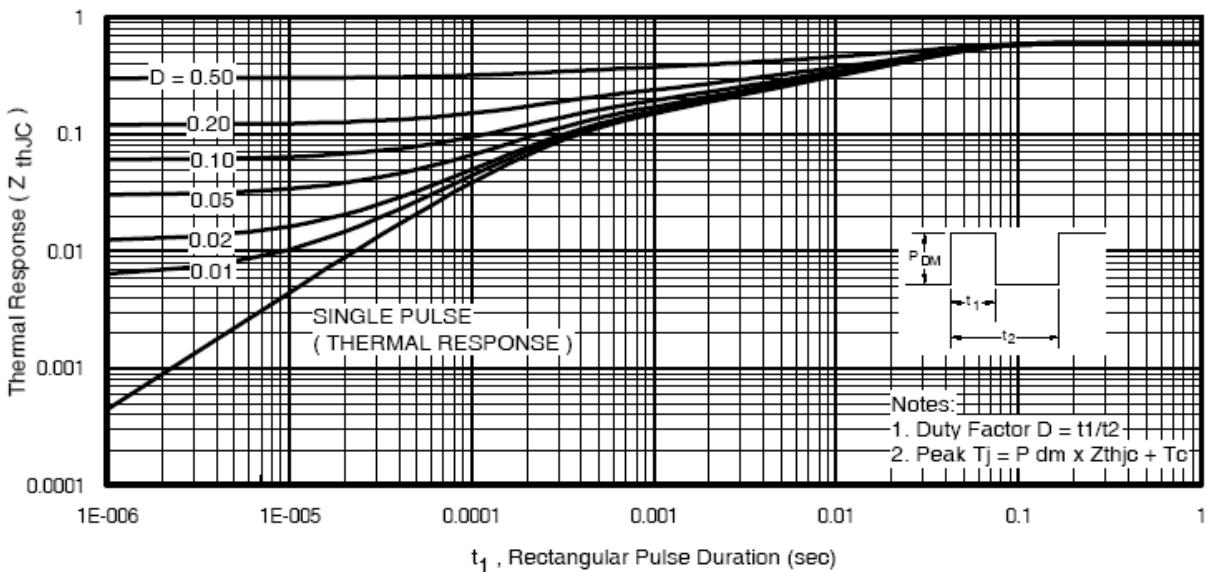
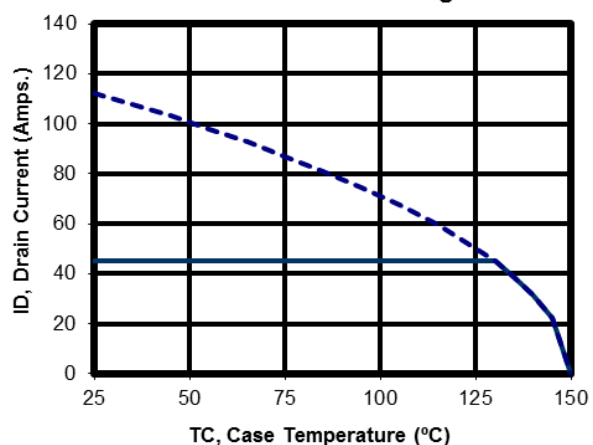


FIGURE 3. Thermal impedance curves.

2N7470T1, 2N7470D4
Maximum Current Rating



2N7471T1, 2N7471D4
Maximum Current Rating

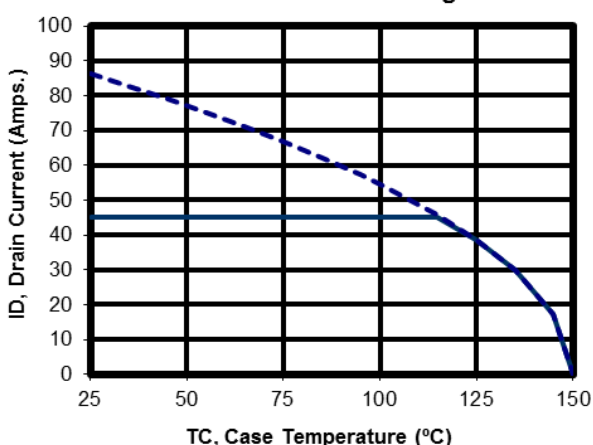
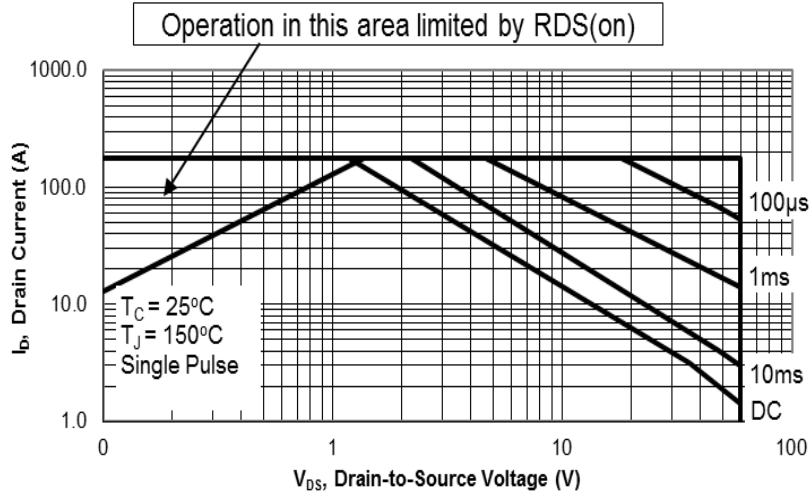
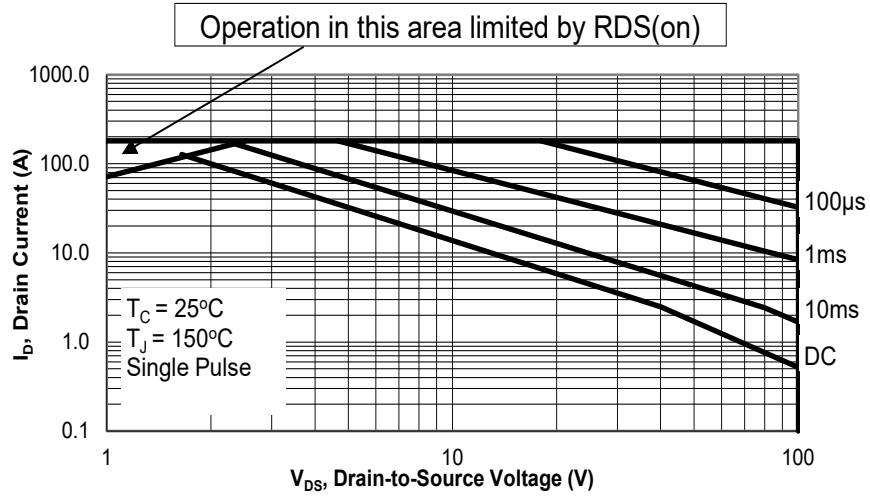


FIGURE 4. Maximum drain current versus case temperature graphs.



2N7470T1, 2N7470D4



2N7471T1, 2N7471D4

FIGURE 5. Safe operating area graphs.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

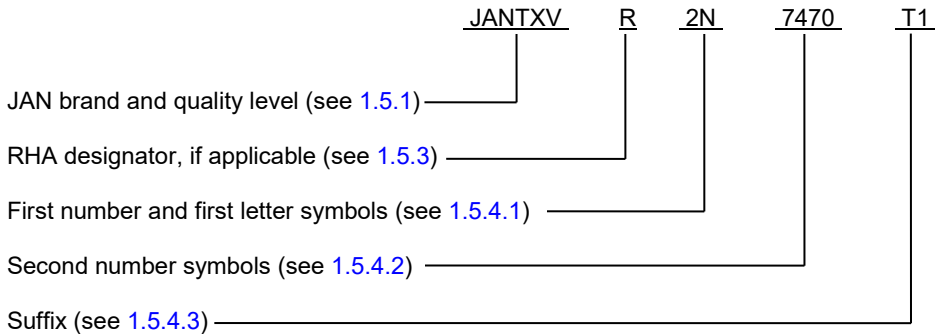
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead formation and finish (see 3.4.1).
- d. The complete PIN, see 1.5 and 6.5.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

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6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7470T1	JANTXV#2N7470T1	JANS2N7470T1	JANS#2N7470T1
JANTXV2N7470D4	JANTXV#2N7470D4	JANS2N7470D4	JANS#2N7470D4
JANTXV2N7471T1	JANTXV#2N7471T1	JANS2N7471T1	JANS#2N7471T1
JANTXV2N7471D4	JANTXV#2N7471D4	JANS2N7471D4	JANS#2N7471D4

(1) The number sign (#) represent one of four RHA designators available on this specification sheet ("R", "F", "G" or "H").

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHMS57064	2N7470T1
IRHMS57160	2N7471T1

6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

6.8 Application data.

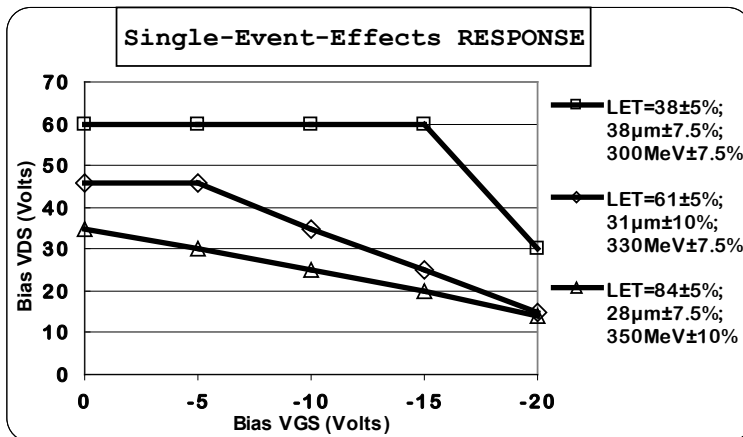
6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

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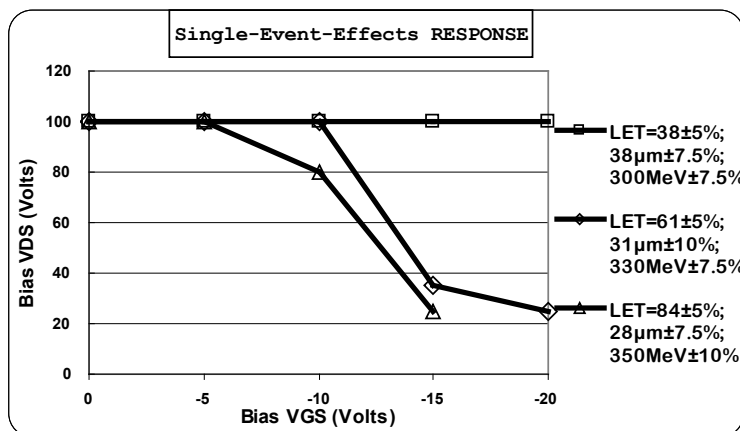
TABLE IV. Manufacturers characterization conditions.

Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of February 2009 and older)	SEE <u>1/</u>	1080	See figure 6 . IGSSF1, IGSSR1, and IDSS1 in accordance with table 1 , subgroup 2 Fluence = $3E5 \pm 20$ percent ions/cm ² , flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = 25 ± 5 °C Surface LET = 38 MeV-cm ² /mg $\pm 5\%$, range = 38 μ m $\pm 7.5\%$, energy = 300 MeV $\pm 7.5\%$	3 devices
	2N7470T1, D4		In-situ bias conditions: $V_{DS} = 60$ V and $V_{GS} = -15$ V $V_{DS} = 30$ V and $V_{GS} = -20$ V (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7471T1, D4		In-situ bias conditions: $V_{DS} = 100$ V and $V_{GS} = -20$ V (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 61 MeV-cm ² /mg $\pm 5\%$, range = 31 μ m $\pm 10\%$, energy = 330 MeV $\pm 7.5\%$	
	2N7470T1, D4		In-situ bias conditions: $V_{DS} = 46$ V and $V_{GS} = -5$ V $V_{DS} = 30$ V and $V_{GS} = -10$ V $V_{DS} = 25$ V and $V_{GS} = -15$ V $V_{DS} = 15$ V and $V_{GS} = -20$ V (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7471T1, D4		In-situ bias conditions: $V_{DS} = 100$ V and $V_{GS} = -10$ V $V_{DS} = 35$ V and $V_{GS} = -15$ V $V_{DS} = 25$ V and $V_{GS} = -20$ V (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = 84 MeV-cm ² /mg $\pm 5\%$, range = 28 μ m $\pm 7.5\%$, energy = 350 MeV $\pm 7.5\%$	
	2N7470T1, D4		In-situ bias conditions: $V_{DS} = 35$ V and $V_{GS} = 0$ V $V_{DS} = 30$ V and $V_{GS} = -5$ V $V_{DS} = 25$ V and $V_{GS} = -10$ V $V_{DS} = 20$ V and $V_{GS} = -15$ V $V_{DS} = 14$ V and $V_{GS} = -20$ V (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7471T1, D4		In-situ bias conditions: $V_{DS} = 100$ V and $V_{GS} = -5$ V $V_{DS} = 80$ V and $V_{GS} = -10$ V $V_{DS} = 25$ V and $V_{GS} = -15$ V (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Electrical Measurements <u>2/</u>			
Upon qualification, all manufacturers shall provide the verification test conditions to be added to this table.				

1/ IGSSF1, IGSSR1, and IDSS1 was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table 1](#), subgroup 2, may be performed at the manufacturer's option.



2N7470T1, 2N7470D4



2N7471T1, 2N7471D4

FIGURE 6. SEE safe operating area graph.

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6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-6939 or DSN 850-6939.

6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC
(Project 5961-2019-041)

* Review activity:
Army - MI
Air Force - 71, 19

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