

The documentation and process conversion measures necessary to comply with this revision shall be completed by 18 August 2011

INCH-POUND

MIL-PRF-19500/690A
18 May 2011
SUPERSEDING
MIL-PRF-19500/690
7 November 2003

* PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, DIODE, SILICON, SWITCHING
TYPES 1N4148SCSP (NBN), JANHC AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for silicon, diffused, switching diodes, mounted with silicon-on-insulator technology as a very small sealed chip scale package (SCSP). They are available as single down-mounted device, or available in multiple arrays as designated by the NBN suffix. Two levels of product assurance are provided for the device type as specified in MIL-PRF-19500.

* 1.2 Physical dimensions. See [figure 1](#) and [figure 2](#).

* 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Type	$V(\text{BR})$	V_{RWM}	I_{O} $T_A = 25^\circ\text{C}$	I_{FSM} $t_p = 1/120 \text{ s}$	T_{STG}	T_{J}	$Z_{\theta\text{JX}}$	$R_{\theta\text{JMP}}$
1N4148SCSP	$\frac{V \text{ dc}}{100}$	$\frac{V \text{ (pk)}}{75}$	$\frac{\text{mA}}{200}$ (1)	$\frac{A \text{ (pk)}}{2}$	$^\circ\text{C}$ -55 to +175	$^\circ\text{C}$ -55 to +175	$\frac{^\circ\text{C/W}}{20}$	$\frac{^\circ\text{C/W}}{80}$ (2)

(1) Derate at 1.6 mA/°C above $T_A = 25^\circ\text{C}$.

(2) Maximum value shown is for solder mounting thickness of 1.5 mill-inches on infinite heat sink.

* 1.4 Primary electrical characteristics at $T_A = +25^\circ\text{C}$, unless otherwise indicated.

Type (1)	V_{F1}		V_{F2}		I_{R1} at $V_{\text{R}} = 20 \text{ V dc}$	I_{R2} at $V_{\text{R}} = 75 \text{ V dc}$
1N4148SCSP	$\frac{I_{\text{F}} \text{ (mA dc)}}{10}$	$\frac{V \text{ dc}}{0.8}$	$\frac{I_{\text{F}} \text{ (mA dc)}}{100}$	$\frac{V \text{ dc}}{1.2}$	$\frac{\text{nA dc}}{25}$	$\frac{\mu\text{A dc}}{0.5}$

Type	I_{R3} at $V_{\text{R}} = 20 \text{ V dc}$ $T_A = 150^\circ\text{C}$	I_{R4} at $V_{\text{R}} = 75 \text{ V dc}$ $T_A = 150^\circ\text{C}$	t_{fr} at $V_{\text{fr}} = 5.0 \text{ V dc (pk)}$ and $I_{\text{F}} = 50 \text{ mA dc}$	t_{rr}
1N4148SCSP	$\frac{\mu\text{A dc}}{35}$	$\frac{\mu\text{A dc}}{75}$	$\frac{\text{ns}}{20}$	$\frac{\text{ns}}{5}$

(1) See [figures 1](#) and [2](#).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.daps.dla.mil/>.

- * 1.4 Primary electrical characteristics at $T_A = +25^\circ\text{C}$, unless otherwise indicated - Continued.

Type	V_{F1} (Max) at $I_F = 10 \text{ mA dc}$	V_{F2} (Max) at $I_F = 100 \text{ mA dc}$	I_{R1} (Max) at $V_R = 20 \text{ V dc}$	I_{R2} (Max) at $V_R = 75 \text{ V dc}$
1N4148SCSP	<u>V dc</u> 0.8	<u>V dc</u> 1.2	<u>nA dc</u> 25	<u>$\mu\text{A dc}$</u> 0.5

Type	I_{R3} (Max) at $V_R = 20 \text{ V dc}$ $T_A = +150^\circ\text{C}$	I_{R4} (Max) at $V_R = 75 \text{ V dc}$ $T_A = +150^\circ\text{C}$	t_{fr} (Max) at $V_{fr} = 5.0 \text{ V dc (pk)}$ and $I_F = 50 \text{ mA dc}$	t_{rr} (Max)
1N4148SCSP	<u>$\mu\text{A dc}$</u> 35	<u>$\mu\text{A dc}$</u> 75	<u>ns</u> 20	<u>ns</u> 5

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

- * 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

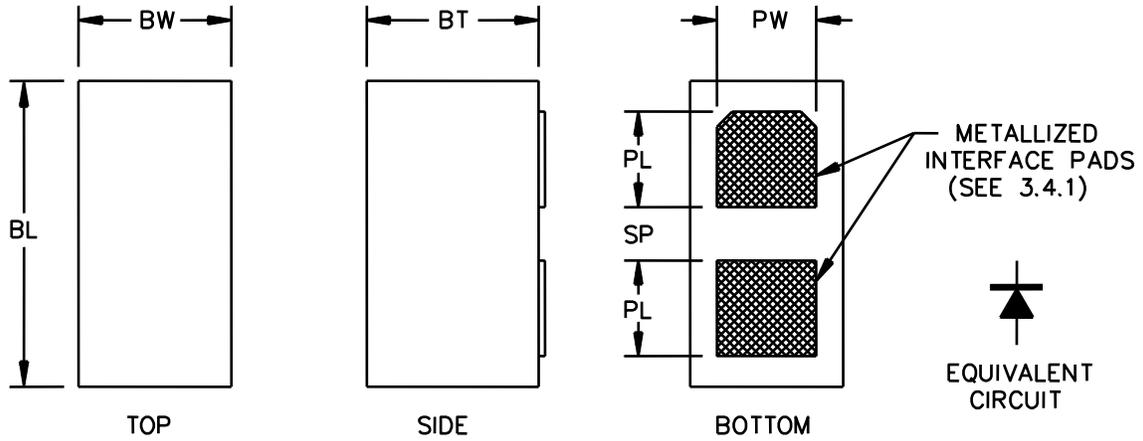
MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch/> or <https://assist.daps.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

- * 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



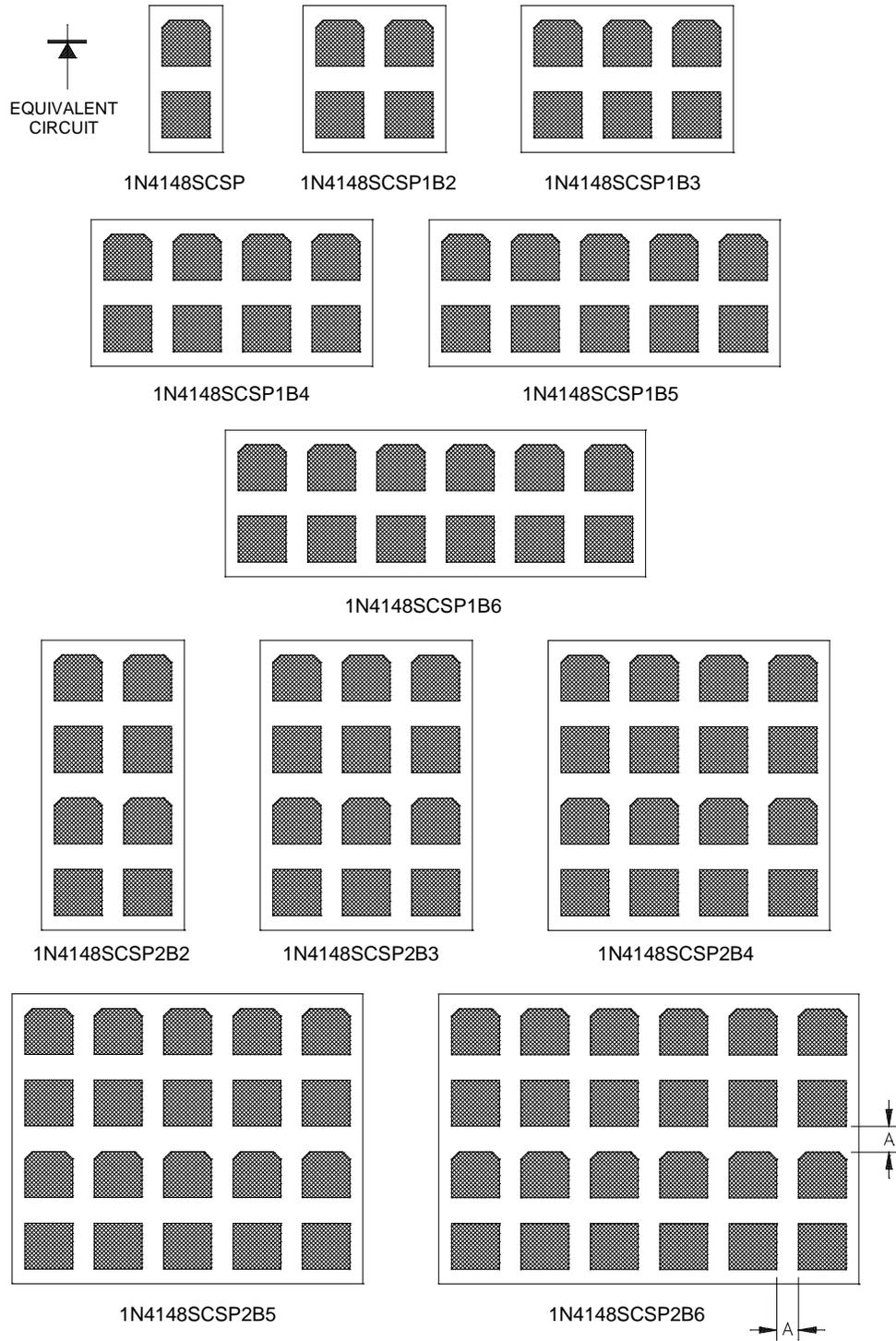
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	0.039	0.042	0.99	1.07	
BT	0.018	0.023	0.44	0.59	
BW	0.019	0.022	0.48	0.56	
PL	0.0125	0.0145	0.32	0.37	
PW	0.013	0.015	0.33	0.38	
SP	0.0055	0.0075	0.14	0.19	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.

* FIGURE 1. Semiconductor device, diode, type 1N4148SCSP.

MIL-PRF-19500/690A



Note: See figure 1 for individual dimensions. A is .00075 - .0105 inch (0.019 – 0.027 mm)

* FIGURE 2. Description of NBN array designations.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

* 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

CSP	Chip scale package.
PIN	Part Identification Number.
$R_{\theta JMP}$	Thermal resistance, junction to mounting pad.
V_{fr}	Forward recovery voltage. Specified maximum forward voltage used to determine forward recovery time.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on [figures 1](#) and [2](#) herein.

3.4.1 Interface metallization. Interface metallization shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of interface metallization is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.2 Diode construction. Devices shall be constructed using a silicon on insulator technique with both the cathode and anode attachments on one side of the device. The opposite (top) side of the device shall be a Pyrex layer (insulator) that serves as a mechanical carrier for the silicon device. The silicon and Pyrex both have a TCE (thermal coefficient of expansion) of 3.0-3.5 ppm/°C for overall mounting considerations. This construction becomes a sealed chip scale package with flip-chip features. They are also qualified and screened in a similar manner as chips due to their very small size, including conformance inspections as described in appendix G of MIL-PRF-19500 except for wire bonding features that are not applicable. See [tables I](#) and [II](#) for further details.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, [1.4](#), and [table I](#) herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in [tables I](#) and [II](#) herein.

* 3.7 Polarity. The polarity shall be indicated by an arrow pointing toward the cathode end on the top-side view.

3.8 Marking. Devices shall not have a part number marked on them. Devices shall be marked with polarity as described in 3.7. Initial container package marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

* 4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- * c. Conformance inspection (see [4.4](#) and [tables I](#) and [II](#) herein).

* 4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

MIL-PRF-19500/690A

* 4.2.1 Group E qualification. Group E qualification shall be performed for qualification or requalification beyond that described by appendix G of MIL-PRF-19500 only in accordance with the instructions of the qualifying agency for these JANHC and JANKC chip packages. In case qualification was awarded to a prior revision of the associated specification that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein shall be performed on the first inspection lot to this revision to maintain qualification.

* 4.2.2 JANHC and JANKC sealed chip scale packages. Qualifications shall be in accordance with Appendix G of MIL-PRF-19500 and as specified herein.

* 4.3 Screening. See [table II](#), Subgroups 1 and 2 herein.

* 4.4 Conformance inspection. Conformance inspection to JANHC or JANKC shall be in accordance with [table II](#) as specified herein. Conformance inspection shall be performed on PIN 1N4148SCSP to qualify all variations. The conformance inspection samples may be mounted to appropriate substrates or carriers in order to facilitate testing.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and [table I](#) herein as it applies to [tables II](#) and [III](#) herein.

* 4.4.2 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table IX of MIL-PRF-19500 and as specified herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Forward recovery voltage and time. Forward recovery time shall be measured as the time interval between zero time and the point where the pulse has decreased to 110 percent of the steady-state value of V_F when $I_F = 50$ mA dc. The maximum rise time of the response detector shall be 1 ns.

* 4.5.3 Thermal resistance. Thermal resistance measurement shall be in accordance with method 4081 of MIL-STD-750. Forced moving air or draft shall not be permitted across the device during test. The maximum limit for $R_{\theta JMP}$ under these test conditions with 1.5 mill-inches of solder thickness on an infinite heat sink, shall be $R_{\theta JMP} \leq 80^\circ\text{C/W}$. The following conditions shall apply when using method 4081.

- a. I_H 75 mA to 300 mA.
- b. t_H 25 seconds minimum
- c. I_M 1 mA to 10 mA.
- d. t_{MD} 70 μs maximum.

MIL-PRF-19500/690A

* TABLE I. Group A inspection.

Inspection 1/ Method	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual inspection	2071	See 4.3 and table II , subgroup 2				
<u>Subgroup 2</u>						
Forward voltage	4011	$I_F = 10 \text{ mA dc}$	V_{F1}		0.8	V dc
Breakdown voltage	4021	$I_R = 100 \text{ } \mu\text{A dc}$	V_{BR1}	100		V dc
Reverse current	4016	DC method, $V_R = 20 \text{ V dc}$	I_{R1}		25	nA dc
Reverse current	4016	DC method, $V_R = 75 \text{ V dc}$	I_{R2}		500	nA dc
Forward voltage	4011	$I_F = 100 \text{ mA dc}$	V_{F2}		1.2	V dc
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
Reverse current	4016	DC method, $V_R = 20 \text{ V dc}$	I_{R3}		35	$\mu\text{A dc}$
Reverse current	4016	DC method, $V_R = 75 \text{ V dc}$	I_{R4}		75	$\mu\text{A dc}$
Forward voltage	4011	$I_F = 10 \text{ mA dc}$	V_{F3}		0.8	V dc
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward voltage	4011	$I_F = 100 \text{ mA dc}$	V_{F4}		1.3	V dc
<u>Subgroup 4</u>						
Junction capacitance	4001	$V_R = 0 \text{ V dc}$, $f = 1 \text{ MHz}$, $V_{\text{sig}} = 50 \text{ mV}_{\text{p-p}}$ maximum	C_1		4.0	pF
Junction capacitance	4001	$V_R = 1.5 \text{ V dc}$, $f = 1 \text{ MHz}$, $V_{\text{sig}} = 50 \text{ mV}_{\text{p-p}}$ maximum	C_2		2.8	pF
Reverse recovery time	4031	Condition A, $C \geq 1 \text{ nF}$, $I_F = I_R = 10 \text{ mA dc}$, $R_L = 100 \text{ } \Omega \pm 5\%$ $I_{R(\text{REC})} = 1.0 \text{ mA dc}$, $R \geq 1,000 \text{ } \Omega$.	t_{rr}		5	ns

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> Not applicable						
<u>Subgroup 6</u> Surge current	4066	Condition A (sine wave) if(surge) = 2 A (pk), I _O = maximum rated dc current = 0 V _{RM} = 0 Ten surges, 8.3 ms width each, one surge per minute, T _A = +25°C				
Electrical measurements		See table I , subgroup 2				
<u>Subgroup 7</u> Forward recovery voltage and time	4026	I _F = 50 mA dc, (see 4.5.2)	V(PEAK) t _{fr}	5.0 20	V (pk) ns	

1/ For sampling plan, see MIL-PRF-19500.

MIL-PRF-19500/690A

* TABLE II. SCSP evaluation requirements. 1/

Subgroup	Class		Test	MIL-STD-750		Quantity (accept no.)		Reference notes	
	K	H		Method	Condition	Class			
						K	H		
1	X	X	Electrical test		Group A, Subgroup 2	100%			
2	X	X	Visual inspection		See 6.2.1	100%			
3A	X	X	Internal/die Visual inspection		Random sample	45 (0)	22 (0)		
3B	X	X	Sample assembly			45 pieces min	22 pieces min	2	
4	X	X	* High temp life Non-operating life (stabilization bake)	1032	+175°C, 340 hours	45 (0)	22 (0)		
	X	X	Temperature cycling	1051	Condition C				
	X		Mechanical shock or Constant acceleration	2016	Y1 axis direction				
				2006	Y1 axis direction				
	X	X	Electrical test (read/record)		Group A, subgroups 2, 3, 4				3
	X	X	HTRB	1038	Condition A				
	X	X	Electrical test (read/record)		Group A, Subgroup 2				3 4
	X	X	Burn-in						5
	X	X	Electrical test (read/record)		Group A, subgroups 2, 3				3 4
	X		Steady-state life	1038	Condition B				6
	X		Electrical test (read and record)		Group A, Subgroups 2, 3, 4				3
5A			Solderability evaluation	2026	"Test B" for surface mount			22 (0)	
5B			Die shear evaluation	2017		5 (0) or 10 (1)		7	
6	X		SEM	2077	As applicable	See test method 2077			
7			RHA not required						
8			Surge	4066	Group A, subgroup 6	45 (0)	22 (0)		
9			Forward Recovery	4026	Group A, subgroup 7				

See footnotes on next page.

TABLE II. SCSP evaluation requirements - Continued. 1/

- 1/ NOTE: This table is similar to appendix G of MIL-PRF-19500 for die element evaluation requirements; however, this also includes further additions (with an asterisk) for this CSP. Wire bond is not applicable to this CSP with flip-chip mounting.
- 2/ Test samples shall be assembled in suitable packages using standard assembly procedures. The packaged sample shall be marked or labeled to identify:
 - a. Serial numbers, if required;
 - b. Device PIN and
 - c. Inspection lot number or date code.
- 3/ Thermal impedance shall not apply.
- 4/ For JANHC only, if one device fails during any of the subgroup 4 tests following electrical tests (table E-V of MIL-PRF-19500, group A, subgroups 2, 3, or 4), then 16 additional devices may be added to the element evaluation with no additional failures allowed, 38 devices, $c = 1$.
- 5/ Power burn-in conditions are as follows: Method 1038 of MIL-STD-750, condition B. $I_F = 200$ mA dc minimum; or $V_R =$ rated V_{RWM} , $f = 50$ to 60 Hz, $I_O = 200$ mA. $T_A = +75^\circ\text{C}$ maximum.
- 6/ Time and temperature requirements in accordance with table G-I of MIL-PRF-19500.
- 7/ Die shear test shall be performed in accordance with test method 2017 of MIL-STD-750. If only one die fails, another sample may be selected and subjected to subgroup 3B evaluation. If the second sample contains no failures, the die shear test results are accepted and the lot is acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot shall be rejected.

MIL-PRF-19500/690A

* TABLE III. Group E inspection (all quality levels) for qualification or requalification only.

Inspection	MIL-STD-750		Sample plan * Class H and K
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	-55 to +175°C, 500 cycles, condition C	
Electrical measurements		See table I , subgroup 2	
Moisture resistance	1021	10 cycles	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent operating life	1037	10,000 cycles	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 3</u>			3 devices c = 0
DPA		In accordance with suppliers procedure	
<u>Subgroup 4</u>			6 devices c = 0
Thermal resistance	4081	See 4.5.3 herein	
<u>Subgroup 6</u>			11 devices c = 0
ESD	1020		

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

* (This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

* c. Interface metallization (see 3.4.1).

d. Product assurance level and type designator.

e. Type designation including array suffix (see figure 2 herein) and product assurance level.

f. Special array configurations and dimensions other than specified on figures 1 and 2, with approval of the manufacturer, will be identified in the contract.

* 6.2.1 Visual inspection criteria. Contact manufacturer for visual inspection criteria.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

* 6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project: 5961-2011-001)

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