The documentation and process conversion measures necessary to comply with this revision shall be completed by 24 January 2021.

INCH-POUND

MIL-PRF-19500/683G
W/AMENDMENT 3
22 October 2021
SUPERSEDING
MIL-PRF-19500/683G
W/AMENDMENT 2
8 April 2020

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT, N-CHANNEL, RADIATION HARDENED, ENCAPSULATED (SURFACE MOUNT AND CARRIER BOARD PACKAGES), TYPE 2N7467, JANTXVR, F, G, AND H AND JANSR, F, G, AND H

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode power MOSFET transistor with radiation hardened total dose and single event (SEE) effects ratings, with avalanche energy maximum rating (EAS) and maximum avalanche current (I_{AS}). Two levels of product assurance (JANTXV and JANS) are provided for each encapsulated device. Provisions for radiation hardness assurance (RHA) to four radiation levels ("R", "F", "G", and "H") are provided for JANTXV and JANS product assurance levels. See 6.7 for JANHC and JANKC die versions.

1.2 Package outlines. The device package outlines are as follows: TO-276AC in accordance with figure 1, TO-276AC with lead option (U2L) in accordance with figure 2, SMD2 TO-276AC with carrier board option (U2S) in accordance with figure 3, and surface mount (U2A) in accordance with figure 4 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type (1)	P_T (2) T_C = +25°C	P_T T_A = +25°C (free air)	$R_{\theta JC}$ (3)	$R_{\theta J}$ Carrier U2S	$R_{\theta J}$ Lid U2L (4)	V_{DS}	V_{DG}	V_{GS}	I_{D1} T_C = +25°C (5) (6)	I_{D2} T_C = +100°C (5) (6)	I_S	I_{DM} (7)	T_J and T_{STG}
	W	W	°C/W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C
2N7467U2, U2A, U2L, U2S	250	2.5	0.50	1.50	10	30	30	±20	75	75	75	300	-55 to +150

(1) Electrical characteristics for the "U2L", "U2A" and “U2S” suffix devices are identical to the non-suffix devices unless otherwise noted.
(2) Derate linearly 2.0 W/°C for T_C > +25°C.
(3) See figure 5, thermal impedance curves.
(4) The Thermal resistance is applicable for mounting methods where a heatsink is attached to the lid for U2L suffix devices.
(5) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and device construction to 75 Amps:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(6) See figure 6, maximum drain current graph.
(7) I_{DM} = 4 X I_{D1} as calculated in note (5).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

AMSC N/A FSC 5961

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc		E_{AS} at I_{D1}	I_{AS}
					T_J = 25°C at I_{D2}	T_J = 150°C at I_{D2}		
	V dc	V dc		µA dc	ohm	ohm	mJ	A
		Min	Max					
2N7467U2, U2A, U2L, U2S	30	2.0	4.0	10	.0035	.006	500	75

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "R", "F", "G", and "H".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbol for the transistors covered by this specification sheet is as follows: "7467".

1.5.3.3 Suffix letters. The suffix letters "U2" are used on devices that are packaged in the SMD2 TO-276AC package of figure 1. The suffix letters "U2L" are used on devices that are packaged in the SMD2 TO-276AC package and have additional flat leads added, see figure 2. The suffix letters "U2S" are used on devices that are packaged in the SMD2 TO-276AC package mounted to a carrier board, see figure 3. The suffix letters "U2A" are used on surface mount devices of figure 4.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.6 Radiation features:

Maximum total ionizing dose (TID) available (Dose rate = 50-300 rad(Si)/s):

For device type 2N7467 (U2, U2A): ..... 100 krads(Si) 1/

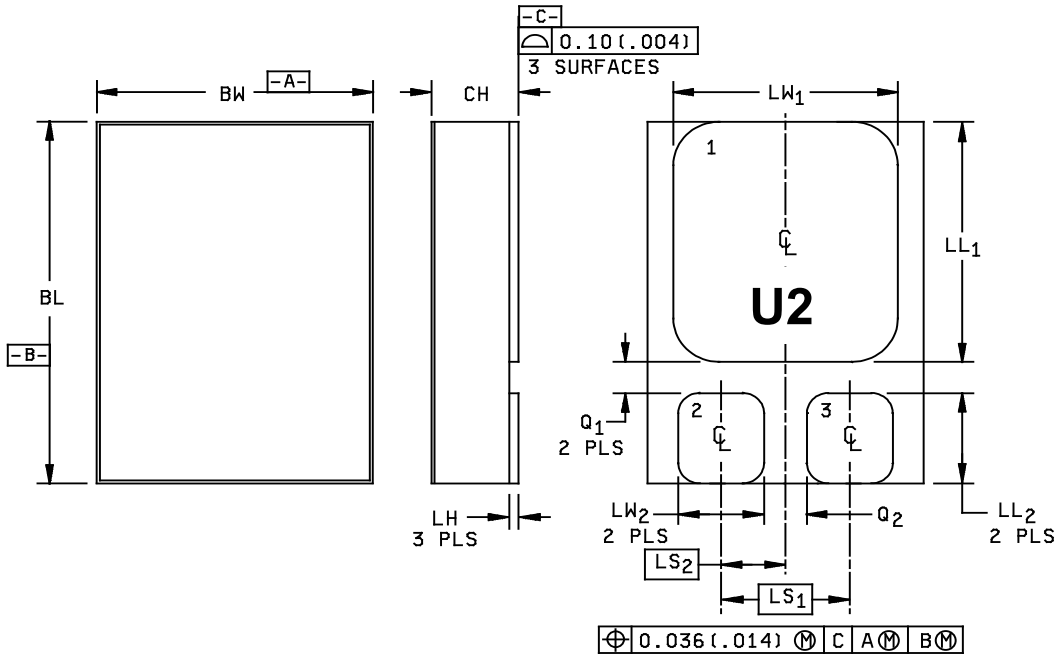
Heavy Ion Single Event Effect (SEE) SEB and SEGR test:

For device type 2N7467 (U2, U2A):

No SEB and SEGR were observed at surface LET (see table V) .....≤ 84 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = 25 V and V_{GS} = -5 V)
(In-situ Bias V_{DS} = 20 V and V_{GS} = -10 V)

1/ Manufacturer supplying device types 2N7467 has performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 100krads (Si).

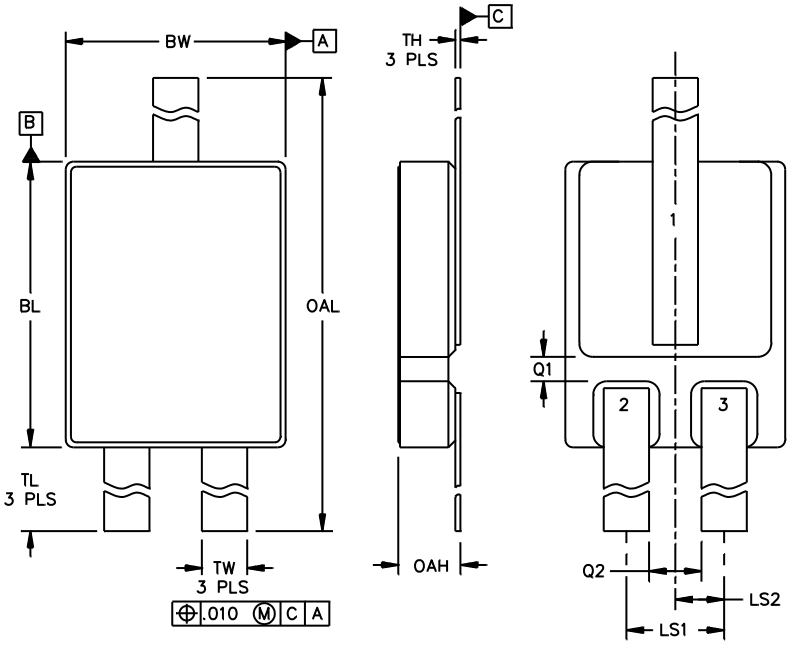
2/ Manufacturer also performed heavy ion SEB and SEGR test at Brookhaven National Lab Accelerator for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.



LTR	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
CH		.141		3.58
LL1	.470	.480	11.94	12.19
LL2	.152	.162	3.86	4.11
LH	.010	.020	.254	.508
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
LW1	.435	.445	11.05	11.30
LW2	.135	.145	3.43	3.68
Q1	.035		.89	
Q2	.050		1.27	

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
* 3. Dimensions and tolerancing shall be in accordance with ASME Y14.5.
4. Terminal 1 – Drain, Terminal 2 – Gate, Terminal 3 – Source

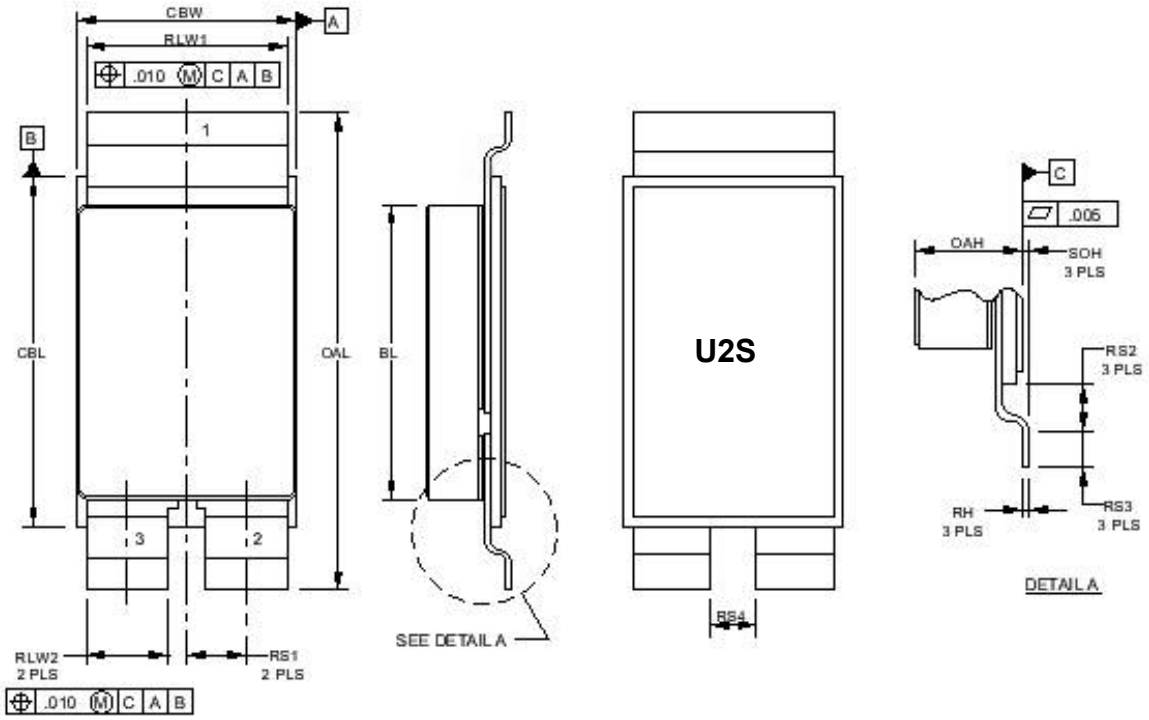
FIGURE 1. Physical dimensions for surface mount - 2N7467U2 (TO-276AC).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
TH	.005	.007	0.127	0.177
TL	.650	.675	16.52	17.14
TW	.095	.105	2.42	2.66
OAH		.150		3.81
OAL	1.985	2.045	50.42	51.94
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
* 4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions, U2 with leaded option (2N7467U2L).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
CBL	.825	.840	20.96	21.34
CBW	.520	.535	13.21	13.59
OAH	.174	.204	4.42	5.18
OAL	1.109	1.144	28.17	29.06
RH	.009	.015	0.23	0.38
RLW1	.473	.497	12.01	12.62
RLW2	.178	.202	4.52	5.13
RS1	.1475 BSC		3.75 BSC	
RS2	.142	.152	3.61	3.86
* RS3	.040	.060	1.02	1.52
RS4	.093		2.36	
SOH	.005	.015	0.13	0.38
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
* 4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

* FIGURE 3. Physical dimensions, U2 with carrier board option (2N7467U2S).

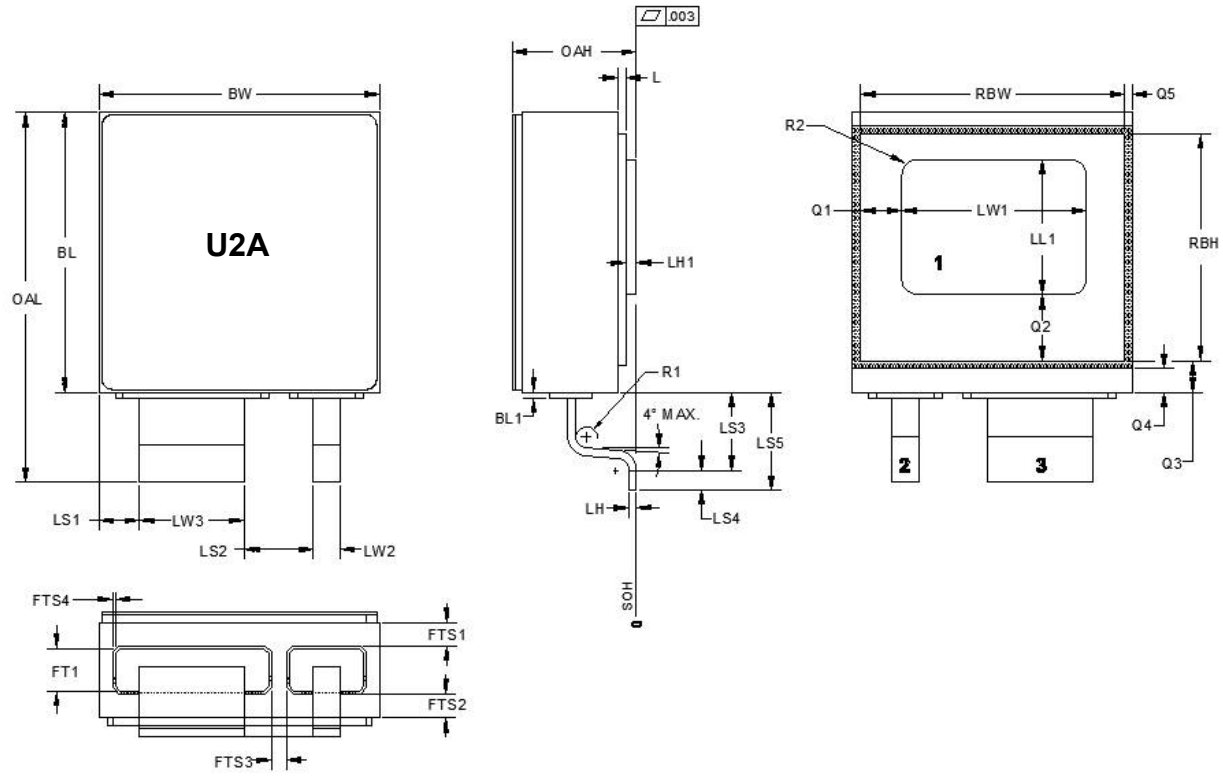


FIGURE 4. Physical dimensions, U2A surface mount.

Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.524	.536	13.31	13.61
BL1	.005	.015	0.13	0.38
BW	.524	.536	13.31	13.61
FT1	.075	.085	1.91	2.16
FTS1	.036		0.91	
FTS2	.036		0.91	
FTS3	.030		0.76	
FTS4	.005 TYP		0.127 TYP	
L	.013	.017	0.33	0.43
LH	.013	.017	0.33	0.43
LH1	.02	.024	0.51	0.61
LL1	.25	.26	6.35	6.60
LS1	.07	.08	1.78	2.03
LS2	.125	.135	3.18	3.43
LS3	.125	.145	3.18	3.68
LS4	.040	.050	1.02	1.27
LS5	.170	.190	4.32	4.83
LW1	.345	.355	8.76	9.02
LW2	.045	.055	1.14	1.4
LW3	.195	.205	4.95	5.21
OAH		.26		6.60
OAL	.71 TYP		18.03 TYP	
Q1	.073	.083	1.85	2.11
Q2	.12	.13	3.05	3.3
Q3	.055	.065	1.4	1.65
Q4	.04		1.02	
Q5	.010	.020	.25	.51
RBH	.425	.435	10.8	11.05
RBW	.495	.505	12.57	12.83
R1	.02		0.51	
R2	.025	.035	0.635	0.889
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.

* FIGURE 4. Physical dimensions, U2A surface mount – continued.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Test Method Standard Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS}..... Rated avalanche current, non-repetitive.
nC ..... nano Coulomb.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (U2, TO-276AC), 2 (U2L, surface mount TO-276AC with additional flat leads added) 3 (U2S, surface mount TO-276AC with additional flat leads added and mounted to a carrier board), and 4 (U2A surface mount) herein. Methods used for the electrical isolation of the terminals shall employ materials that contain a minimum of 90 percent Al_2O_3 (ceramic).

3.4.1 Lead material and finish. Terminal material shall be copper tungsten. Terminal finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of terminal finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction is not permitted to meet the requirements of this specification.

3.4.3 Lead attach or carrier package. Alternations to the device shall be performed on devices that have passed all screening and QCI required per MIL-PRF-19500 and listed herein. When leads or carrier attach is added to the U2 package, as a minimum, the vendor shall perform the tests specified in 4.3.4 herein.

3.4.4 Silicone die coat. The use of a silicone die coat requires a successful completion of MIL-STD-883, method 5011 on each silicone lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container. Devices that have been altered with lead or carrier attached per the specification herein shall have the altered part number on the device or on the device packaging.

3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III (and table IV as applicable) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE (SEB/SEGR) shall be performed in accordance with TM1080 of MIL-STD-750 at initial qualification and after process or design changes which may affect radiation hardness (see table III and table V). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE (SEB/SEGR) characterization data shall be made available upon request of the qualifying or acquiring activity.

4.2.1.2 Lead or carrier attach. For devices that include a lead or carrier attach package configuration qualification shall be performed in accordance with table IV herein, at initial qualification and after process or design changes.

4.3 Screening (JANS, JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance, (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.6)	Not applicable
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{DSS1} = ±500 nA dc or ±100 percent of initial value, whichever is greater	Subgroup 2 of table I herein;
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{DSS1} = ±500 nA dc or ±100 percent of initial value, whichever is greater $\Delta r_{DS(on)1}$ =±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value	Subgroup 2 of table I herein ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater ΔI_{DSS1} = ±500 nA dc or ±100 percent of initial value, whichever is greater $\Delta r_{DS(on)1}$ = ±20 percent of initial value $\Delta V_{GS(th)1}$ = ±20 percent of initial value
17	Method 1081 of MIL-STD-750 (see 4.3.5). End-points: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.5). End-points: Subgroup 2 of table I herein.

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured).
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, $V_{GS(th)1}$, and $r_{DS(ON)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 24 V minimum for t = 250 µs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_{AS}) ..... $I_{AS(max)}$.

b. Peak gate voltage (V_{GS}) ..... 12 V minimum up to rated V_{GS} maximum.

c. Gate to source resistor (R_{GS}) ..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance (L)..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 25 V minimum up to rated V_{GS} maximum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, t_{SW}, (and V_H where appropriate). See table III, group E, subgroup 4 herein.

4.3.4 Lead or carrier attach screening (all quality levels). All surface mount devices with added leads or carrier boards shall be screened as specified herein.

Screen	MIL-STD-750	
	Method	Conditions
1. Hermetic Seal 1/ a. Fine Leak b. Gross Leak	1071	
2. Thermal Response (see 4.3.3) A2 dc Electrical 2/ 3/	3161	Read and record.
3. X-Radiography	2076	The solder material coverage at the package lead pad/SMD carrier sub interfaces shall be 85% minimum
4. External Visual Examination	2071	Cracks or separation of materials shall not be evident on any device after the SMD lead attach assembly operation. Pad and Isolation areas shall be free from foreign matter and extraneous solder. Solder filet coverage at the lead/package lead pad interfaces, along all visible sides, minimum of 75% solder fillet coverage.
5a. Physical dimensions	2066	6 piece sample, each device shall meet the requirements specified in figures 2 and 3.
5b. Terminal Strength	2036	3 piece sample.

1/ Evaluation of surface sorption in accordance with method 1071 shall be performed.
2/ Only DC electrical test specified herein.
3/ When lead carrier bend is requested, the electrical test is performed prior to the bend process.

4.3.5 Dielectric withstanding voltage.

a. Magnitude of test voltage ..... 900 V dc (U2, U2L, U2S), 1,200 V dc (U2A).

b. Duration of application of test voltage ..... 15 seconds (min).

c. Points of application of test voltage..... All leads to case (bunch connection).

d. Method of connection..... Mechanical.

e. Kilovolt-ampere rating of high voltage source ..... 1,200 V/1.0 mA (min).

f. Maximum leakage current..... 1.0 mA.

g. Voltage ramp up time..... 500 V/second.

4.3.6 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500. End-point electrical measurements shall be in accordance with table I, subgroup 2 herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as specified herein.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

Subgroup	Method	Condition
B3	1051	Test condition G, 100 cycles.
B3	2075	See 3.4.2.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	Test condition D. Neither heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
B5	1042	Test condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
B5	1042	Test condition A, V_{DS} = rated; T_A = +175°C; t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
B5	2037	Bond strength; test condition D.

4.4.2.2 Quality level JANTXV, table E-VIB of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening).
B3	1042	Test condition D. Neither heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
B4	2075	See 3.4.2.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
C2	1021	Omit initial conditioning.
C2	2036	Not applicable.
C3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	Thermal resistance, see 4.3.3.
C6	1042	Test condition D. Neither heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with appendix E, table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III (and table IV as applicable) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. The thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, t_{SW} (and V_H where appropriate). See MIL-PRF-19500, table E-IX, group E, subgroup 4.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0 V dc, I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$	30		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.0	4.0	V dc
Gate current	3411	V_{GS} = +20 V dc bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 24 V dc	I_{DSS1}		10	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$		.0035	Ω
Forward voltage	4011	Condition A, $I_D = I_{D1}$, V_{GS} = 0 V dc	V_{SD}		1.3	V
Subgroup 3						
High-temperature operation:		$T_C = T_J$ = +125°C				
Gate current	3411	V_{GS} = +20 V dc and -20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		± 200	nA dc
Drain current	3413	V_{GS} = 0 V dc, bias condition C, V_{DS} = 24 V dc	I_{DSS2}		25	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$		.0055	Ω
Gate to source voltage (thresholds)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.0		V dc
Low-temperature operation:		$T_C = T_J$ = -55°C				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.0	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4						
Forward transconductance	3475	I_D = 45 A, V_{DD} = 15 V (see 4.5.1)	g_{FS}	45		
Switching time test	3472	I_D = 45 A, V_{GS}= 12 V dc, R_G = 2.35Ω, V_{DD} = 15 V dc				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r		125	ns
Turn-off delay time			$t_{d(off)}$		80	ns
Fall time			t_f		50	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 7; t_p = 10 ms V_{DS} = 24 V				
Electrical measurements		See table I, subgroup 2 herein.				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B, I_D = 45 A				
On-state gate charge			$Q_{G(on)}$		200	nC
Gate to source charge			Q_{GS}		55	nC
Gate to drain charge			Q_{GD}		40	nC
Reverse recovery time	3473	$d_i/ d_t \leq$ 100 A/μs, condition A, $V_{DD} \leq$ 25 V, I_D = 45 A	t_{rr}		165	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

	Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
		Method	Conditions		R, F, G and H		R, F and G		H 4/		
					Min	Max	Min	Max	Min	Max	
	Subgroup 1										
	Not applicable										
	Subgroup 2		T_C = +25°C								
*	Steady-state total dose irradiation (V_{GS} bias) 5/	1019	Condition A, V_{GS} = 12V V_{DS} = 0								
*	Steady-state total dose irradiation (V_{DS} bias) 5/	1019	Condition A, V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)								
	End-point electricals:										
	Breakdown voltage, drain to source	3407	Bias condition C V_{GS} = 0 I_D = 1 mA	$V_{(BR)DSS}$	30		30		30		V dc
	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	V_{GSth1}	2.0	4.0	2.0	4.0	1.5	4.0	V dc
	Gate current	3411	Bias condition C V_{GS} = 20 V V_{DS} = 0	I_{GSSF1}		100		100		100	nA dc
	Gate current	3411	Bias condition C V_{GS} = -20 V V_{DS} = 0	I_{GSSR1}		-100		-100		-100	nA dc
	Drain current	3413	Bias condition C V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		10		10		25	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
	Method	Conditions		R, F, G and H		R, F and G		H 4/		
				Min	Max	Min	Max	Min	Max	
Subgroup 2 -Continued										
Static drain to source on-state voltage 6/	3405	Condition A V_{GS} = 12 V pulsed (see 4.5.1) I_D= 45 A	V_{Dson1}		.180		.180		.2025	V dc
Static drain to source on-state voltage	3405	Condition A V_{GS} = 12 V pulsed (see 4.5.1) I_D= 45 A	V_{Dson1}		.1575		.1575		.180	V dc
Forward voltage source to drain diode	4011	Condition A, V_{GS} = 0, I_D= 45 A	V_{SD}		1.3		1.3		1.3	V dc

1/ For sampling plan, see MIL-PRF-19500.
2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its' qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ The "H" designation represents devices which pass end-points at the G, R, and F designated Total-Ionizing-Dose (TID).
5/ Separate samples shall be pulled for each bias.
6/ Limit using TO-204AE package. The higher package resistance necessitates the higher V_{DSon1} limit when the manufacturer uses the alternate package as allowed in 4/ above.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

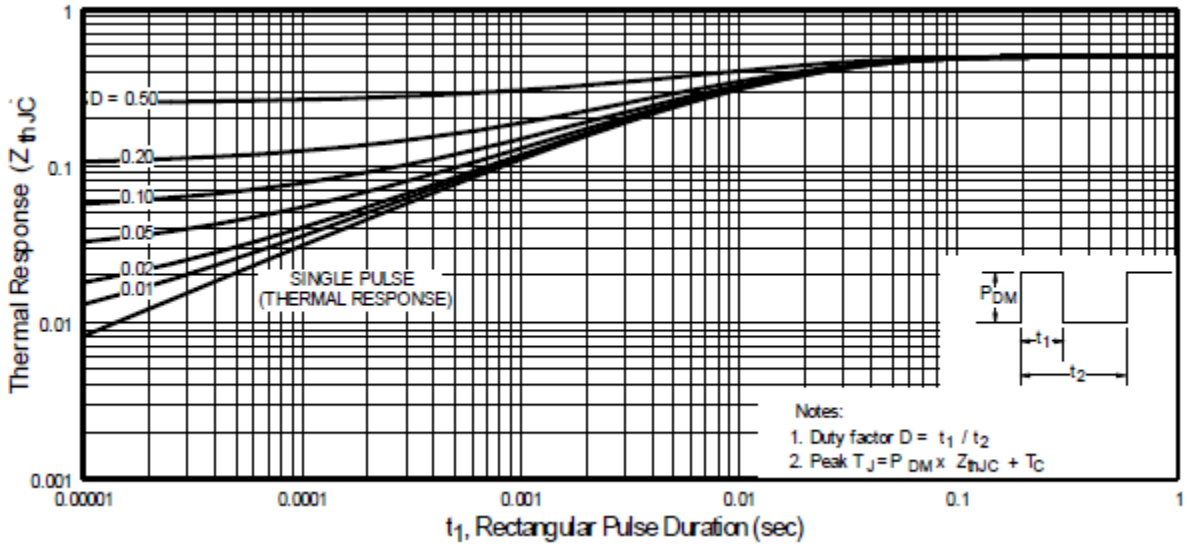
Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			
Not applicable			
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
Subgroup 11			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level linear energy transfer (LET) is sufficient to qualify all lower level LETs.

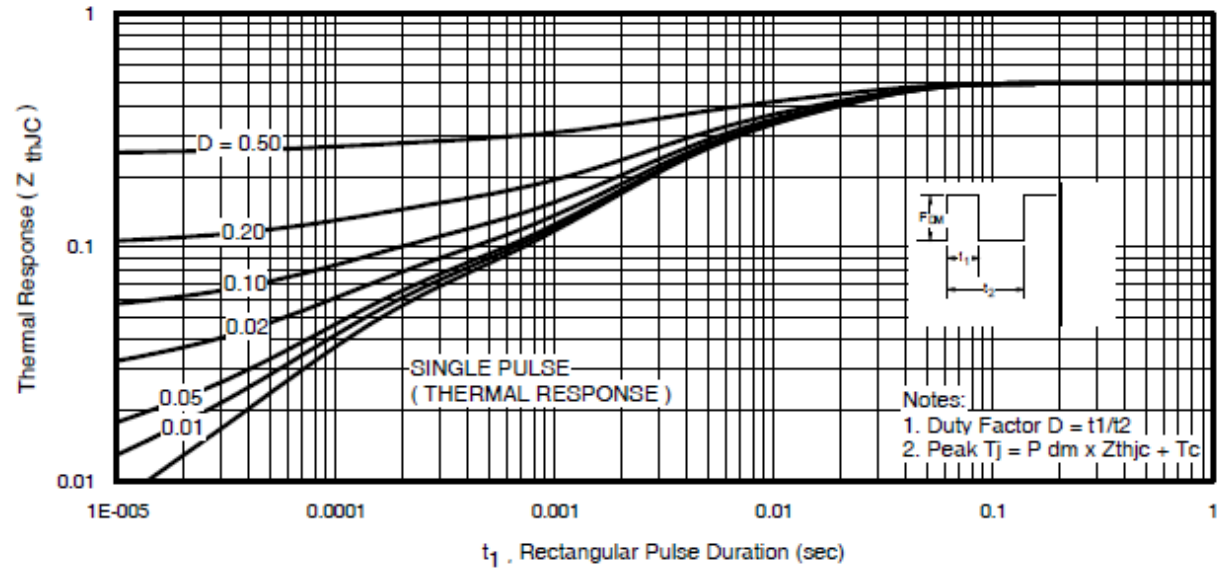
TABLE IV. Lead alternation qualification inspection requirements.

Inspections 1/	MIL-STD-750		Sample size
	Method	Conditions	
Subgroup 1			6 devices, c = 0
Temperature cycle	1051	100 Temp cycles, test condition G or maximum storage temperature.	
Hermetic seal Fine leak Gross leak	1071		
A2 dc electrical		Read and record.	
Thermal response	3161		
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	
Subgroup 2			6 devices, c = 0
Intermittent operating life	1042	Condition D; 6,000 cycles.	
A2 dc electrical		Read and record.	
Thermal response	3161		
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	
Subgroup 3			6 devices, c = 0
Terminal strength	2036	Tension; Condition A 10lbs for 10 seconds Fatigue; Condition E 3 arcs of 90 +/_5 degrees each 8.0 oz.	
A2 dc electrical		Read and record.	
External visual examination	2071	Cracks or separation of materials shall not be evident on test samples.	

1/ Qualification samples performed on non-formed leaded devices.

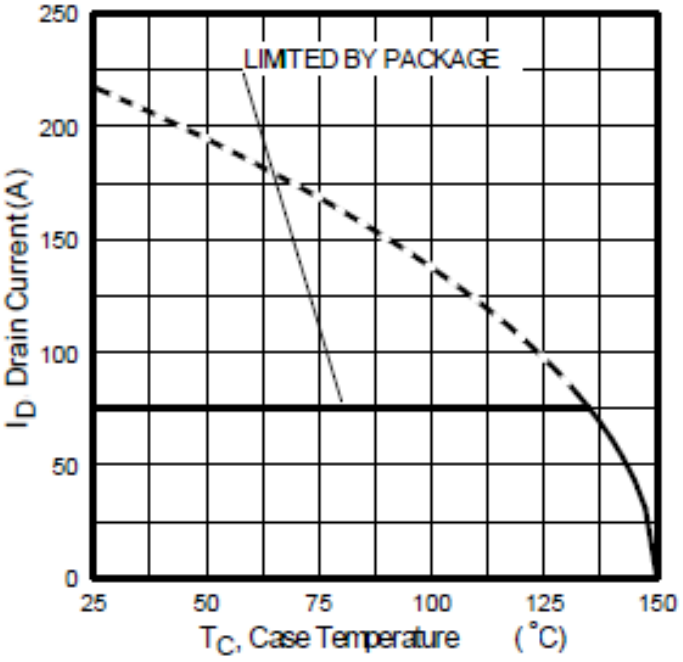


2N7467U2, U2L, U2S

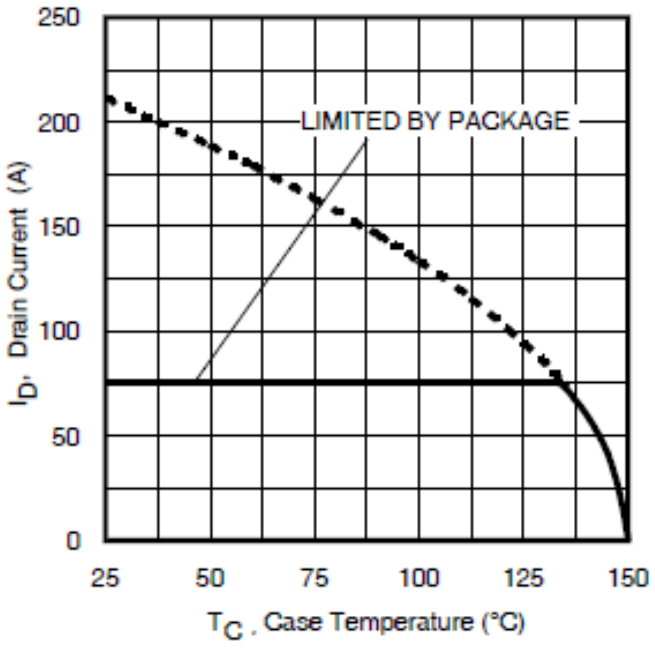


2N7467U2A

FIGURE 5. Thermal impedance curves.

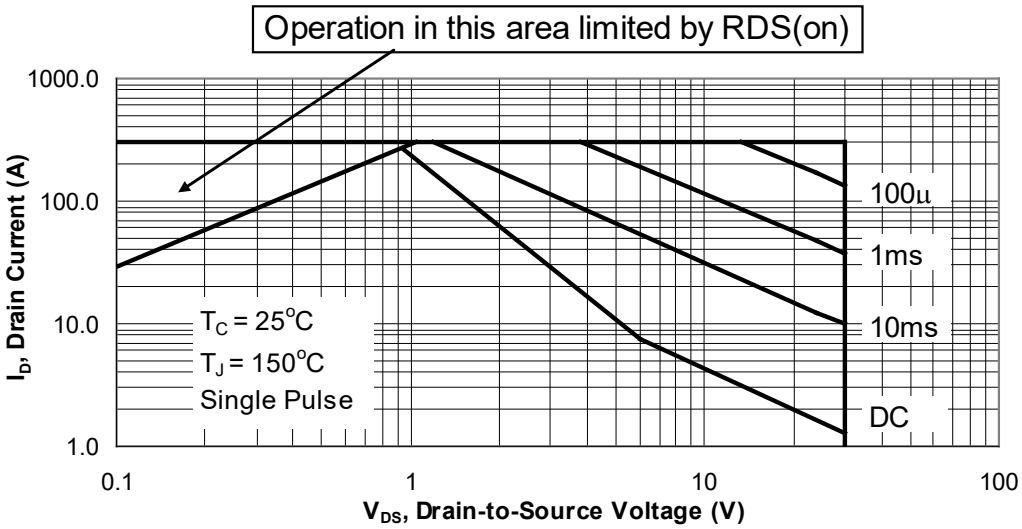


2N7467U2, U2L, U2S

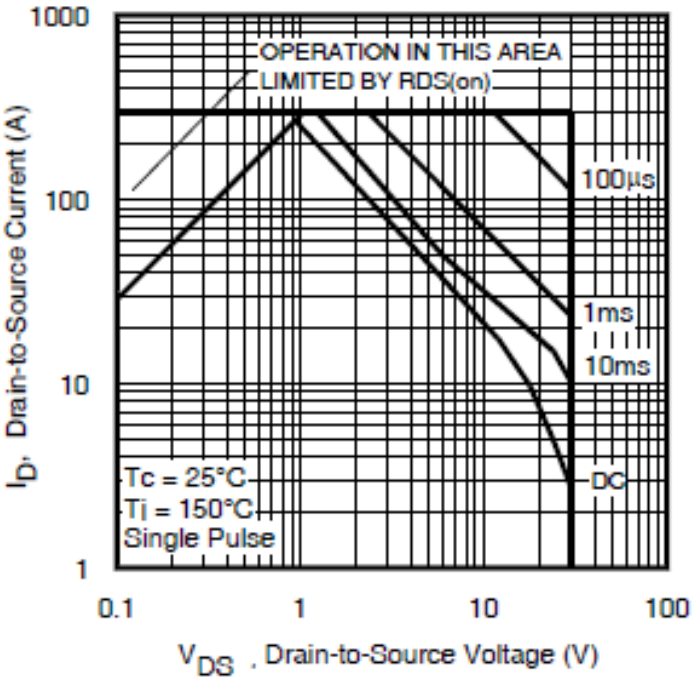


2N7467U2A

FIGURE 6. Maximum drain current versus case temperature graph.



2N7467U2, U2L, U2S



2N7467U2A

FIGURE 7. Safe operating area graphs.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

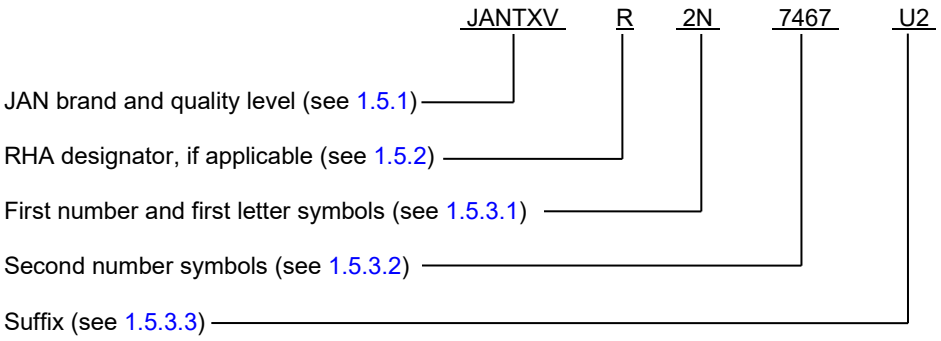
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.

f. If SEE testing data is desired, it should be specified in the contract or order (see 4.2.1.1).

g. If specific SEE characterization conditions are desired (see section 6.8 and table V), manufacturer's cage code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://qpldocs.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7467U2	JANTXV#2N7467U2	JANS2N7467U2	JANS#2N7467U2
JANTXV2N7467U2A	JANTXV#2N7467U2A	JANS2N7467U2A	JANS#2N7467U2A
JANTXV2N7467U2L	JANTXV#2N7467U2L	JANS2N7467U2L	JANS#2N7467U2L
JANTXV2N7467U2S	JANTXV#2N7467U2S	JANS2N7467U2S	JANS#2N7467U2S

(1) The number sign (#) represents one of four RHA designators available on this specification sheet ("R" "F", "G" or "H").

6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types	Commercial types
2N7467U2 2N7467U2A	IRHNA57Z60 IRHNS57Z60

6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet MIL-PRF-19500/741.

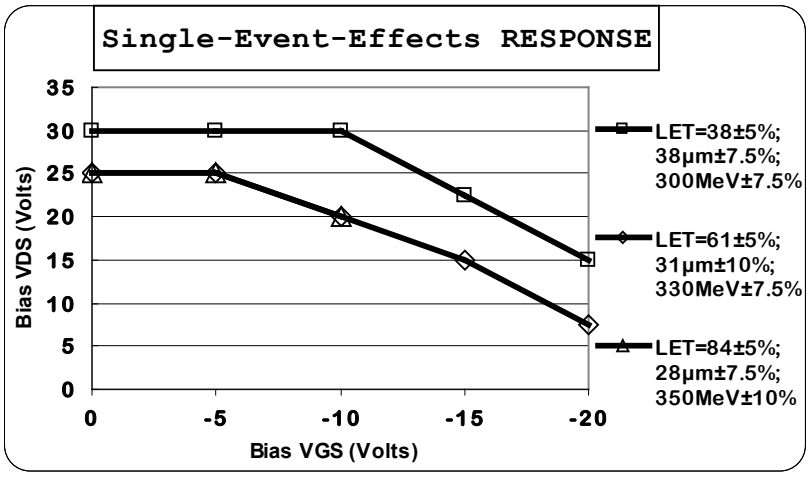
6.8 Application data.

* 6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this specification sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table V) for information only. SEE (SEB and SEGR) conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE V. Manufacturers characterization conditions.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
* 69210 (Applicable to devices with a date code of 21 August 2012 and older)	SEE 1/	1080.0	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 8.	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25º ±5 °C Surface LET = 38 MeV-cm2/mg ±5%, range = 38 µm ±7.5%, energy = 300 MeV ±7.5%. In situ bias conditions: V_{DS} = 30 V and V_{GS} = -10 V, V_{DS} = 22.5 V and V_{GS} = -15 V, V_{DS} = 15 V and V_{GS} = -20 V, (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator). Surface LET = 61 MeV-cm2/mg ±5%, range = 31 µm ±10%, energy = 330 MeV ±7.5%. In situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V, V_{DS} = 20 V and V_{GS} = -10 V, V_{DS} = 15 V and V_{GS} = -15 V, V_{DS} = 7.5 V and V_{GS} = -20 V, (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator). Surface LET = 84 MeV-cm2/mg ±5%, range = 28 µm ±7.5%, energy = 350 MeV ±7.5%. In situ bias conditions: V_{DS} = 25 V and V_{GS} = -5 V, V_{DS} = 20 V and V_{GS} = -10 V, (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator).	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers should provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.



* FIGURE 8. Cage 69210 typical SEE response graph.

6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review Activities:
Air Force - 19

Preparing activity:
DLA - CC

(Project 5961-2021-077)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.