

The documentation and process conversion measures necessary to comply with this revision shall be completed by 26 September 2016.

INCH-POUND

MIL-PRF-19500/682C
24 June 2016
SUPERSEDING
MIL-PRF-19500/682B
1 March 2013

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DIODE, SILICON, SCHOTTKY
POWER RECTIFIER, SURFACE MOUNT,
TYPE 1N6845U3, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, schottky power rectifier. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided as specified in [MIL-PRF-19500](#).

* 1.2 Package outlines. The device package outline for this specification sheet is a U3 in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Column 1	Column 2	Column 3	Column 4	Column 5
Types	V_{RWM}	$I_O (1)$ $T_C = +100^\circ\text{C}$	I_{FSM} $t_p = 8.3 \text{ ms}$ $T_C = +25^\circ\text{C}$	T_{STG} and T_J
	V dc	A dc	A (pk)	$^\circ\text{C}$
1N6845U3	45	30	300	-65 to +150

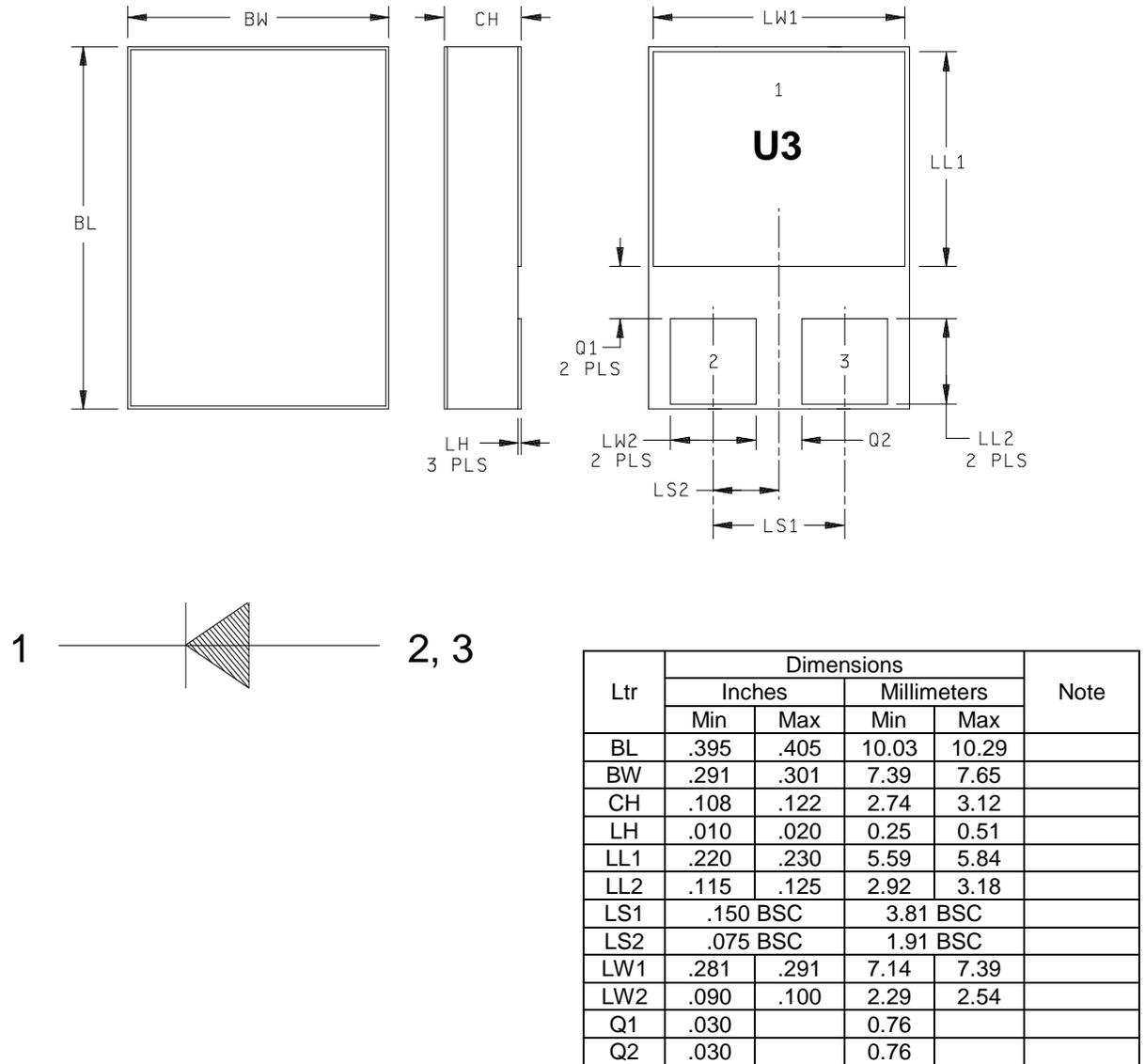
(1) Derate linearly at 400 mA/ $^\circ\text{C}$ from $T_J = T_C = +125^\circ\text{C}$ to + 150 $^\circ\text{C}$. See [figure 2](#).

1.4 Primary electrical characteristics. $R_{\theta JC} = 2.0^\circ\text{C/W}$ maximum, C_J at 10 V dc = 800 pF.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.



MIL-PRF-19500/682C



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. In accordance with ASME Y14.5M, diameters are equivalent to Φ x symbology.

FIGURE 1. Physical dimensions.

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.4](#) for PIN construction example and [6.5](#) for a list of available PINs.

* 1.5.1 JAN certification mark and quality level. The JAN certification mark and quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The semiconductor of this specification sheet use the first number and letter symbols "1N".

* 1.5.2.2 Second number symbols. The second number symbols for the semiconductor covered by this specification sheet are as follows: "6845".

* 1.5.3 Suffix symbols. The suffix symbols "U3" Indicates a 3 pad surface mount package (see [figure 1](#)).

* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and on [figure 1](#) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in [tables I](#) and [II](#) herein.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500 and herein.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II herein).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTXV, and JANTX levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement	
	JANS level	JANTX and JANTXV levels
(1) (2) 3b	Method 4066 of MIL-STD-750, condition A, one pulse, $t_p = 8.3$ ms, $I_O = 0$, $V_{RWM} = 0$, I_{FSM} = see 1.3 herein	Method 4066 of MIL-STD-750, condition A, one pulse, $t_p = 8.3$ ms, $I_O = 0$, $V_{RWM} = 0$, I_{FSM} = see 1.3 herein
(2) 3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
3d	Avalanche energy test (see 4.3.3)	Avalanche energy test (see 4.3.3)
4, 5, 8	Required	Not applicable
9, 10	Not applicable	Not applicable
11	V_{F1} and I_{R1}	V_{F1} and I_{R1}
12	See 4.3.1 240 hours	See 4.3.1 48 hours
13	Subgroup 2 and 3, of table I herein, V_{F1} and I_{R1} ; $\Delta V_{F1} = \leq 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or ± 50 uA, whichever is greater	Subgroup 2, of table I herein; V_{F1} and I_{R1} ; $\Delta V_{F1} = \leq 50$ mV (pk); $\Delta I_{R1} = \pm 100$ percent from the initial value or ± 50 uA, whichever is greater

- (1) Surge shall precede thermal impedance.
- (2) Shall be performed anytime after temperature cycling, screen 3a. JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 High temperature reverse bias. Reverse bias conditions are as follows: Method 1038 of MIL-STD-750, test condition A, $V_R = 36$ V dc; $T_J = +125^\circ\text{C}$.

* 4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3101 or 4081 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , and t_{MD} . See table III, subgroup 4 herein.

4.3.3 Avalanche energy test. The avalanche energy test is to be performed with method 4064 of MIL-STD-750, using the circuit as shown on figure 3 or equivalent. The Schottky rectifier under test must be capable of absorbing the reverse energy, as follows: $I_{AS} = 1$ A, $V_{RWM} = 45$ V minimum, $L = 150$ μH .

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#), and [table I](#) herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of [table II](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables E-VIA (JANS) and E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#) and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with [table II](#) herein.

4.4.2.1 Group B inspection, table E-VIA (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$\Delta T_J = +85^\circ\text{C}$, $I_F = 2$ A minimum for 2,000 cycles.
B5	1038	Condition A, $V_R = 36$ V dc, $T_J = +125^\circ\text{C}$, $t = 340$ hours min; heat sinking allowed. This test shall be extended to 1000 hours on each JANS wafer lot.

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1037	$\Delta T_J = +85^\circ\text{C}$, $I_F = 2$ A minimum for 2,000 cycles.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#). Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2, forward voltage test (V_{F1}) and reverse leakage test (I_{R1}) herein. Delta measurements shall be in accordance with [table II](#) herein.

4.4.3.1 Group C inspection, table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Not applicable.
C5	4081	Limit for thermal resistance for 1N6845U3 is 2.0°C/W .
C6	1037	$\Delta T_J = +85^\circ\text{C}$, $I_F = 2$ A minimum for 6,000 cycles.
C6	1038	Condition A, $V_R = 36$ V dc, $T_J = +125^\circ\text{C}$, $t = 1,000$ hours minimum (required for TX, TXV only) (heat sinking allowed).

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table III](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

MIL-PRF-19500/682C

* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3101	See 4.3.2	Z _{θJX}			°C/W
Forward voltage	4011	Condition B, I _F = 10 A (pk), pulsed test (see 4.5.1)	V _{F1}	.65		V dc
Forward voltage	4011	Condition B, I _F = 20 A (pk), pulsed test (see 4.5.1)	V _{F2}	.72		V dc
Forward voltage	4011	Condition B, I _F = 40 A (pk), pulsed test (see 4.5.1)	V _{F3}	.86		V dc
Reverse current	4016	V _R = 45 V, DC method, pulsed test (see 4.5.1)	I _{R1}		100	μA dc
<u>Subgroup 3</u>						
High temperature operation:		T _C = +100°C				
Forward voltage	4011	Condition B, I _F = 10 A (pk), pulsed test (see 4.5.1)	V _{F4}	.55		V dc
Forward voltage	4011	Condition B, I _F = 20 A (pk), pulsed test (see 4.5.1)	V _{F5}	.67		V dc
Reverse current	4016	V _R = 45 V, DC method, pulsed test (see 4.5.1)	I _{R2}		10.0	mA dc
Low temperature operation:		T _C = -55°C				
Forward voltage	4011	Condition B, I _F = 10 A (pk), pulsed test (see 4.5.1)	V _{F6}	.78		V dc
<u>Subgroup 4</u>						
Capacitance	4001	V _R = 5 V dc, f = 1 MHz, V _{SIG} = 50 mV (p-p)	C _J		800	pF
<u>Subgroup 5</u>						
Not applicable						

See footnotes at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 6</u>						
Surge	4066	Condition A, see 1.3, column 4 herein, ten surges each diode, 60 seconds between surges, (see 4.5.1)	IFSM			
Electrical measurements		See table I, subgroup 2 herein				
<u>Subgroup 7</u>						
Dielectric withstanding voltage	1016	$V_R = 500$ V dc; all leads shorted; measure from leads to case	DWV		10	μ A
Scope display evaluation	4023	Stable only				
Electrical measurements		See table I, subgroup 2 herein				

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:
 Group B, subgroups 3, 4 and 5 (JANS).
 Group B, subgroups 2 and 3 (JAN, JANTX, JANTXV).
 Group C, subgroups 2 and 6.
 Group E, subgroup 1.

TABLE II. Groups B, C, and E delta requirements. 1/ 2/ 3/ 4/ 5/ 6/

Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Forward voltage 1N6845U3	4011	Condition B, $I_F = 20$ A (pk), pulsed (see 4.5.1)	ΔV_{F2}	± 50 mV dc from initial reading.		
2.	Reverse current	4016	DC method , $V_R = 45$ V dc	ΔI_{R1}	50 μ A or ± 100 percent from initial reading, whichever is greater.		

- 1/ Each individual diode.
- 2/ The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows:
- Subgroup 4, see table II herein, steps 1 and 2.
 - Subgroup 5, see table II herein, steps 1 and 2.
- 3/ The delta measurements for table E-VIB (JAN, JANTX and JANTXV) of MIL-PRF-19500 are as follows:
- Subgroup 2, see table II herein, steps 1 and 2.
 - Subgroup 3, see table II herein, steps 1 and 2.
 - Subgroup 6, see table II herein, steps 1 and 2.
- 4/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows:
- Subgroups 2 and 3, see table II herein, steps 1 and 2 for all levels.
 - Subgroup 6, see table II herein, steps 1 and 2 for all levels.
- 5/ Devices which exceed the table I limits for this test shall not be accepted.
- 6/ The delta measurements for table E-IX of MIL-PRF-19500 are as follows:
- Subgroup 1, see table II herein, steps 1 and 2.
 - Subgroup 2, see table II herein, steps 1 and 2.

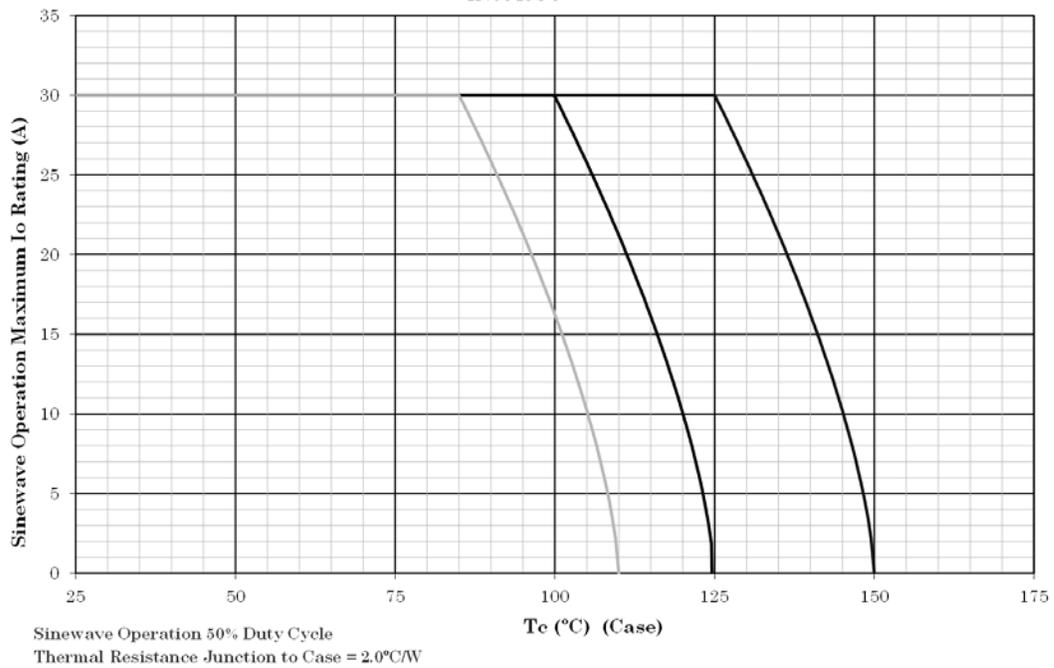
MIL-PRF-19500/682C

TABLE III. Group E inspection (all quality levels) – for qualification and requalification only.

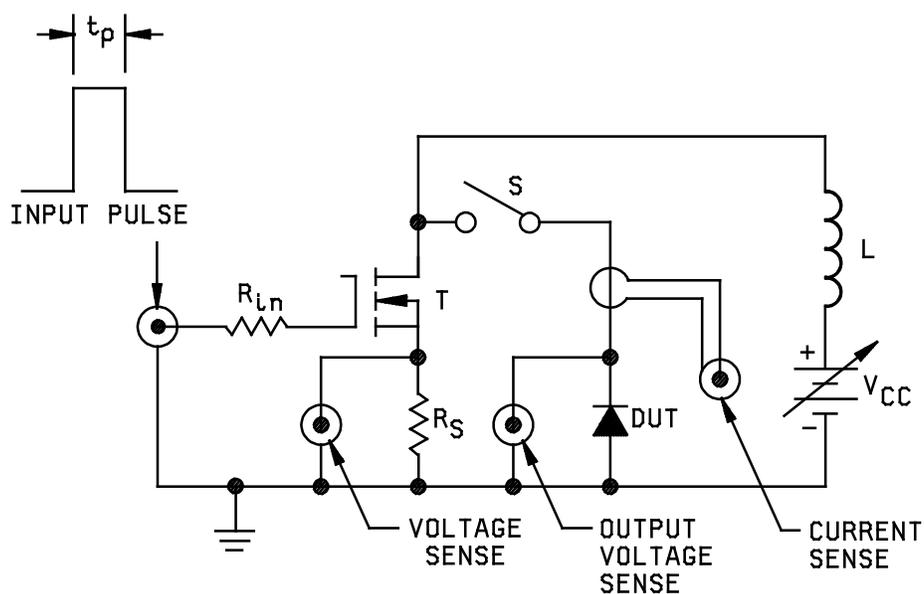
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			n = 45, c = 0
Temperature cycling (air to air)	1051	Test condition G, 500 cycles, -55°C to +150°C.	
Hermetic seal	1071		
Electrical measurements		See table I , subgroup 2 and table II herein.	
<u>Subgroup 2</u>			n = 45, c = 0
Life test	1048	t = 1,000 hours, T _J = +125°C, V _R = 36 V dc.	
Electrical measurements		See table I , subgroup 2 and table II herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10</u>			n = 5, c = 0
Surge	4066		
1N6845U3		Condition A, T _A = +25°C, I _{FSM} = 300 A, 100 surges of 8.3 ms superimposed on I _O . V _R = 0; I _O = 0 A pk half sine wave, continuous.	
Electrical measurements		See table I subgroup 2.	

Temperature-Current Derating Curve

1N6845U3



* FIGURE 2. Temperature-current derating curve.



Input pulse $R_{in} = 50$ ohms, 1 watt
 $V_G = 10$ Volts, $R_S = 0.1$ ohms, 1 watt
 $Z_G = 50$ ohms
 $L = 150 \mu\text{H}$
 $P.W. \approx 30 \mu\text{s}$
 Duty cycle ≤ 1 percent, $T = \text{IRF350/2N6768}$ or equivalent

Procedure:

1. With S open, adjust pulse width to a test current of 1 amp through R_S .
2. Close S, verify test current with current sense.
3. Read peak output voltage (see 4.3.3).

FIGURE 3. Peak reverse energy test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

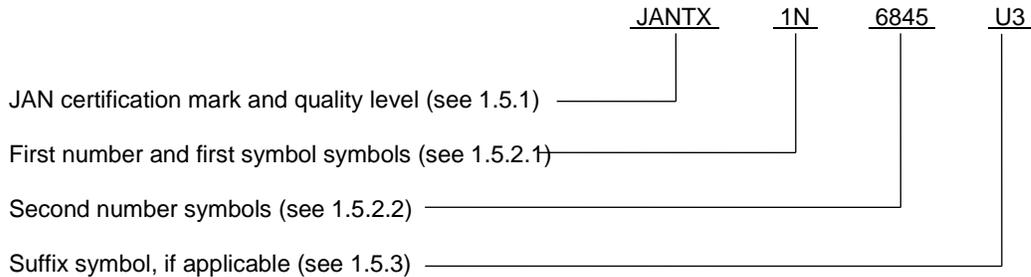
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).

* d. The complete Part or Identifying Number (PIN), see 1.2.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs. The following is a list of possible PINs (without JAN prefix) available on this specification sheet.

List of PINs	
JAN1N6845U3	JANTXV1N6845U3
JANTX1N6845U3	JANS1N6845U3

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

* 6.7 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

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 Army - CR
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Preparing activity:
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