The documentation and process conversion measures necessary to comply with this revision shall be completed by 3 December 2021.

INCH-POUND

MIL-PRF-19500/676G
w/AMENDMENT 1
3 September 2021
SUPERSEDING
MIL-PRF-19500/676G
7 June 2018

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED, N-CHANNEL, SILICON, TYPES 2N7465 AND 2N7466, JANTXVR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened, power transistor. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). Provisions for radiation hardness assurance (RHA) to one radiation level "R" is provided for JANS and JANTXV product assurance levels.

1.2 Package outlines. The device package outlines are as follows: TO-257AA in accordance with figure 1 and TO-276AA (U3) surface mount in accordance with figure 2 for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

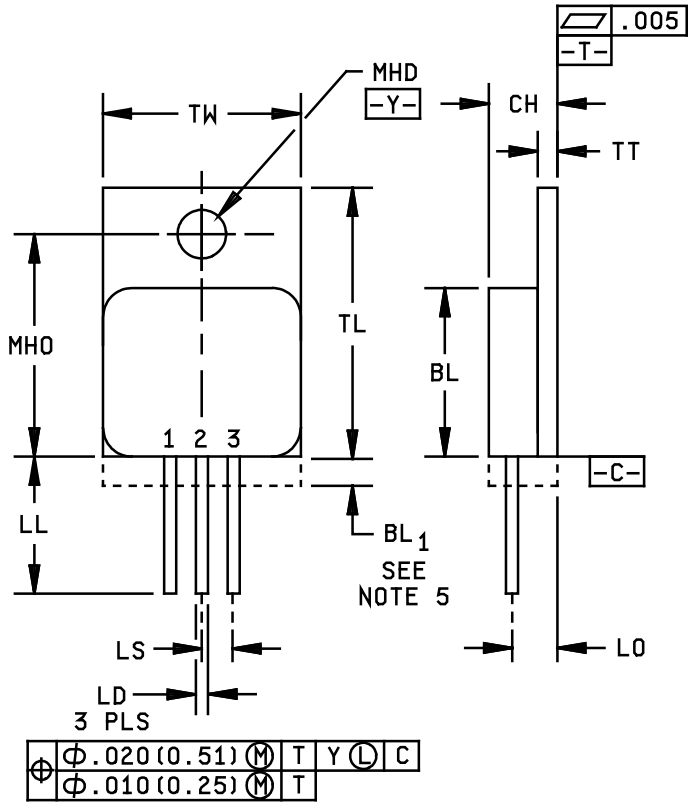
Type	P_T (1) T_C = +25°C	P_T T_A = +25°C (free air)	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C = +25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	V_{ISO} 70,000 foot altitude	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	V dc	°C
2N7465T3, U3	75	2	1.67	400	400	±20	5.0	3.2	5.0	20	400	-55 to +150
2N7466T3, U3	75	2	1.67	500	500	±20	4.4	2.8	4.4	17.6	500	

(1) Derate linearly 0.6 W/°C for T_C > +25°C.
(2) See figure 4, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graphs.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

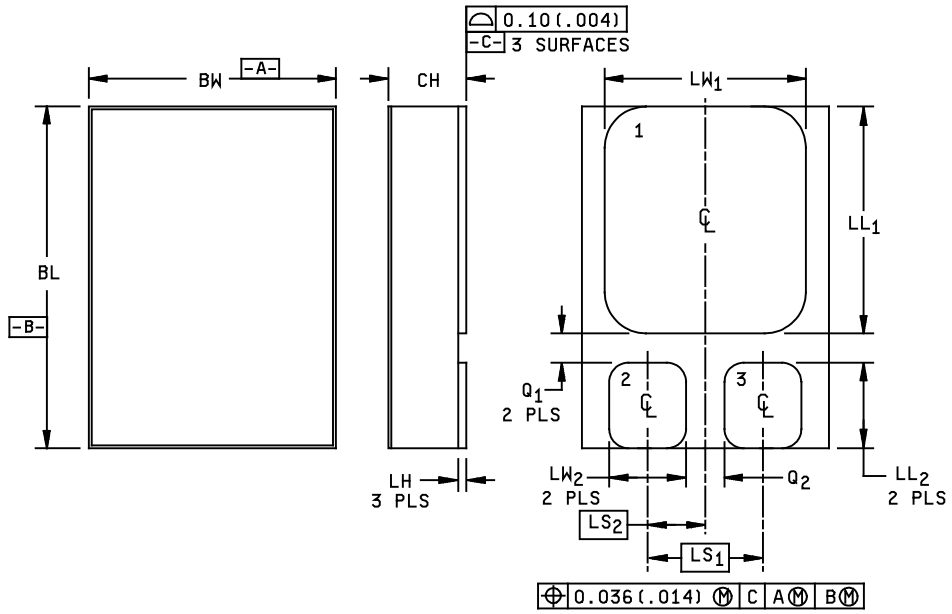
Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.



Ltr	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
BL_1		.033		0.84
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
* 4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.
5. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).

FIGURE 1. Physical dimensions for TO-257AA (2N7465T3 and 2N7466T3).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH		.124		3.15
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.76	
Q2	.030		0.76	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for general information only.
* 3. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

FIGURE 2. Physical dimensions for TO-276AA (2N7465U3 and 2N7466U3).

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = 1.0 mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = 1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80 percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) V_{GS} = 12 V dc		E_{AS} at I_{D1}	I_{AS}
					T_J = +25°C at I_{D2}	T_J = +150°C at I_{D2}		
	V dc	V dc		µA dc	ohm	ohm	mJ	A
		Min	Max					
2N7465T3, U3	400	2.5	4.5	50	1.39	3.0	150	5.0
2N7466T3, U3	500	2.5	4.5	50	1.77	3.9	150	4.4

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JANTXV” and "JANS".

1.5.2 Radiation hardness assurance (RHA) designator. The RHA level that is applicable for this specification sheet is level "R".

1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7465" and "7466".

1.5.3.3 Suffix letters. The suffix letters "T3" are used on devices that are packaged in the TO-257AA package of figure 1. The suffix letters "U3" are used on devices that are packaged in the TO-276AA package of figure 2.

1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.6 Radiation features:

Maximum total ionizing dose (TID) available (Dose rate = 50-300 rad(Si)/s):

For device type 2N7465U3: ..... 100 krads(Si) 1/

Heavy Ion Single Event Effect (SEE) SEB and SEGR test:

For device types 2N7465T3, 2N7465U3:

No SEB and SEGR were observed at surface LET (see table IV) .....≤ 37 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = 325 V and V_{GS} = -10 V)
(In-situ Bias V_{DS} = 275 V and V_{GS} = -15 V)

For device type 2N7466T3, 2N7466U3:

No SEB and SEGR were observed at surface LET (see table IV) .....≤ 37 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = 350 V and V_{GS} = -10 V)
(In-situ Bias V_{DS} = 325 V and V_{GS} = -15 V)
(In-situ Bias V_{DS} = 300 V and V_{GS} = -20 V)

1/ Manufacturer supplying device type 2N7465U3 has performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 100krads (Si).

2/ Manufacturer also performed heavy ion SEB and SEGR test at Brookhaven National Lab Accelerator for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
MIL-STD-883 - Test Methods Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil/

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS}..... Rated avalanche current, non-repetitive.
nC ..... nano Coulomb.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (TO-257AA) figure 2 (U3, surface mount, TO-276AA) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

* 3.4.4 Silicone die coating. The use of a silicone die coat requires a successful completion of MIL-STD-883, method 5011 on each silicone lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.

3.5 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools, and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, $R \leq 100\ k\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE (SEB and SEGR) shall be performed in accordance with TM1080 of MIL-STD-750 at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the performance specification sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E_{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein, ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$= ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI_{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI_{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ±20 percent of initial value. $\Delta V_{GS(TH)1}$= ±20 percent of initial value.
17	For TO–257AA and TO-276AA packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein	For TO–257AA and TO-276AA packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein

(1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
(2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and $V_{GS(th)1}$ shall be invoked.
(3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV does not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply V_{GS} = 30 V minimum for t = 250 μs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current (I_{AS}) ..... $I_{AS(max)}$.

b. Peak gate voltage (V_{GS}) ..... 12 V.

c. Gate to source resistor (R_{GS}) ..... $25\Omega \leq R_{GS} \leq 200\Omega$.

d. Initial case temperature (T_C) ..... +25°C +10°C, -5°C.

e. Inductance (L) ..... $\left[\frac{2E_{AS}}{(I_{D1})^2}\right]\left[\frac{V_{BR} - V_{DD}}{V_{BR}}\right]$ mH minimum.

f. Number of pulses to be applied ..... 1 pulse minimum.

g. Supply voltage (V_{DD}) ..... 50 V.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{MD}, t_{SW}, (and V_H where appropriate). (See figure 4 herein.) See table III, group E, subgroup 4 herein.

* 4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

* 4.3.5 Dielectric withstanding voltage.

a. Magnitude of test voltage ..... 800 V dc (TO-257AA); 900 V dc (TO-276AA).

b. Duration of application of test voltage ..... 15 seconds (min).

c. Points of application of test voltage ..... All leads to case (bunch connection).

d. Method of connection ..... Mechanical.

e. Kilovolt-ampere rating of high voltage source ..... 1,200 V/1.0 mA (min).

f. Maximum leakage current ..... 1.0 mA.

g. Voltage ramp up time ..... 500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and herein.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

	Subgroup	Method	Condition
	B3	1051	Test condition G, 100 cycles.
	B3	2075	See 3.4.2 herein.
	B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
*	B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	B4	1042	Condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
*	B5	1042	Accelerated steady-state gate bias, Test condition B, V_{GS} = rated T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
*	B5	1042	Accelerated steady-state reverse bias, Condition A, V_{DS} = rated; T_A = +175°C; t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.

4.4.2.2 Quality levels JANTXV, table E-VIB of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles. (45 total, including 20 cycles performed in screening)
B3	1042	Test condition D. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.
B4	2075	See 3.4.2 herein.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

	Subgroup	Method	Condition
	C2	1056	Test condition B.
	C2	2036	Test condition A, weight = 10 lbs (4.54 Kg), t = 10 s (applicable to TO-257AA only).
*	C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	C5	3161	See 4.3.3, $R_{\theta JC}$ = 1.67 °C/W.
	C6	1042	Test condition D, 6,000 cycles. No heat sink nor forced-air cooling on the device shall be permitted during the on cycle. The heating cycle shall be 60 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	V_{GS} = 0, I_D = 1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N7465T3, U3				400		V dc
2N7466T3, U3				500		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)1}$	2.5	4.5	V dc
Gate reverse current	3411	V_{GS} = +20 V dc bias condition C, V_{DS} = 0	I_{GSSF1}		+100	nA dc
Gate reverse current	3411	V_{GS} = -20 V dc, bias condition C, V_{DS} = 0	I_{GSSR1}		-100	nA dc
Drain current	3413	V_{GS} = 0 , bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS1}		50	µA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(on)}1$			
2N7465T3, U3					1.39	Ω
2N7466T3, U3					1.77	Ω
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, condition A, pulsed (see 4.5.1), I_D = I_{D1}	$r_{DS(on)}2$			
2N7465T3, U3					1.52	Ω
2N7466T3, U3					1.90	Ω
Forward voltage	4011	Condition A, I_D = I_{D1}, V_{GS} = 0	V_{SD}		1.2	V

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 3						
High-temperature operation:		$T_C = T_J = +125°C$				
Gate reverse current	3411	V_{GS} = +20 V dc and -20 V dc, bias condition C, V_{DS} = 0	I_{GSS2}		±200	nA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 100 percent of rated V_{DS}	I_{DSS2}		1.0	mA dc
Drain current	3413	V_{GS} = 0, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS3}		0.25	mA dc
Static drain to source on-state resistance	3421	V_{GS} = 12 V dc, bias condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7465T3, U3					2.64	Ω
2N7466T3, U3					3.76	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)2}$	1.5		V dc
Low-temperature operation:		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = 1 mA dc	$V_{GS(TH)3}$		5.5	V dc
Subgroup 4						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = 15 V (see 4.5.1)	g_{FS}			
2N7465T3, U3				0.5		mhos
2N7466T3, U3				0.4		mhos
Switching time test	3472	$I_D = I_{D1}$, V_{GS}= 12 V dc, R_G = 7.5 Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$			
2N7465T3, U3					25	ns
2N7466T3, U3					25	ns
Rise time			t_r			
2N7465T3, U3					75	ns
2N7466T3, U3					65	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Turn-off delay time			$t_{d(off)}$			
2N7465T3, U3					58	ns
2N7466T3, U3					60	ns
Fall time			t_f			
2N7465T3, U3					58	ns
2N7466T3, U3					63	ns
Subgroup 5						
Safe operating area test (high voltage)	3474	See figures 5 and 6; t_p = 10 ms, V_{DS} = 200 V				
Electrical measurements		See table I, subgroup 2 herein.				
Subgroup 6						
Not applicable						
Subgroup 7						
Gate charge	3471	Condition B	$Q_{G(on)}$			
2N7465T3, U3					31	nC
2N7466T3, U3					30	nC
Gate to source charge			Q_{GS}			nC
2N7465T3, U3					8.5	nC
2N7466T3, U3					8	nC
Gate to drain charge			Q_{GD}			
2N7465T3, U3					20	nC
2N7466T3, U3					18	nC
Reverse recovery time	3473	Condition A, di/dt ≤ 100A/µs, V_{DD} ≤ 50 V, I_D = I_{D1}	t_{rr}			
2N7465T3, U3					350	ns
2N7466T3, U3					400	ns

1/ For sampling plan, see MIL-PRF-19500.
2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 2 and 3 (JANTXV).
Group B, subgroups 3 and 4 (JANS).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Preirradiation limits		Postirradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
Subgroup 1 Not applicable								
Subgroup 2		T_C = +25°C						
* Steady-state total dose irradiation (V_{GS} bias) 4/	1019	Condition A, V_{GS} = 12V dc V_{DS} = 0						
* Steady-state total dose irradiation (V_{DS} bias) 4/	1019	Condition A, V_{GS} = 0 V V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)						
End-point electricals:								
Breakdown voltage, drain to source	3407	V_{GS} = 0 V I_D = 1 mA bias condition C	$V_{(BR)DSS}$					
2N7465T3, U3				400		400		V dc
2N7466T3, U3				500		500		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$					
2N7465T3, U3				2.5	4.5	2.0	4.5	V dc
2N7466T3, U3				2.5	4.5	2.0	4.5	V dc
Gate reverse current	3411	V_{GS} = 20 V dc V_{DS} = 0 bias condition C	I_{GSSF1}		100		100	nA dc
Gate reverse current	3411	V_{GS} = -20 V dc V_{DS} = 0 bias condition C	I_{GSSR1}		-100		-100	nA dc
Drain current	3413	V_{GS} = 0 V bias condition C V_{DS} = 80 percent of rated V_{DS} (pre-irradiation)	I_{DSS1}		50		50	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

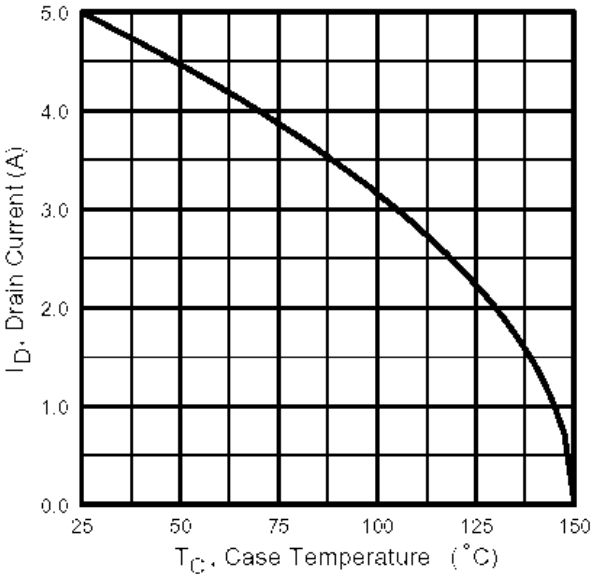
Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Preirradiation limits		Postirradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
Static drain to source on-state voltage	3405	V_{GS} = 12 V condition A pulsed (see 4.5.1) $I_D = I_{D2}$	V_{DSon1}					
2N7465T3, U3					4.726		4.726	V dc
2N7466T3, U3					4.956		4.956	V dc
Forward voltage source to drain diode	4011	Condition A, V_{GS} = 0 $I_D = I_{D1}$	V_{SD}		1.2		1.2	V dc

1/ For sampling plan, see MIL-PRF-19500.
2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ Separate samples shall be pulled for each bias.

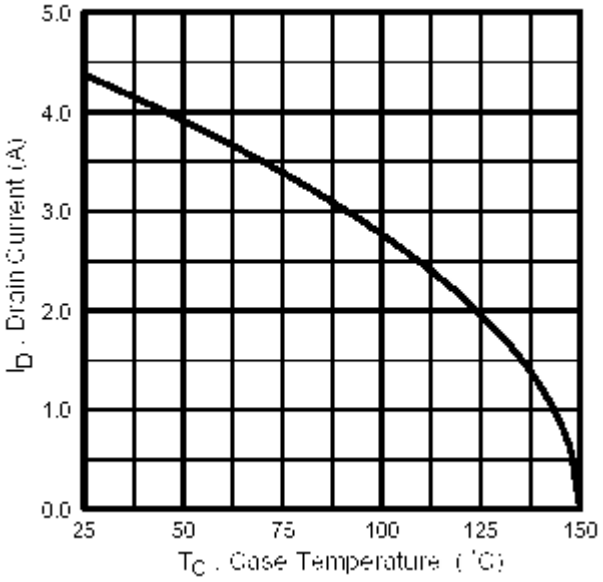
TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Thermal shock (temperature cycling)	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 5			3 devices c = 0
Barometric pressure (reduced) (all devices)	1001	V_{DS} = rated $V_{(BR)DSS}$, $I_{(ISO)}$ < 0.25 mA	
Subgroup 10			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
Subgroup 11			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

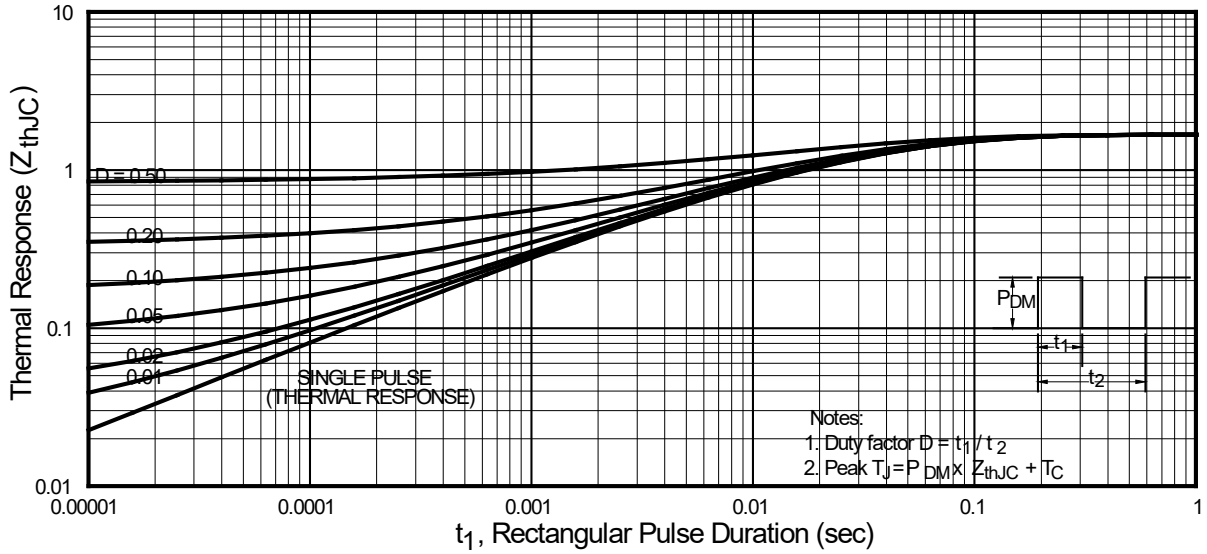


2N7465T3, and 2N7465U3



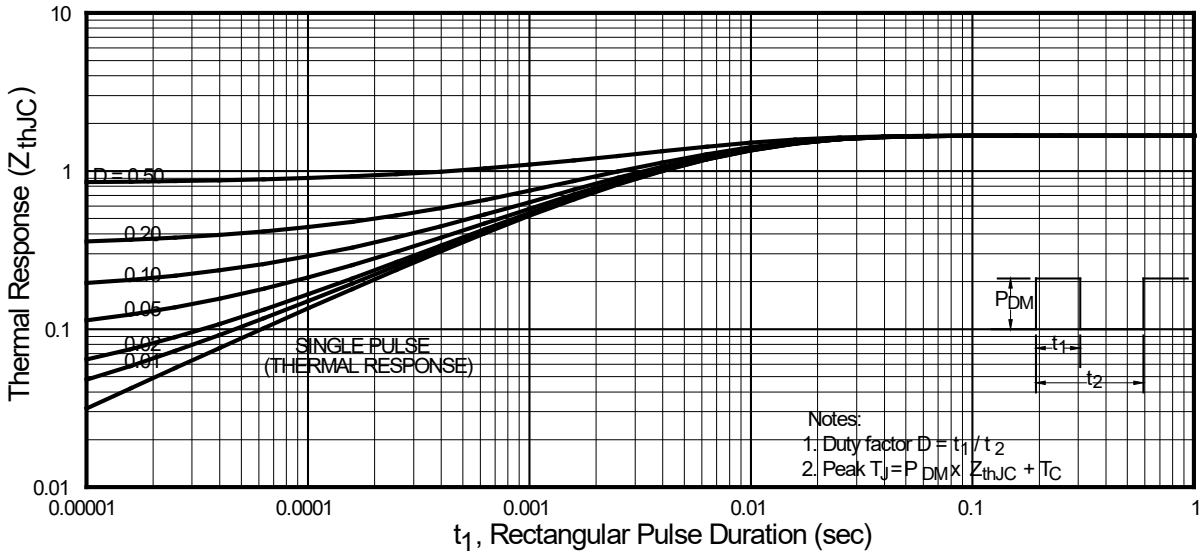
2N7466T3, and 2N7466U3

FIGURE 3. Maximum drain current and case temperature graphs.



2N7465T3 and 2N7466T3

FIGURE 4. Thermal impedance curves.



2N7465U3, and 2N7466U3

FIGURE 4. Thermal impedance curves – Continued.

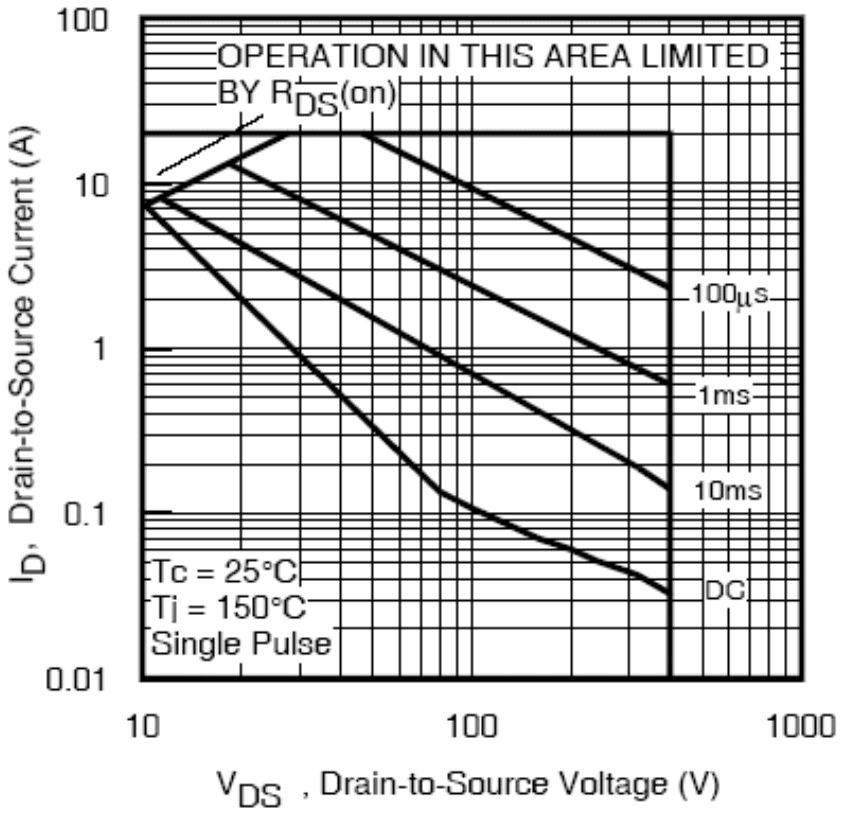


FIGURE 5. Safe operating area graph (2N7465T3, and 2N7465U3).

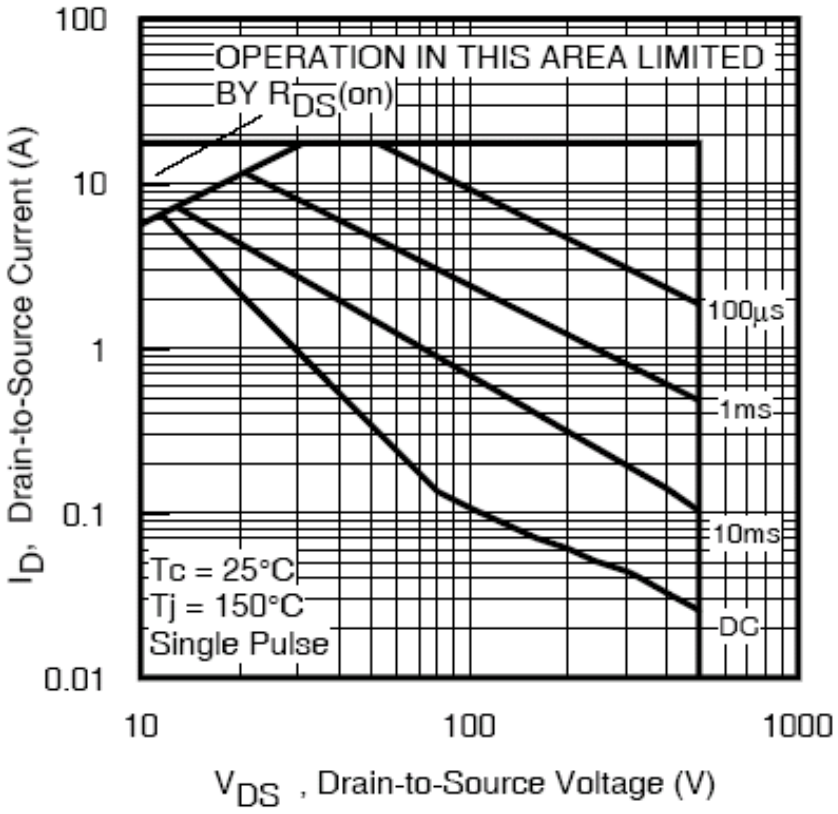


FIGURE 6. Safe operating area graph (2N7466T3, and 2N7466U3).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

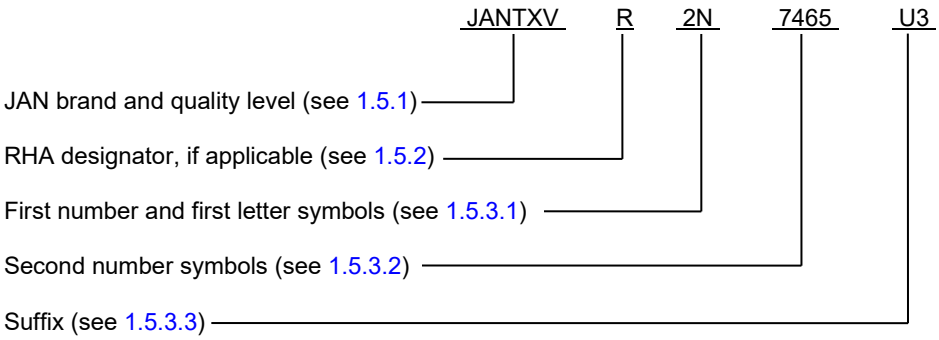
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract or order.

f. If SEE testing data is desired, it should be specified in the contract or order.

g. If specific SEE characterization conditions are desired (see section 6.7 and table IV), manufacturer's CAGE code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JANTXV#2N7465T3	JANS#2N7465T3
JANTXV#2N7465U3	JANS#2N7465U3
JANTXV#2N7466T3	JANS#2N7466T3
JANTXV#2N7466U3	JANS#2N7466U3

(1) The number sign (#) represent one RHA designator available (R). The PIN is also available without a RHA designator.

6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN	
	TO-257AA	SMD.5
2N7465T3, U3 2N7466T3, U3	IRHY7330CMSE IRHY7430CMSE	IRHNJ7330SE IRHNJ7430SE

6.7 Application data.

* 6.7.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE (SEB and SEGR) conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

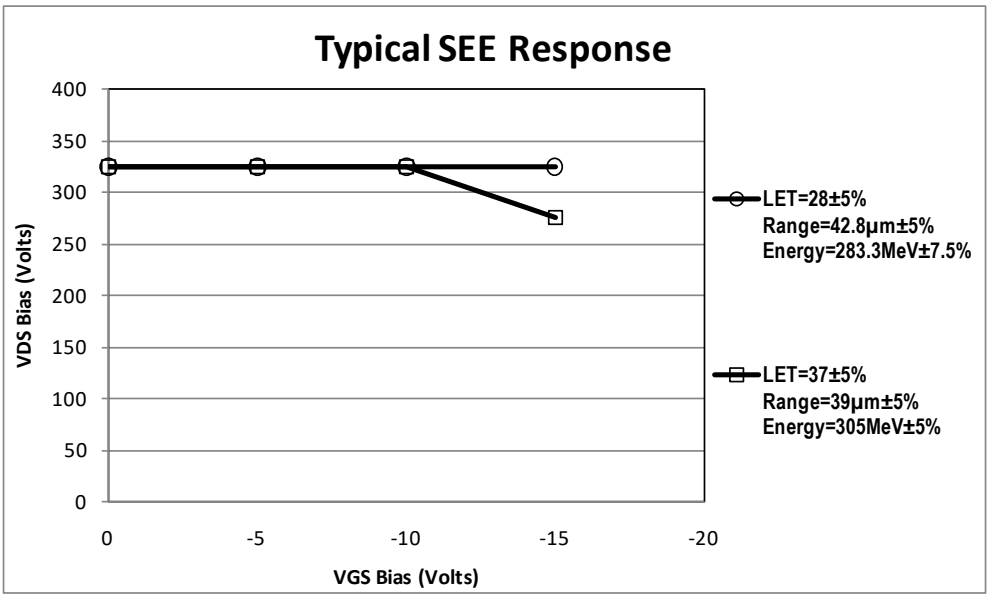
TABLE IV. Manufacturers characterization conditions.

Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of February 1998 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 7.	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
	SEE irradiation:		Fluence = 3E5 ±20 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25º ±5 °C	
	2N7465T3 & 2N7465U3		Surface LET = 28 MeV-cm^2/mg ±5.0 %, range = 42.8 µm ±7.5%, energy = 283.3 MeV ±7.5% In-situ bias conditions: V_{DS} = 325 V and V_{GS} = -15 V (typical 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7466T3 & 2N7466U3		In-situ bias conditions: V_{DS} = 375 V and V_{GS} = -20 V (nominal 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7465T3 & 2N7465U3		Surface LET = 37 MeV-cm^2/mg ±5.0 %, range = 39 µm ±7.5%, energy = 305 MeV ±7.5% In-situ bias conditions: V_{DS} = 325 V and V_{GS} = -10 V V_{DS} = 275 V and V_{GS} = -15 V (nominal 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7466T3 & 2N7466U3		In-situ bias conditions: V_{DS} = 350 V and V_{GS} = -10 V V_{DS} = 325 V and V_{GS} = -15 V V_{DS} = 300 V and V_{GS} = -20 V (typical 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers should provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

* 2/ Manufacturer performed heavy ion SEE(SEB/SEGR) test at Brookhaven National Lab Accelerator for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. No single event burnout (SEB) and Single event gate rupture (SEGR) were observed to surface LET as stated above table IV and safe operating area (see figures 5 and 6). Limits are characterized at initial qualification and after any design or process changes which may affect the SEE(SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.

2N7465T3, 2N7465U3



2N7466T3, 2N7466U3

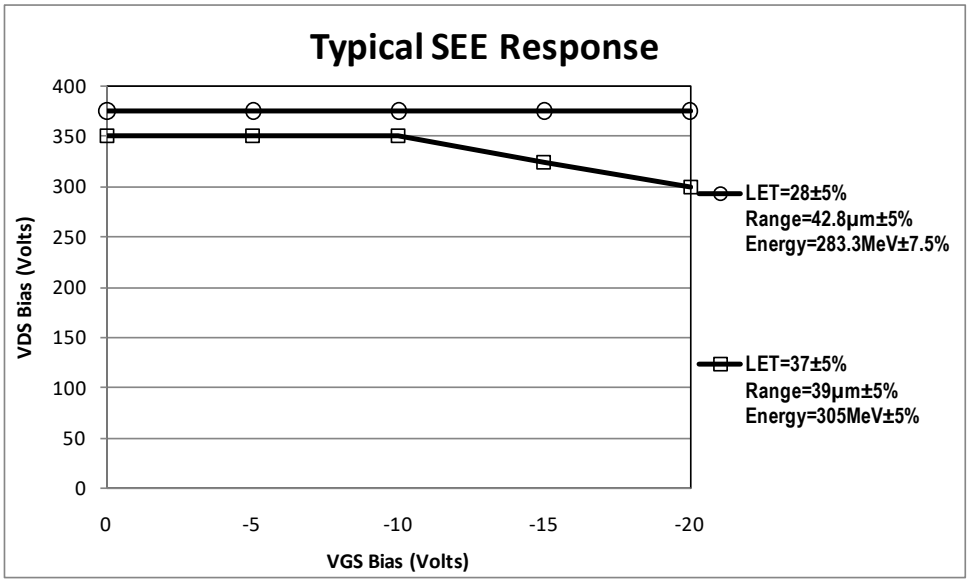


FIGURE 7. SEE safe operation area graph.

6.8 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

* 6.7 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Review activity:
* Air Force - 170

Preparing activity:
DLA - CC

(Project 5961-2021-061)

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.