

The documentation and process conversion measures necessary to comply with this revision shall be completed by 24 April 2017.

INCH-POUND

MIL-PRF-19500/661F  
 24 January 2017  
 SUPERSEDING  
 MIL-PRF-19500/661E  
 25 February 2014

PERFORMANCE SPECIFICATION SHEET

\* TRANSISTOR, FIELD EFFECT RADIATION HARDENED  
 N-CHANNEL, SILICON, TYPES 2N7444, 2N7434, 2N7391, AND 2N7392,  
 JANTXVR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an N-channel, enhancement-mode, MOSFET, radiation hardened, power transistor intended for use in high density power switching applications. Two levels of product assurance (JANTXV and JANS) are provided for each device, with avalanche energy maximum rating (E<sub>AS</sub>) and maximum avalanche current (I<sub>AS</sub>). See 6.7 for JANHC and JANKC die versions.

\* 1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with [figure 1](#) and a modified (tabless) TO-254AA in accordance with [figure 2](#) for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet [MIL-PRF-19500/657](#).

\* 1.3 Maximum ratings. Unless otherwise specified, T<sub>C</sub> = +25°C.

Type	P <sub>T</sub> (1)	P <sub>T</sub> T <sub>A</sub> = +25°C	R <sub>θJC</sub> (2)	V <sub>DS</sub>	V <sub>DG</sub>	V <sub>GS</sub>	I <sub>D1</sub> (3) (4)	I <sub>D2</sub> (3) (4) T <sub>C</sub> = +100°C	I <sub>S</sub>	I <sub>DM</sub> (5)	T <sub>J</sub> and T <sub>STG</sub>	V <sub>ISO</sub> 70,000 ft altitude
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A(pk)	°C	V dc
2N7444	250	3.0	0.5	200	200	±20	35.0	25.0	35.0	140	-55	NA
2N7434	250	3.0	0.5	250	250	±20	31.0	19.0	31.0	124	to	250
2N7391, D4	250	3.0	0.5	400	400	±20	22.0	14.0	22.0	88	+150	400
2N7392	250	3.0	0.5	500	500	±20	18.0	11.7	18.0	72		500

- (1) Derate linearly 2.0 W/°C for T<sub>C</sub> > +25°C.
- (2) See [figure 3](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I<sub>D</sub> limit. I<sub>D</sub> is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 4](#), maximum drain current graphs.
- (5) I<sub>DM</sub> = 4 x I<sub>D1</sub> as calculated in note 3.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.4 Primary electrical characteristics at  $T_c = +25^\circ\text{C}$ .

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0$ mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0$ mA dc	Max $I_{DSS1}$ $V_{GS} = 0$ $V_{DS} = 80$ percent of rated $V_{DS}$	Max $r_{DS(ON)}$ (1) $V_{GS} = 12$ V dc		$E_{AS}$ at $I_{D1}$	$I_{AS}$	
				$T_J = +25^\circ\text{C}$ at $I_{D2}$	$T_J = +150^\circ\text{C}$ at $I_{D2}$			
	<u>V dc</u>	<u>V dc</u>		<u><math>\mu\text{A dc}</math></u>	<u>ohm</u>	<u>ohm</u>	<u>mJ</u>	<u>A</u>
		Min	Max					
2N7444	200	2.5	4.5	50	0.070	0.150	500	35.0
2N7434	250	2.5	4.5	50	0.110	0.250	500	31.0
2N7391, D4	400	2.5	4.5	50	0.200	0.450	500	22.0
2N7392	500	2.5	4.5	50	0.320	0.700	500	18.0

(1) Pulsed (see 4.5.1).

\* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

\* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

\* 1.5.2 Radiation hardness assurance (RHA) designator. The only RHA level designator applicable for this specification sheet is "R".

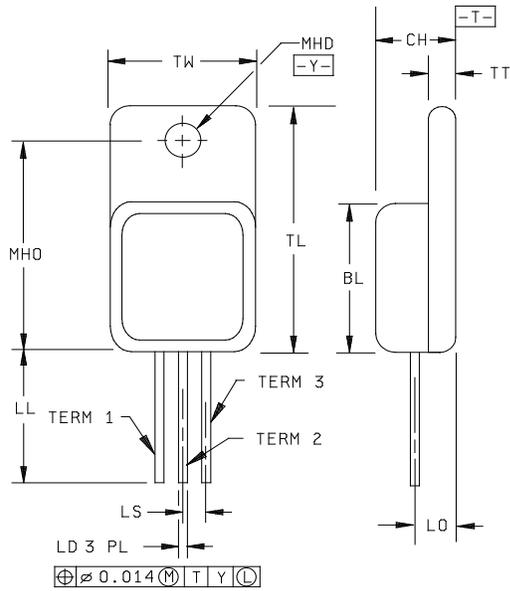
\* 1.5.3 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

\* 1.5.3.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

\* 1.5.3.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "7392", "7391", "7434" and "7444".

\* 1.5.3.3 Suffix letters. No suffix letters are used on devices that are packaged in the TO-254AA package of figure 1. The suffix letters "D4" are used on devices that are packaged in the tabless TO-254AA package of figure 2.

\* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

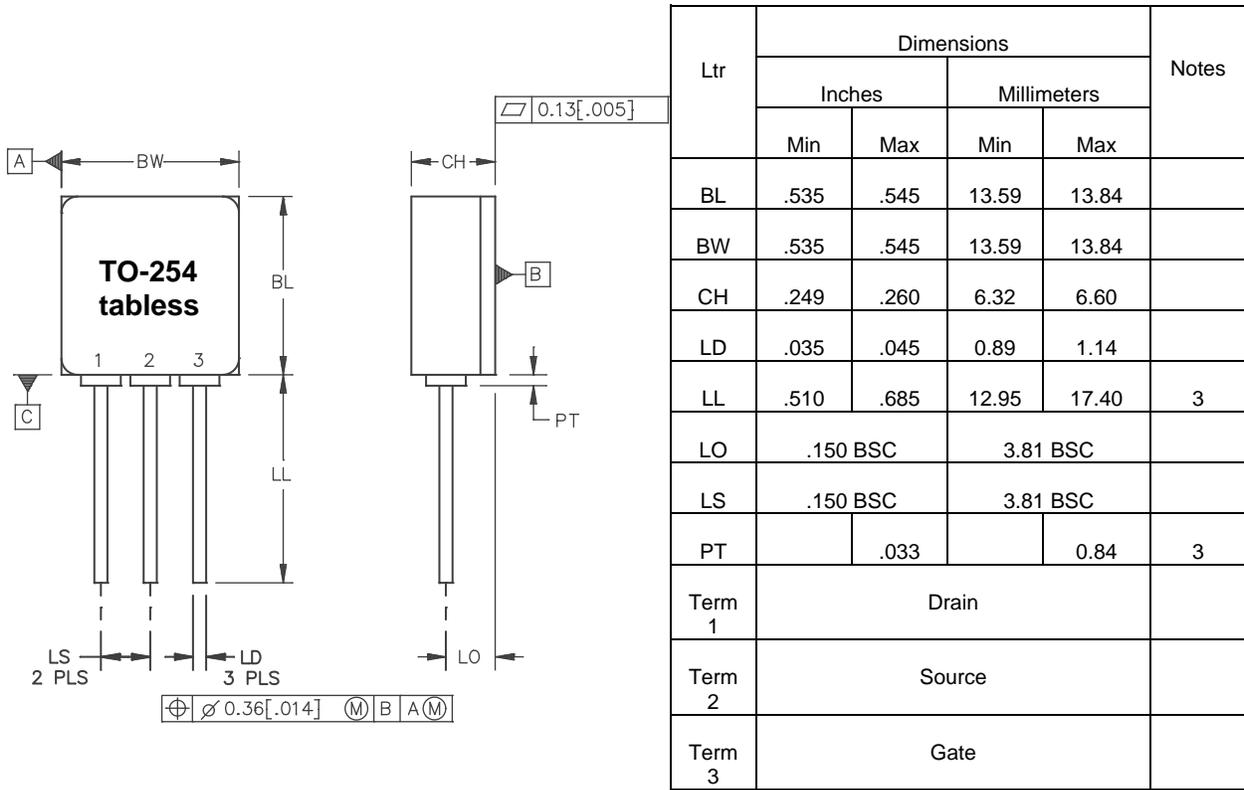


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
BL	.535	.545	13.59	13.84	
CH	.249	.260	6.32	6.60	
LD	.035	.045	0.89	1.14	
LL	.510	.570	12.95	14.48	3
LO	.150 BSC		3.81 BSC		
LS	.150 BSC		3.81 BSC		
MHD	.139	.149	3.53	3.78	
MHO	.665	.685	16.89	17.40	
TL	.790	.800	20.07	20.32	4
TT	.040	.050	1.02	1.27	
TW	.535	.545	13.59	13.84	4
Term 1	Drain				
Term 2	Source				
Term 3	Gate				

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Protrusion thickness of ceramic eyelets included in dimension LL.
4. All terminals are isolated from case.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 1. Physical dimensions for TO-254AA.



- NOTES:
1. Dimensions are in inches.
  2. Millimeters are given for general information only.
  3. Protrusion thickness (PT) of ceramic eyelets included in dimension LL.
  4. All terminals are isolated from case.
  5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

\* FIGURE 2. Physical dimensions for TO-254AA tabless package.

## 2. APPLICABLE DOCUMENTS

\* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

IAS.....Rated avalanche current, nonrepetitive  
nC .....nano coulomb.

\* 3.4 Interface physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and [figure 1](#) and [figure 2](#) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent AL<sub>2</sub>O<sub>3</sub> (ceramic). Examples of such construction techniques are metallized ceramic eyelets.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Internal construction. Multiple chip construction is not permitted.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.6).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source,  $R \leq 100 \text{ k}\Omega$ , whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4 and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I, II, and III).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.2 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with table II. SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

\* 4.3 Screening (JANTXV and JANS levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV levels
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Unclamped inductive switching, method 3470 of MIL-STD-750 (see 4.3.2), optional	Unclamped inductive switching, method 3470 of MIL-STD-750 (see 4.3.2), optional
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.3)	Method 3161 of MIL-STD-750 (see 4.3.3)
9	I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , Subgroup 2 of table I herein.	Subgroup 2 of table I herein.
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , r <sub>DS(on)</sub> , V <sub>GS(th)1</sub> Subgroup 2 of table I herein.  $\Delta I_{GSSF1} = +20 \text{ nA dc or } +100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = -20 \text{ nA dc or } -100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 10 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$	I <sub>GSSF1</sub> , I <sub>GSSR1</sub> , I <sub>DSS1</sub> , r <sub>DS(on)</sub> , V <sub>GS(th)1</sub> Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein.  $\Delta I_{GSSF1} = +20 \text{ nA dc or } +100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = -20 \text{ nA dc or } -100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 10 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(on)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(th)1} = \pm 20 \text{ percent of initial value.}$	Subgroup 2 of table I herein.  $\Delta I_{GSSF1} = +20 \text{ nA dc or } -100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{GSSR1} = +20 \text{ nA dc or } -100 \text{ percent of initial value, whichever is greater.}$ $\Delta I_{DSS1} = \pm 10 \text{ } \mu\text{A dc or } \pm 100 \text{ percent of initial value, whichever is greater.}$ $\Delta r_{DS(on)1} = \pm 20 \text{ percent of initial value.}$ $\Delta V_{GS(th)1} = \pm 20 \text{ percent of initial value.}$
17	Method 1081 of MIL-STD-750 (see 4.3.4). End-points: Subgroup 2 of table I herein.	Method 1081 of MIL-STD-750 (see 4.3.4). End-points: Subgroup 2 of table I herein.

- (1) At the end of the test program, I<sub>GSSF1</sub>, I<sub>GSSR1</sub>, and I<sub>DSS1</sub> are measured.
- \* (2) An out-of-family program to characterize I<sub>GSSF1</sub>, I<sub>GSSR1</sub>, I<sub>DSS1</sub>, V<sub>GS(th)1</sub>, and r<sub>DS(ON)1</sub> shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply  $V_{GS} = 30$  V minimum for  $t = 250$   $\mu$ s minimum.

4.3.2 Single pulse avalanche energy  $E_{AS}$ .

- a. Peak current ( $I_{AS}$ ) .....  $I_{AS(max)}$ .
- b. Peak gate voltage ( $V_{GS}$ ) ..... 12 V.
- c. Gate to source resistor ( $R_{GS}$ ) .....  $25\Omega \leq R_{GS} \leq 200\Omega$ .
- d. Initial case temperature ( $T_C$ ) .....  $+25^\circ\text{C}, +10^\circ\text{C}, -5^\circ\text{C}$ .
- e. Inductance (L) ..... 
$$L = \left[ \frac{2 E_{AR}}{(I_{DI})^2} \right] \left[ \frac{V_{BR} - V_{DD}}{V_{BR}} \right] \text{ nH minimum}$$
- f. Number of pulses to be applied ..... 1 pulse minimum.
- g. Supply voltage ( $V_{DD}$ ) ..... 50 V.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$ , (and  $V_H$  where appropriate). Measurement delay time ( $t_{MD}$ ) = 70  $\mu$ s max. See [table III](#), group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

- a. Magnitude of test voltage.....900 V dc.
- b. Duration of application of test voltage.....15 seconds (min).
- c. Points of application of test voltage.....All leads to case (bunch connection).
- d. Method of connection.....Mechanical.
- e. Kilovolt-ampere rating of high voltage source.....1,200 V/1.0 mA (min).
- f. Maximum leakage current.....1.0 mA.
- g. Voltage ramp up time.....500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of [MIL-PRF-19500](#) and [table I](#) herein. End-point electrical measurements shall be in accordance with [table I](#), subgroup 2 herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIA (JANS) and table VIB (JANTXV) of [MIL-PRF-19500](#), and herein.

\* 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2075	See 3.4.2.
B3	2077	SEM qualification may be performed anytime prior to lot formation.
B4	1042	The heating cycle shall be 30 seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} = \text{rated}$ , $T_A = +175^\circ\text{C}$ , $t = 24$ hours minimum; or, $T_A = +150^\circ\text{C}$ , $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} = \text{rated}$ , $T_A = +175^\circ\text{C}$ , $t = 120$ hours minimum; or, $T_A = +150^\circ\text{C}$ , $t = 240$ hours minimum.
B5	2037	Bond strength; test condition D.

\* 4.4.2.2 Quality level JANTXV, table E-VIB of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	The heating cycle shall be 30 seconds minimum.
B3	2037	Test condition D; All internal bond wires for each device shall be pulled separately.
B4	2075	See 3.4.2.
B5 and B6		Not applicable.

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A; weight = 10 pounds (4.54 Kg); $t = 15$ s.
C5	3161	See 4.3.3, $R_{\theta JC(\text{max})} = 0.50^\circ\text{C/W}$
C6	1042	The heating cycle shall be 30 seconds minimum.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.\* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in of MIL-STD-750.

\*

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage, drain to source	3407	$V_{GS} = 0 \text{ V}$ , $I_D = 1 \text{ mA dc}$ , bias condition C	$V_{(BR)DSS}$			
2N7444				200		V dc
2N7434				250		V dc
2N7391, D4				400		V dc
2N7392				500		V dc
Gate to source voltage threshold	3403	$V_{DS} \geq V_{GS}$ , $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	2.5	4.5	V dc
Gate current	3411	$V_{GS} = +20 \text{ V dc}$ , bias condition C, $V_{DS} = 0$	$I_{GSSF1}$		+ 100	nA dc
Gate current	3411	$V_{GS} = -20 \text{ V dc}$ , bias condition C, $V_{DS} = 0$	$I_{GSSR1}$		- 100	nA dc
Drain current	3413	$V_{GS} = 0 \text{ V dc}$ , bias condition C, $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS1}$		50	μA dc
Static drain to source on-state resistance	3421	$V_{GS} = 12 \text{ V dc}$ , condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)1}$			
2N7444					0.070	ohm
2N7434					0.110	ohm
2N7391, D4					0.200	ohm
2N7392					0.320	ohm
Static drain to source on-state resistance	3421	$V_{GS} = 12 \text{ V dc}$ , condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$r_{DS(on)2}$			
2N7444					0.075	ohm
2N7434					0.123	ohm
2N7391, D4					0.210	ohm
2N7392					0.360	ohm
Forward voltage	4011	Condition A, pulsed (see 4.5.1), $I_D = I_{D1}$ , $V_{GS} = 0 \text{ V dc}$	$V_{SD}$			
2N7444					1.4	V dc
2N7434					1.4	V dc
2N7391, D4					1.4	V dc
2N7392					1.8	V dc

See footnotes at end of table.

\*

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:						
Gate current	3411	$T_C = T_J = +125^\circ\text{C}$ $V_{GS} = +20$ and $-20$ V dc, bias condition C, $V_{DS} = 0$	$I_{GSS2}$		$\pm 200$	nA dc
Drain current	3413	$V_{GS} = 0$ V; bias condition C, $V_{DS} = 80$ percent of rated $V_{DS}$	$I_{DSS2}$		0.25	mA dc
Static drain to source on-state resistance	3421	Condition A, $V_{GS} = 12$ V dc, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7444					0.140	ohm
2N7434					0.220	ohm
2N7391, D4					0.390	ohm
2N7392					0.590	ohm
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 1$ mA dc	$V_{GS(TH)2}$	1.5		V dc
Low temperature operation:						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$ , $I_D = 1$ mA dc	$V_{GS(TH)3}$		5.5	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = \text{rated } I_{D2}$ , $V_{DD} = 15$ V, (see 4.5.1)	$g_{FS}$			
2N7444				12		S
2N7434				10		S
2N7391, D4				6		S
2N7392				6		S
Switching time test	3472	$I_D = I_{D1}$ , $V_{GS} = 12$ V dc, $R_G = 2.35\Omega$ , $V_{DD} = 50$ percent of rated $V_{DS}$				
Turn-on delay time			$t_{d(on)}$			
2N7444					35	ns
2N7434					30	ns
2N7391, D4					28	ns
2N7392					29	ns

See footnotes at end of table.

\*

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued						
Rise time			$t_r$			
2N7444					200	ns
2N7434					130	ns
2N7391, D4					97	ns
2N7392					93	ns
Turn-off delay time			$t_{d(off)}$			
2N7444					150	ns
2N7434					100	ns
2N7391, D4					120	ns
2N7392					90	ns
Fall time			$t_f$			
2N7444					150	ns
2N7434					90	ns
2N7391, D4					72	ns
2N7392					59	ns
<u>Subgroup 5</u>	3474					
Safe operating area test (high voltage)		See <a href="#">figure 4</a> , $t_p = 10$ ms minimum, $V_{DS} = 80$ percent of maximum rated $V_{DS}$ , ( $V_{DS} \leq 200$ )				
Electrical measurements		See <a href="#">table I</a> , subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$			
2N7444					260	nC
2N7434					210	nC
2N7391, D4					185	nC
2N7392					180	nC

See footnotes at end of table.

\*

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 7</u> - Continued						
Gate to source charge 2N7444 2N7434 2N7391, D4 2N7392			$Q_{gs}$		80 50 35 30	nC nC nC nC
Gate to drain charge 2N7444 2N7434 2N7391, D4 2N7392			$Q_{gd}$		150 110 100 95	nC nC nC nC
Reverse recovery time  2N7444 2N7434 2N7391, D4 2N7392	3473	$di/dt \leq 100 \text{ A}/\mu\text{s}$ , $V_{DD} \leq 50 \text{ V}$ , $I_D = I_{D1}$	$t_{rr}$		650 700 720 800	ns ns ns ns

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:  
 Group B, subgroups 3 and 4 (JANS).  
 Group B, subgroups 2 and 3 (JANTXV).  
 Group C, subgroups 2 and 6.  
 Group E, subgroup 1.

\*

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Preirradiation limits		Postirradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
<u>Subgroup 1</u>								
Not applicable								
<u>Subgroup 2</u>		T <sub>C</sub> = +25°C						
Steady-state total dose irradiation (V <sub>GS</sub> bias) 4/	1019	V <sub>GS</sub> = 12V, V <sub>DS</sub> = 0						
Steady-state total dose irradiation (V <sub>DS</sub> bias) 4/	1019	V <sub>GS</sub> = 0, V <sub>DS</sub> = 80 percent of rated V <sub>DS</sub> (pre-irradiation)						
End-point electricals								
Breakdown voltage, drain to source	3407	Bias condition C, V <sub>GS</sub> = 0, I <sub>D</sub> = 1 mA	V <sub>(BR)DSS</sub>					
2N7444				200		200		V dc
2N7434				250		250		V dc
2N7391, D4				400		400		V dc
2N7392				500		500		V dc
Gate to source voltage (threshold)	3403	V <sub>DS</sub> ≥ V <sub>GS</sub>	V <sub>GS(th)1</sub>					
2N7444				2.5	4.5	2.0	4.5	V dc
2N7434				2.5	4.5	2.0	4.5	V dc
2N7391, D4				2.5	4.5	2.0	4.5	V dc
2N7392				2.5	4.5	2.0	4.5	V dc
Gate current	3411	Bias condition C, V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0	I <sub>GSSF1</sub>		100		100	nA dc
Gate current	3411	Bias condition C, V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0	I <sub>GSSR1</sub>		-100		-100	nA dc
Drain current	3413	Bias condition C, V <sub>GS</sub> = 0, V <sub>DS</sub> = 80 percent of rated V <sub>DS</sub> (pre-irradiation)	I <sub>DSS1</sub>		50		50	μA dc

See footnotes at end of table.

\*

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Preirradiation limits		Postirradiation limits		Unit
	Method	Conditions		R		R		
				Min	Max	Min	Max	
<u>Subgroup 2</u> - Continued.								
Static drain to source on- state voltage	3405	Bias condition A, $V_{GS} = 12\text{ V}$ , pulsed (see 4.5.1), $I_D = I_{D2}$	$V_{DS(on)1}$					
2N7444					1.75		1.75	V dc
2N7434					2.09		2.09	V dc
2N7391, D4					2.80		2.80	V dc
2N7392					3.744		3.744	V dc
Forward voltage source to drain diode	4011	Condition A, $V_{GS} = 0$ , $I_D = I_{D1}$	$V_{SD}$					
2N7444					1.4		1.4	V dc
2N7434					1.4		1.4	V dc
2N7391, D4					1.4		1.4	V dc
2N7392					1.8		1.8	V dc

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071	As applicable.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2.	
<u>Subgroup 2</u> <sup>1/</sup>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2.	
Steady-state gate bias	1042	Condition B, 1,000 hours.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See <a href="#">MIL-PRF-19500</a> .	
<u>Subgroup 5</u>			3 devices c = 0
Barometric pressure	1001	Condition C, $V_{DS} = \text{rated}$ ; $I_{(ISO)} < 0.25 \text{ mA}$ , not required for 2N7444	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
<u>Subgroup 11</u>			
SEE <sup>2/</sup> <sup>3/</sup>	1080	See <a href="#">MIL-STD-750</a> method 1080 and <a href="#">6.2</a> .	3 devices

<sup>1/</sup> A separate sample may be pulled for each test condition.<sup>2/</sup> Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.<sup>3/</sup> Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

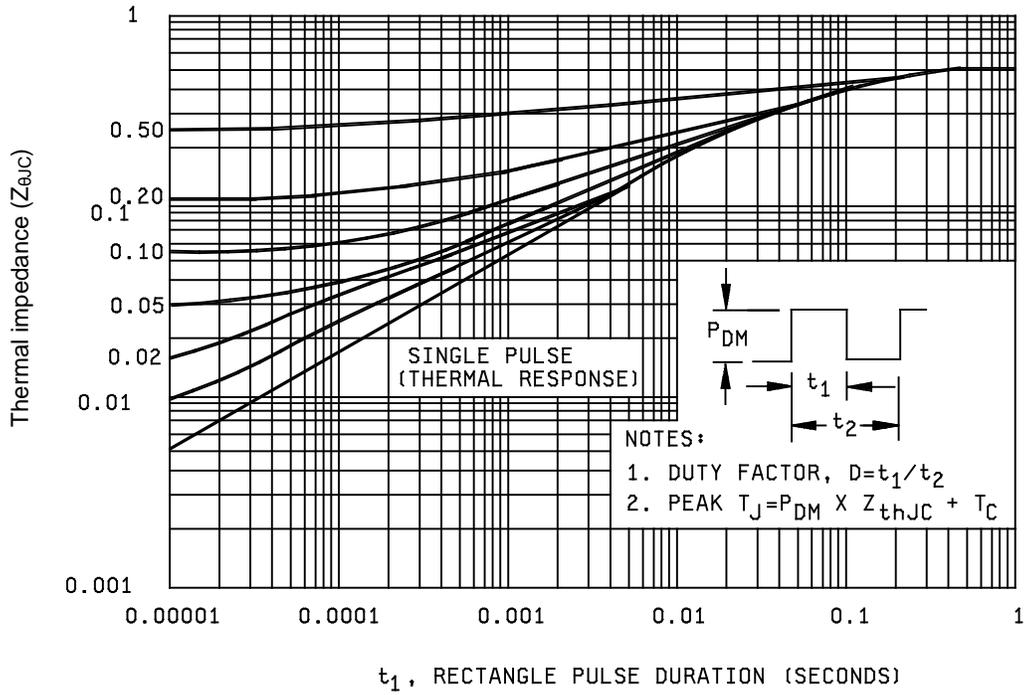
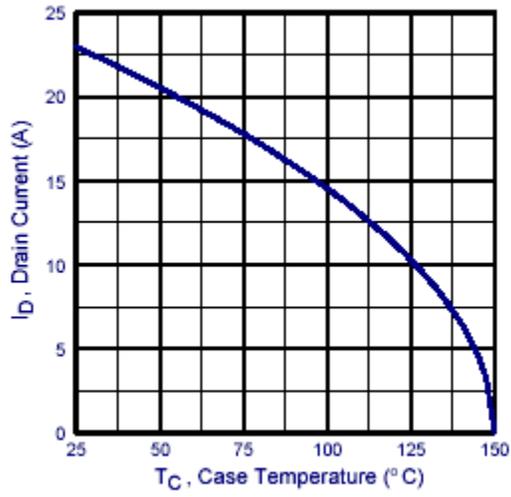
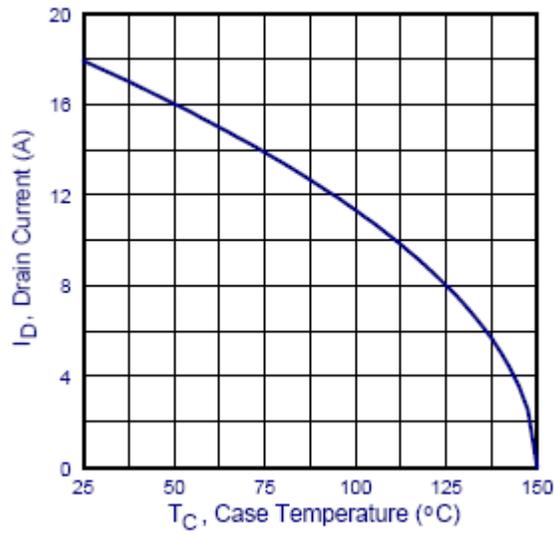


FIGURE 3. Thermal impedance curve.



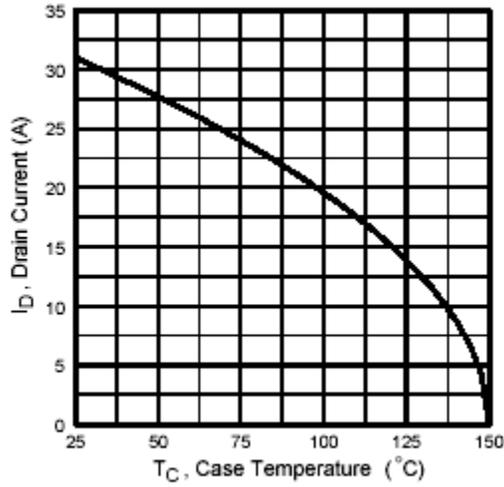
2N7391, 2N7391D4



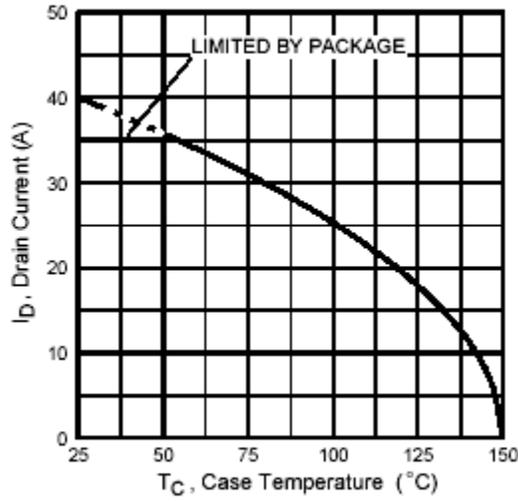
2N7392

\*

FIGURE 4. Maximum drain current versus case temperature graphs.



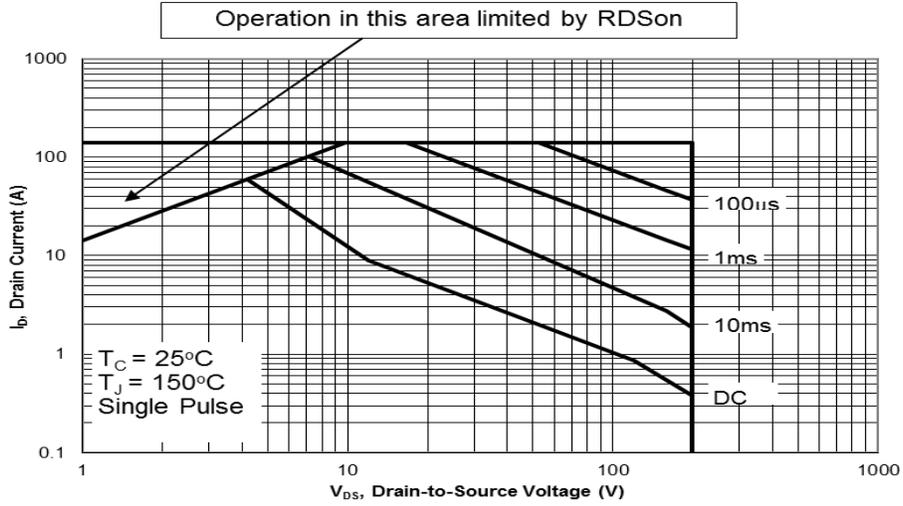
2N7434



2N7444

FIGURE 4. Maximum drain current versus case temperature graphs - Continued.

2N7444



2N7434

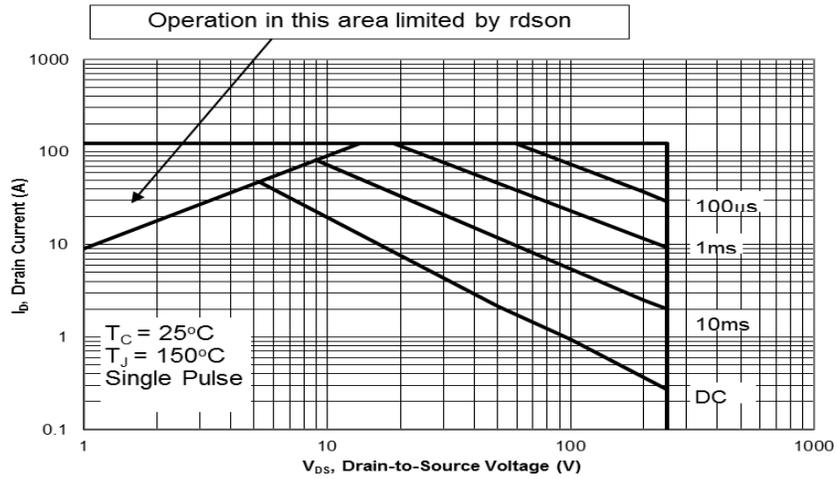
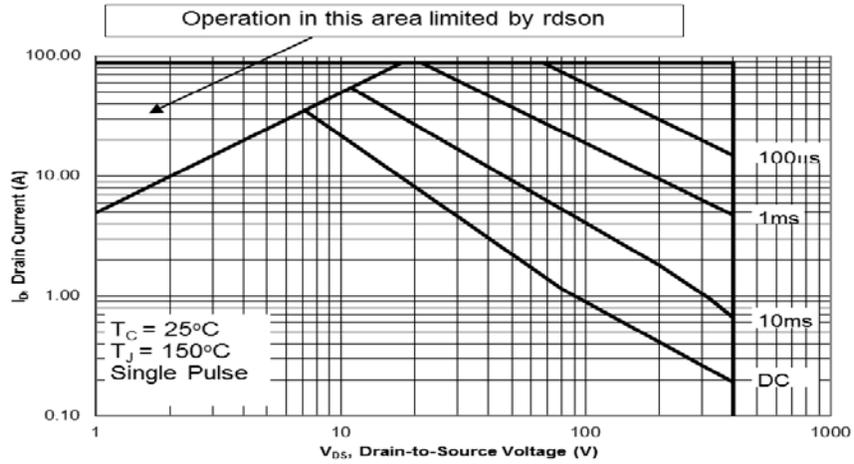


FIGURE 5. Safe operating area graph.

2N7391, 2N7391D4



2N7392

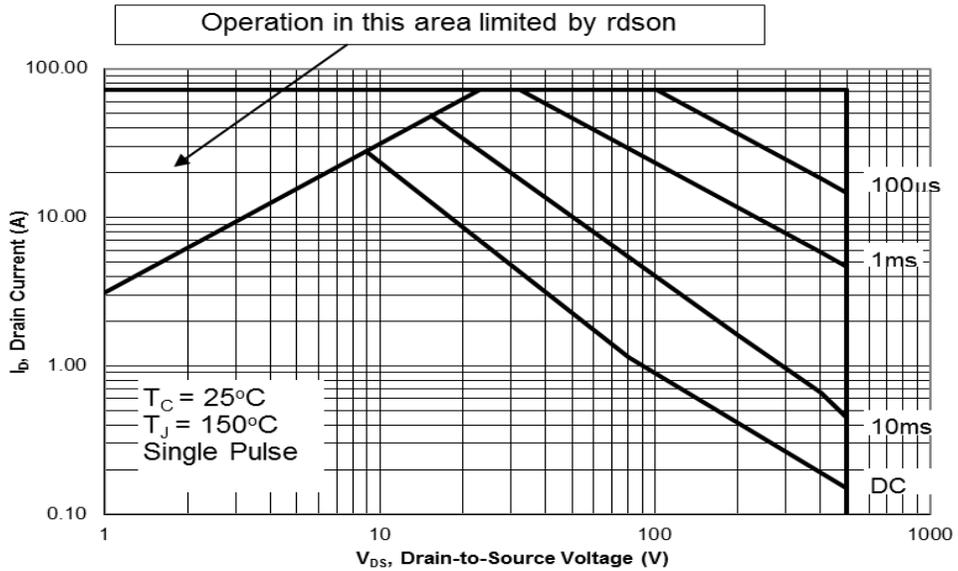


FIGURE 5. Safe operating area graph - Continued.

## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

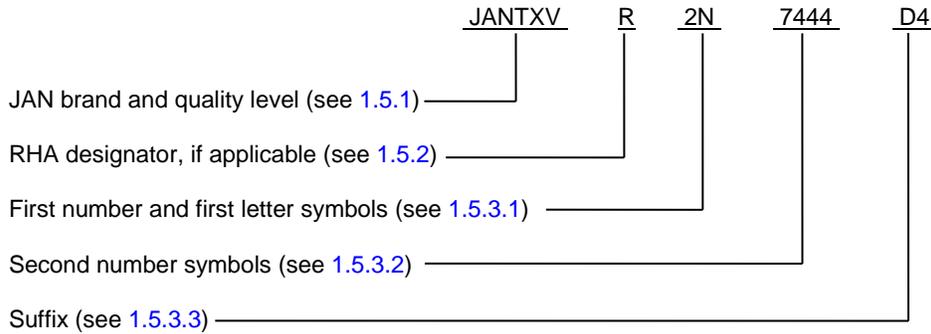
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

\* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- \* d. The complete PIN, see 1.5 and 6.5.
- e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



\* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7391	JANTXVR2N7391	JANS2N7391	JANSR2N7391
JANTXV2N7391D4	JANTXVR2N7391D4	JANS2N7391D4	JANSR2N7391D4
JANTXV2N7392	JANTXVR2N7392	JANS2N7392	JANSR2N7392
JANTXV2N7434	JANTXVR2N7434	JANS2N7434	JANSR2N7434
JANTXV2N7444	JANTXVR2N7444	JANS2N7444	JANSR2N7444

6.6 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types Military PIN	Commercial PIN
	TO-254AA
2N7444 2N7434 2N7391 2N7392	IRHM7260SE IRHM7264SE IRHM7360SE IRHM7460SE

6.7 JANHC and JANKC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/657](#).

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

\*

TABLE IV. Manufacturers characterization conditions.

Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of 2 February 1998 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 6	3 devices
	Electrical measurements		$I_{GSSF1}$ , $I_{GSSR1}$ , and $I_{DSS1}$ in accordance with table I, subgroup 2	
	SEE Irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm <sup>2</sup> Flux = $2E3$ to $2E4$ ions/cm <sup>2</sup> /sec, temperature = $25 \pm 5^\circ C$  Surface LET = 28 MeV-cm <sup>2</sup> /mg $\pm 5$ percent, Range = 42.8 microns $\pm 7.5$ percent, Energy = 283.3 MeV $\pm 7.5$ percent	
	2N7444		In situ bias conditions: $V_{DS} = 200$ V and $V_{GS} = -20$ V (typical 4.53 MeV/Neutron at Brookhaven National Lab Accelerometer)	
	2N7434		In situ bias conditions: $V_{DS} = 250$ V and $V_{GS} = -20$ V (typical 4.53 MeV/Neutron at Brookhaven National Lab Accelerometer)	
	2N7391, D4		In situ bias conditions: $V_{DS} = 325$ V and $V_{GS} = -15$ V (typical 4.53 MeV/Neutron at Brookhaven National Lab Accelerometer)	
	2N7392		In situ bias conditions: $V_{DS} = 375$ V and $V_{GS} = -20$ V (typical 4.53 MeV/Neutron at Brookhaven National Lab Accelerometer)  Surface LET = 37 MeV-cm <sup>2</sup> /mg $\pm 5$ percent, Range = 39 microns +/- 7.5 percent, Energy = 305 MeV +/- 7.5 percent	
	2N7444		In situ bias conditions: $V_{DS} = 200$ V and $V_{GS} = -10$ V $V_{DS} = 180$ V and $V_{GS} = -15$ V $V_{DS} = 140$ V and $V_{GS} = -20$ V (typical 3.77 MeV/Neutron at Brookhaven National Lab Accelerometer)	
	2N7434		In situ bias conditions: $V_{DS} = 250$ V and $V_{GS} = -10$ V $V_{DS} = 225$ V and $V_{GS} = -15$ V $V_{DS} = 210$ V and $V_{GS} = -20$ V (typical 3.77 MeV/Neutron at Brookhaven National Lab Accelerometer)	
	2N7391, D4		In situ bias conditions: $V_{DS} = 325$ V and $V_{GS} = -10$ V $V_{DS} = 275$ V and $V_{GS} = -15$ V (typical 3.77 MeV/Neutron at Brookhaven National Lab Accelerometer)	

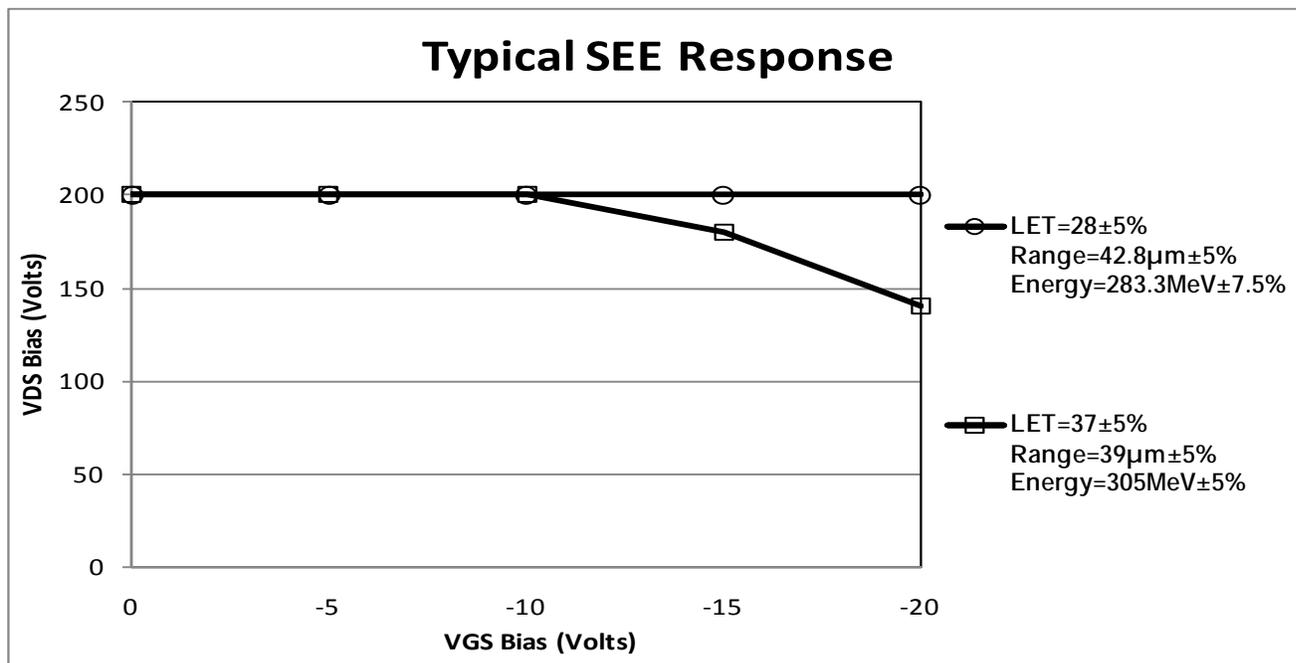
See footnotes at end of table.

\* TABLE IV. Manufacturers characterization conditions - Continued.

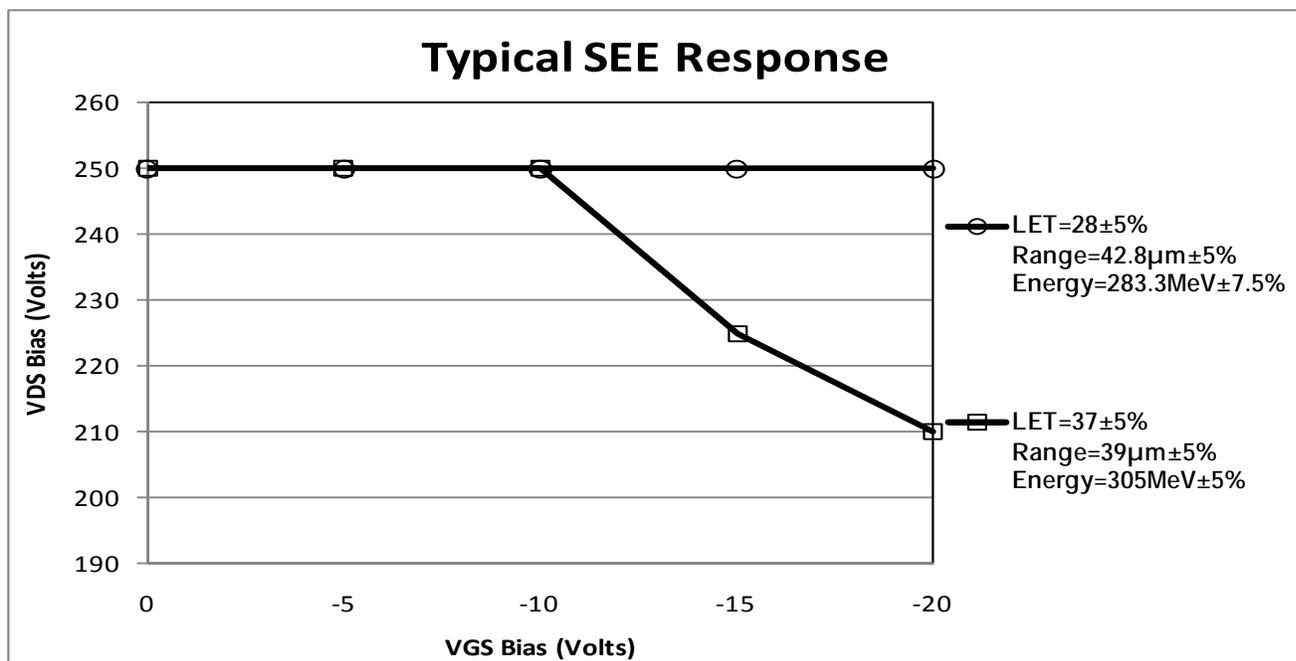
Manufactures CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
	2N7392  Electrical measurements <u>2/</u>		In situ bias conditions: $V_{DS} = 350\text{ V}$ and $V_{GS} = -10\text{ V}$ $V_{DS} = 325\text{ V}$ and $V_{GS} = -15\text{ V}$ $V_{DS} = 300\text{ V}$ and $V_{GS} = -20\text{ V}$ (typical 3.77 MeV/Neutron at Brookhaven National Lab Accelerometer)  $I_{GSSF1}$ , $I_{GSSR1}$ , and $I_{DSS1}$ in accordance with <a href="#">table 1</a> , subgroup 2.	
<div style="border: 1px solid black; padding: 5px; margin: 5px auto; width: 80%;">                         Upon qualification, all manufacturers will provide the verification test conditions to be added to this table.                     </div>				

1/  $I_{GSSF1}$ ,  $I_{GSSR1}$ , and  $I_{DSS1}$  was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with [table 1](#), subgroup 2, may be performed at the manufacturer's option.

2N7444



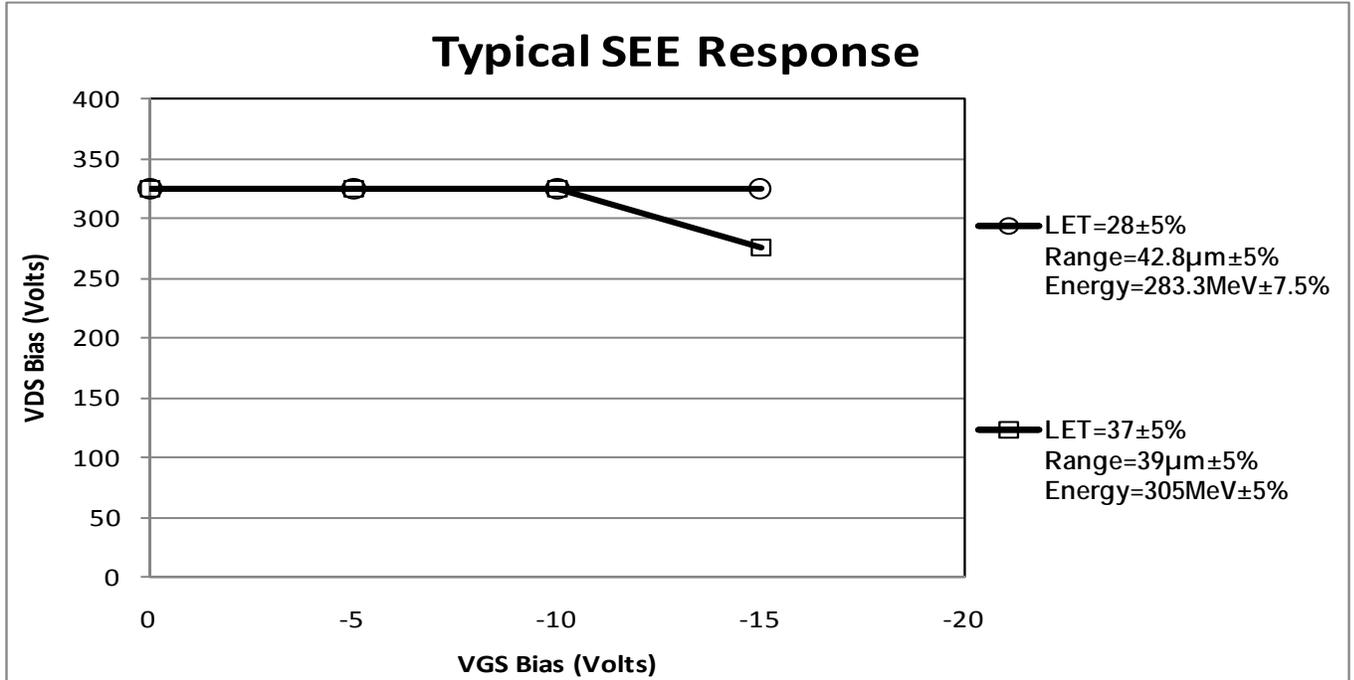
2N7434



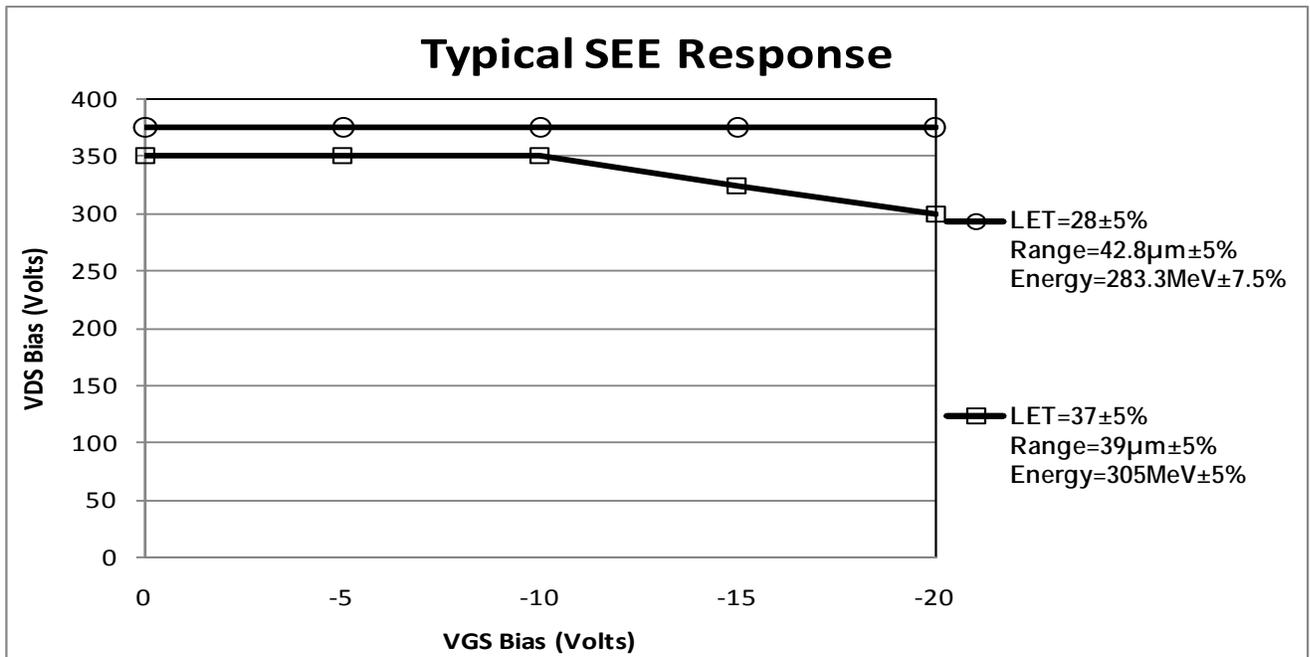
\*

FIGURE 6. Single event effects safe operation area.

### 2N7391, 2N7391D4



### 2N7392



\*

FIGURE 6 Single event effects safe operation area - Continued.

\* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil) or by facsimile (614) 693-1642 or DSN 850-6939.

6.10 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:  
Army - CR  
Navy - EC  
Air Force - 85  
NASA - NA  
DLA - CC

Preparing activity:  
DLA - CC  
  
(Project 5961-2017-013)

Review activities:  
Navy - AS  
Air Force - 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.