

The documentation and process conversion measures necessary to comply with this revision shall be completed by 2 June 2014.

INCH-POUND

MIL-PRF-19500/659A
2 April 2014
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20 August 1998

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED TRANSISTOR, P-CHANNEL SILICON TYPE 2N7440, AND 2N7441 JANSR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-Channel, radiation hardened, enhancement mode, MOSFET, power transistor. One level of product assurance is provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See [figure 1](#), (similar to TO-257).

1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T <u>1/</u> $T_C =$ $+25^\circ\text{C}$	P_T <u>1/</u> $T_A =$ $+25^\circ\text{C}$	V_{DS}	V_{DG}	V_{GS}	I_{D1} <u>2/</u> $T_C = +25^\circ\text{C}$	I_{D2} $T_C =$ $+100^\circ\text{C}$	I_S <u>2/</u>	I_{DM}	T_J and T_{STG}	V_{ISO} 70,000 ft. altitude
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>	<u>V dc</u>
2N7440	56	22	-100	-100	± 20	10.0	6.0	10.0	30	-55 to	N/A
2N7441			-200	-200		7.0	4.0	7.0	21	+150	N/A

1/ Derate linearly 0.45 W/°C for $T_C > +25^\circ\text{C}$; $P_T = (T_{jmax} - T_C)/R_{\theta JC}$

2/ $I_D = ((T_{jmax} - T_C)/(R_{\theta JC}) \times (r_{DS(on)} \text{ at } T_{jmax}))^{1/2}$

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0$ mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0$ mA dc	Max I_{DSS1} $V_{GS} = 0$ $V_{GS} = 80\%$ of rated V_{DS}	Max $r_{DS(on)}$ ^{1/} $V_{GS} = -12\text{V}$		$R_{\theta JC}$ Max	$I_{AS} = I_{DM}$	
				$T_J = 25^\circ\text{C}$ at I_{D2}	$T_J = 125^\circ\text{C}$ at I_{D2}			
	<u>V dc</u>	<u>V dc</u> Min Max		<u>$\mu\text{A dc}$</u>	<u>Ω</u>	<u>Ω</u>	<u>$^\circ\text{C/W}$</u>	<u>A (pk)</u>
2N7440	-100	-2.0	-6.0	25	0.28	0.50	2.2	30
2N7441	-200				0.65	1.24		21

^{1/} Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

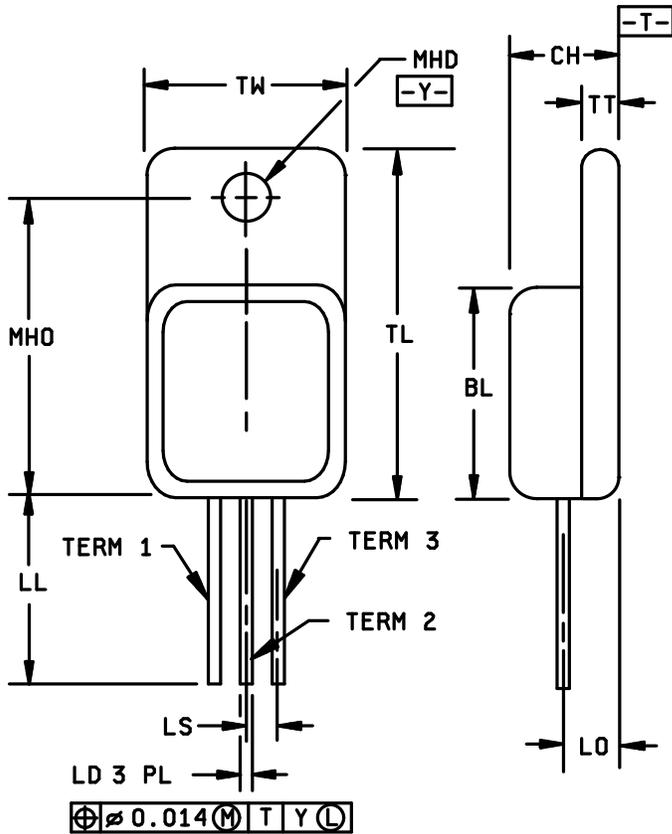
[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.405	.425	10.27	10.80
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.600	.650	15.24	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 TYP		2.54 TYP	
MHD	.140	.150	3.56	3.81
MHO	.522	.542	13.29	13.77
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Gate			
Term 2	Drain			
Term 3	Source			

NOTES:

1. Dimensions are in inches.
2. Equivalents are given for general information only.
3. All terminals are isolated from case.
4. The preferred measurements used herein are the inch units. This transistor was designed using inch-pound units of measurement. In case of conflicts between the metric and inch-pound units, the inch-pound units shall be the rule.
5. Die to base is BeO isolated, terminals to case ceramic (AL₂O₃) isolated.
6. In accordance with ANSI Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 1. Physical dimensions (similar to TO-257).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1 (TO-257AA) herein.

3.4.1 Lead material and finish. Lead material shall be Kovar, Alloy 52, and a copper core is permitted. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition requirement (see 6.2).

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.8 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of Inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E inspection. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see [table III](#) and [table IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with [table III](#). SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

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* 4.3 Screening (JANS only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen (See table E-IV of MIL-PRF-19500)	Measurement
	JANS
<u>1/</u>	E _{AS} test (see 4.5.4)
<u>1/</u>	Method 3161 (see 4.5.3)
<u>1/</u>	Gate stress test (see 4.5.5)
<u>2/</u>	Subgroup 2 of table I herein
9	I _{DSS1} , I _{GSS} as a minimum
10	MIL-STD-750, method 1042 test condition B
11	I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(ON)} , V _{GS(TH)} Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or $\pm 100\%$ of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or $\pm 100\%$ of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or $\pm 100\%$ of initial value, whichever is greater.
12	MIL-STD-750, method 1042 test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or $\pm 100\%$ of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or $\pm 100\%$ of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or $\pm 100\%$ of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20\%$ of initial value. $\Delta V_{GS(TH)1} = \pm 20\%$ of initial value.
17	For TO–257 packages: Method 1081 of MIL-STD-750 (see 4.3.1), Endpoints: Subgroup 2 of table I herein.

- 1/ Shall be performed anytime before screen 10.
2/ Shall be performed after E_{AS} test, method 3161, and gate stress test.

- * 4.3.1 Dielectric withstanding voltage.
 - a. Magnitude of test voltage.....800 V dc.
 - b. Duration of application of test voltage.....15 seconds (min).
 - c. Points of application of test voltage.....All leads to case (bunch connection).
 - d. Method of connection.....Mechanical.
 - e. Kilovolt-ampere rating of high voltage source.....1,200 V/1.0 mA (min).
 - f. Maximum leakage current.....1.0 mA.
 - g. Voltage ramp up time.....500 V/second.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and [table I](#) herein. Electrical measurements (end-points) shall be in accordance with the inspections of [table IV](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) of MIL-PRF-19500, and as follows. End point electrical measurements shall be in accordance with the applicable steps of [table IV](#) herein.

4.4.2.1 Group B inspection, table E-VIa (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Condition G, 100 cycles
B3	2077	
B4	1042	Condition D. The heating cycle shall be 30 seconds minimum.
B5	1042	Condition A, $V_{DS} = \text{rated}$; $T_A = +175^\circ\text{C}$; $t = 120$ hours, min.
B5	1042	Condition B, $V_{GS} = \text{rated}$; $T_A = +175^\circ\text{C}$; $t = 24$ hours.
B5	2037	Bond strength (Al-Au die interconnects only), Test condition A
B6	3161	Thermal resistance, see 4.5.2 .

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Electrical measurements (end points) and delta requirements shall be in accordance with the applicable steps of [table IV](#) herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Terminal strength, test condition A, weight = 10 lbs (4.54 Kg), 15 seconds.
C6	1042	Condition D, the heating cycle shall be 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal Resistance. Thermal Resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC} = 2.2^{\circ}\text{C/W}$. The following parameters shall apply:

- a. Measuring current (I_M).....10 mA
- b. Drain heating current (I_H).....1 A
- c. Heating time (t_H).....Steady-state (see MIL-STD-750, method 3161)
- d. Drain-source heating voltage (V_H).....-25 V
- e. Measurement time delay (t_{MD}).....30 to 60 μs
- f. Sample window time (t_{SW}).....10 μs maximum

4.5.3 Thermal Response (ΔV_{SD} measurement). The ΔV_{SD} measurement shall be performed in accordance with method 3161 of MIL-STD-750. The ΔV_{SD} conditions (I_H and V_H) and maximum limit shall be derived by each vendor from the thermal response curves (see figure 2) and shall be specified in the certificate of conformance prior to qualification. The following parameter measurements shall apply:

- a. Measuring current (I_M)..... 10 mA
- b. Drain heating current (I_H)..... 1 A
- c. Heating time (t_H)..... 100 ms
- d. Drain-source heating voltage (V_H)..... -25 V
- e. Measurement time delay (t_{MD})..... 30 - 60 μs
- f. Sample window time (t_{SW})..... 10 μs maximum

4.5.4 Single pulse avalanche energy (E_{AS}).

- a. $I_{AS} = I_{DM}$
- b. $L = 0.1 \text{ mH}$
- c. $E_{AS} = 1/2 L I_{AS}^2$
- d. $V_{DD} = -50 \text{ V to } -150 \text{ V dc}$
- e. Initial junction temperature = 25°C , -5°C , $+10^{\circ}\text{C}$

4.5.5 Gate stress test.

- a. $V_{GS} = -30 \text{ V}$
- b. $t = 250 \mu\text{s}$, minimum

TABLE I. Group A inspection

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Units
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Breakdown voltage drain to source	3407	$V_{GS} = 0V$, $I_D = 1$ mA dc, Bias condition C	$V_{(BR)DSS}$	-100 -200		V dc V dc
2N7440 2N7441						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1$ mA dc	$V_{GS(TH)1}$	-2.0	-6.0	V dc
Gate current	3411	$V_{GS} = \pm 20V$ dc, Bias condition C, $V_{DS} = 0V$	I_{GSS1}		± 100	nA dc
Drain current	3413	$V_{GS} = 0V$ dc, Bias condition C, $V_{DS} = 80\%$ of rated V_{DS} ,	I_{DSS1}		25	μA dc
Static drain to source "ON" state resistance	3421	$V_{GS} = -12V$ dc, condition A, Pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.28 0.65	Ω Ω
2N7440 2N7441						
Static drain to source "ON" state voltage	3405	$V_{GS} = -12V$ dc, condition A, Pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{DS(ON)}$		-3.36 -5.00	V dc V dc
2N7440 2N7441						
Forward voltage	4011	$V_{GS} = 0V$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		-1.8	V dc
<u>Subgroup 3</u>						
High temperature operation		$T_C = T_J = +125^\circ C$				
Gate current	3411	$V_{GS} = \pm 20V$ dc, Bias condition C, $V_{DS} = 0V$	I_{GSS2}		± 200	nA dc
Drain current	3413	$V_{GS} = 0V$ dc, Bias condition C, $V_{DS} = 80\%$ of rated V_{DS}	I_{DSS2}		0.25	mA dc

See footnotes at end of table.

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TABLE I. Group A inspection – Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Units
	Method	Conditions		Min	Max	
Static drain to source "ON"-state resistance 2N7440 2N7441	3421	$V_{GS} = -12V$ dc, condition A, Pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)2}$		0.50 1.24	Ω Ω
Gate to source voltage (threshold) Low temperature operation	3403	$V_{DS} \geq V_{GS}$, $I_D = 1$ mA dc $T_C = T_J = -55^\circ C$	$V_{GS(TH)2}$	-1.0		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, $I_D = 1$ mA dc	$V_{GS(TH)3}$		-7.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472]	$I_D = I_{D1}$, $V_{GS} = -12$ V dc $R_G = 7.5 \Omega$, $V_{DD} = 50\%$ of rated V_{DS}				
Turn-on delay time 2N7440 2N7441			$t_{D(on)}$		20 20	ns ns
Rise Time 2N7440 2N7441			t_r		55 35	ns ns
Turn-off delay time 2N7440 2N7441			$t_{D(off)}$		45 55	ns ns
Fall time 2N7440 2N7441			t_f		35 30	ns ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 3, $t_p = 10$ ms min. $V_{DS} = 80\%$ of max. rated V_{DS} ($V_{DS} \leq 200$ V)				
Electrical measurements		See table IV, steps 1,2,3,4,5, 6, and 7				

See footnotes at end of table.

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TABLE I. Group A inspection – Continued

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Units	
	Method	Conditions		Min	Max		
<u>Subgroup 6</u>							
Not applicable							
<u>Subgroup 7</u>							
Gate charge	3471	Condition B					
On-state gate charge			$Q_{G(ON)}$				
2N7440					40	nC	
2N7441					40	nC	
Gate to source charge			Q_{GS}				
2N7440					7.4	nC	
2N7441			7.6	nC			
Gate to drain charge			Q_{GD}				
2N7440				19	nC		
2N7441				19	nC		
Reverse recovery time	3473	$di/dt = 100 \text{ A/s}, V_{DD} \leq 30 \text{ V}, I_D = I_{D1}$					
2N7440			t_{rr}		160	ns	
2N7441					220	ns	

For sampling plan, see MIL-PRF-19500.

TABLE II. Group D Inspection

Inspection 1/ 2/ 3/ 4/	MIL-STD-750		Symbol	Pre-irradiation limits		Post irradiation limits		Units
	Method	Conditions		Min.	Max.	Min.	Max.	
<u>Subgroup 1</u>								
Not Applicable								
<u>Subgroup 2</u>								
T _C = +25°C								
Steady state total dose irradiation (V _{GS} bias)	1019	V _{GS} = -12V, V _{DS} = 0V						
Steady state total dose irradiation (V _{DS} bias)	1019	V _{GS} = 0V, V _{DS} = 80% of rated V _{DS}						
Breakdown voltage drain to source	3407	V _{GS} = 0V, I _D = 1 mA dc, Bias condition C	V _{(BR)DSS}					
2N7440				-100		-100		V dc
2N7441				-200		-200		V dc
Gate to source Voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = 1 mA dc	V _{GS(TH)1}	-2.0	-6.0	-2.0	-6.0	V dc
Gate current	3411	V _{GS} = ±20V dc, V _{DS} = 0V, Bias condition C	I _{GSS1}		±100		±100	nA dc
Drain current	3413	V _{GS} = 0V, V _{DS} = 80% of rated V _{DS} , Bias condition C	I _{DSS1}		25		25	μA dc
Static drain to source "ON"-state resistance	3421	V _{GS} = -12V dc, condition A, pulsed (see 4.5.1), I _D = I _{D2}	r _{DS(ON)1}					
2N7440					0.28		0.28	Ω
2N7441					0.65		0.65	Ω
Static drain to source "ON"-state voltage	3405	V _{GS} = -12V dc, condition A, Pulsed (see 4.5.1), I _D = I _{D1}	V _{DS(ON)}					
2N7440				-3.36		-3.36		V dc
2N7441				-5.00		-5.00		V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Electrical specifications are for 'D' and 'R' rad levels.

3/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other detail specification utilizing the same die design.

4/ At the manufacturer

assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package. Option, group D sample

TABLE III. Group E inspection (all quality levels) - For qualification only

Inspection <u>1/ 2/ 3/ 4/ 5/</u>	MIL-STD-750		Qualification and large lot quality conformance inspection.
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table IV , steps 1, 2, 3, 4, 5, 6, and 7	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state gate bias	1042	Test condition B; 1,000 hours	
Electrical measurements		See table IV , steps 1, 2, 3, 4, 5, 6, and 7	
Steady state reverse bias	1042	Test condition A; 1,000 hours	
Electrical measurements		See table IV , steps 1, 2, 3, 4, 5, 6, and 7	
<u>Subgroup 3</u>			
Not applicable			
<u>Subgroup 4</u>			22 devices c = 0
Thermal resistance	3161	$R_{\theta JC} = 2.2^{\circ}\text{C/W}$ maximum. See 4.5.2	
<u>Subgroup 5</u>			
Barometric pressure test (not required for $V_{BR(DSS)} \leq 200\text{V}$)	1001	Test condition C	15 devices c = 0

1/ A separate sample for each test may be pulled.

TABLE IV. Group A, B, C and E electrical measurements

Step	Inspection <u>1/</u> <u>2/</u>	MIL-STD-750		Symbol	Limits		Units
		Method	Conditions		Min	Max	
1.	Breakdown voltage drain to source 2N7440 2N7441	3407	$V_{GS} = 0V$, $I_D = 1 \text{ mA dc}$, Bias condition C	$V_{(BR)DSS}$	-100 -200	V dc V dc	
2.	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	-2.0	-6.0 V dc	
3.	Gate current	3411	$V_{GS} = \pm 20V \text{ dc}$, Bias condition C, $V_{DS} = 0V$	I_{GSS1}		± 100 nA dc	
4.	Drain current	3413	$V_{GS} = 0V \text{ dc}$, Bias condition C, $V_{DS} = 80\%$ of rated V_{DS}	I_{DSS1}		25 $\mu A \text{ dc}$	
5.	Static drain to source "ON"-state resistance 2N7440 2N7441	3421	$V_{GS} = -12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.28 0.65 Ω Ω	
6.	Static drain to source "ON"-state voltage 2N7440 2N7441	3405	$V_{GS} = -12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{DS(ON)}$		-3.36 -5.00 V dc V dc	
7.	Forward voltage	4011	$V_{GS} = 0V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		-1.8 V dc	
8.	Thermal response	3161	See 4.5.3	ΔV_{SD}		85 mV	

1/ The electrical measurements for table VIa (JANS) of MIL-PRF-19500 are as follows:

- a. Subgroup 3, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.
- b. Subgroup 4, see table IV herein, steps 1, 2, 3, 4, 5, 6, 7, and 8.
- c. Subgroup 5, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.

2/ The electrical measurements for table VII of MIL-PRF-19500 are as follows:

- a. Subgroup 2 and 3, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.
- b. Subgroup 6, see table IV herein, steps 1, 2, 3, 4, 5, 6, 7, and 8.

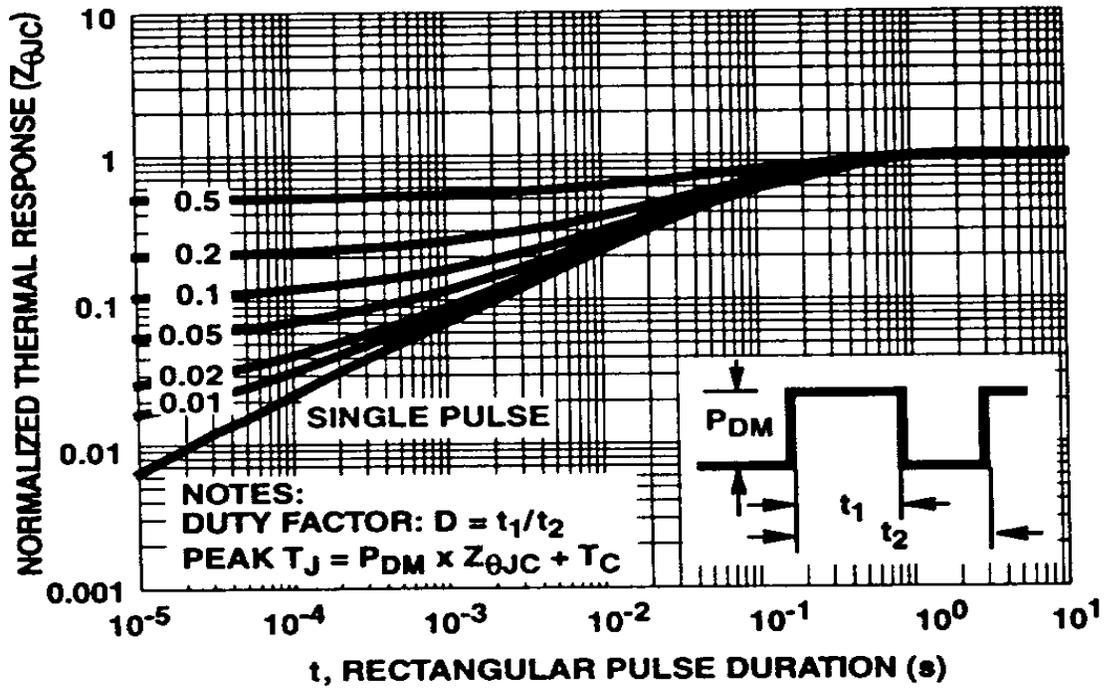
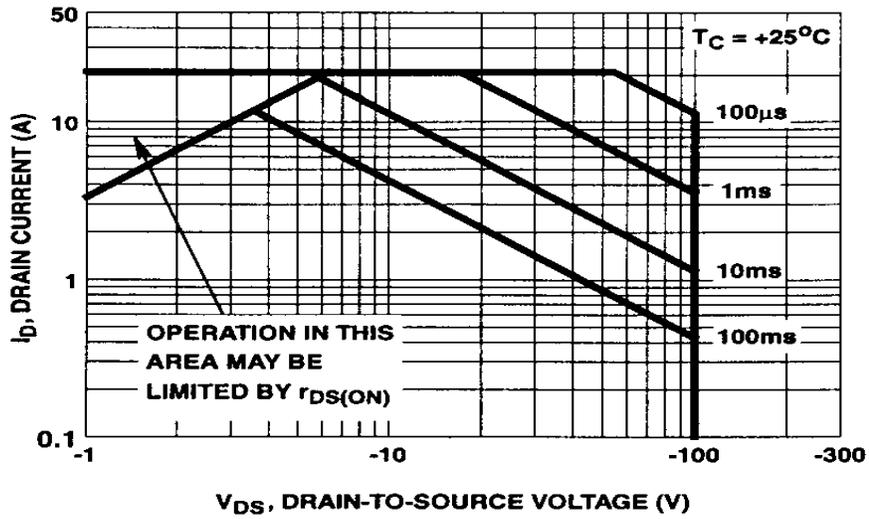


FIGURE 2. Thermal response curves

2N7440



2N7441

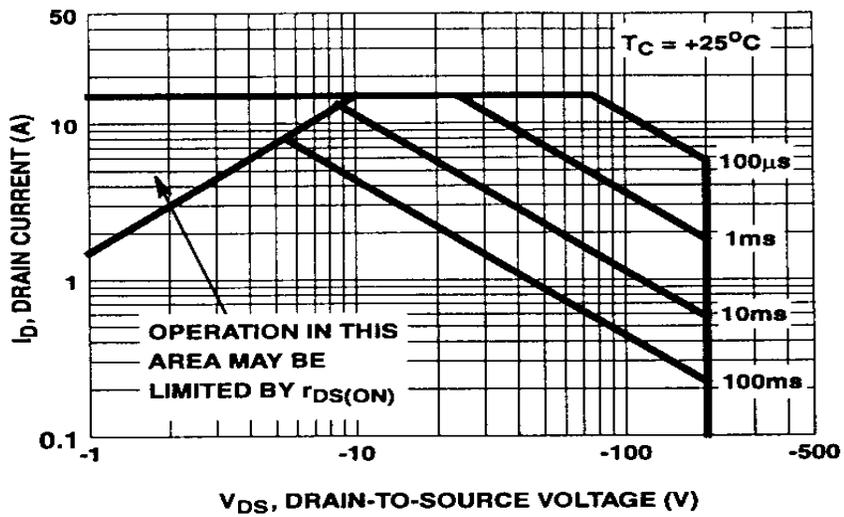


FIGURE 3. Safe operating area graphs

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead material and finish (see 3.4.1).
- d. The complete Part of Identifying Number (PIN), see title and section 1.
- e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If SEE testing data is desired, it should be specified in the contract or order.
- g. If specific SEE characterization conditions are desired (see section 6.6 and [table IV](#)), manufacturer's CAGE code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
SS913A0	2N7440
SS923A0	2N7441

6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA – NA
DLA – CC

Preparing activity:
DLA - CC

(Project 5961-2014-044)

Review activities:
Army - SM
Navy - AS, MC
Air Force - 19, 71, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.