The documentation and process conversion measures necessary to comply with this revision shall be completed by 25 May 2021.

INCH-POUND

MIL-PRF-19500/655G
W/AMENDMENT 1
25 February 2021
SUPERSEDING
MIL-PRF-19500/655G
18 September 2015

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED
P-CHANNEL, SILICON, TYPES 2N7424U, 2N7425U, AND 2N7426U,
JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a P-Channel, enhancement-mode, MOSFET, radiation hardened, power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}). See 6.7 for JANHC and JANKC die versions. Provisions for radiation hardness assurance (RHA) to two radiation levels ("R" and "F") are provided.

1.2 Package outlines. The device package outlines are as follows: surface mount SMD2 in accordance with figure 1 for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet MIL-PRF-19500/657.

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (1) T_C = +25°C	P_T T_A = +25°C	$R_{\theta JC}$ (2)	V_{DS}	V_{DG}	V_{GS}	I_{D1} (3) (4) T_C =+25°C	I_{D2} (3) (4) T_C = +100°C	I_S	I_{DM} (5)	T_J and T_{STG}
	W	W	°C/W	V dc	V dc	V dc	A dc	A dc	A dc	A (pk)	°C
2N7424U	300	2.5	0.42	-60	-60	±20	-48	-30	-48	-192	-55 to +150
2N7425U	300	2.5	0.42	-100	-100	±20	-38	-24	-38	-152	
* 2N7426U	300	2.5	0.42	-200	-200	±20	-29	-18	-29	-116	

(1) Derate linearly by 2.4 W/°C for T_C > +25°C.
(2) See figure 2, thermal impedance curves.
(3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS}(on) \text{ at } T_{JM})}}$$

(4) See figure 3, maximum drain current graph.
(5) I_{DM} = 4 X I_{D1} as calculated in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https//assist.dla.mil/.

1.4 Primary electrical characteristics at T_C = +25°C.

Type	Min $V_{(BR)DSS}$ V_{GS} = 0 I_D = -1.0mA dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ I_D = -1.0 mA dc		Max I_{DSS1} V_{GS} = 0 V_{DS} = 80% of rated V_{DS}	Max $r_{DS(on)}$ (1) V_{GS} = -12V, I_D = I_{D2}		E_{AS}
					T_J = +25°C	T_J = +150°C	
	V dc	V dc		µA dc	Ω	Ω	mJ
		Min	Max				
2N7424U	-60	-2.0	-4.0	-25	0.045	0.100	500
2N7425U	-100	-2.0	-4.0	-25	0.068	0.150	500
2N7426U	-200	-2.0	-4.0	-25	0.154	0.360	500

(1) Pulsed (see 4.5.1).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JANTXV” and "JANS".

1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See 6.7 for unencapsulated devices.

1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANTXV and JANS quality levels are as follows: "R" and "F".

1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7424”, “7425” and “7426”.

1.5.4.3 Suffix letters. The suffix letter "U" is used on devices that are packaged in the SMD2 package of figure 1.

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

* 1.6 Radiation features:

Maximum total ionizing dose (TID) available (Dose rate = 50-300 rad(Si)/s) in accordance with MIL-STD-750, method 1019, Condition A:

For device type JANSF2N7424U, JANSF2N7426U..... 300 krads(Si) 1/
For device type JANSR2N7425U:..... 100 krads(Si) 1/
For device type JANTXVF2N7424U, JANTXVF2N7425U, JANTXVF2N7426U..... 300 krads(Si) 1/

Heavy Ion Single Event Effect (SEE) SEB and SEGR test:

For device type 2N7424U:

No SEB and SEGR were observed at surface LET (see table IV) .....≤ 59.9 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = -40 V and V_{GS} = 0 V)
(In-situ Bias V_{DS} = -35 V and V_{GS} = 5 V)

For device type 2N7425U:

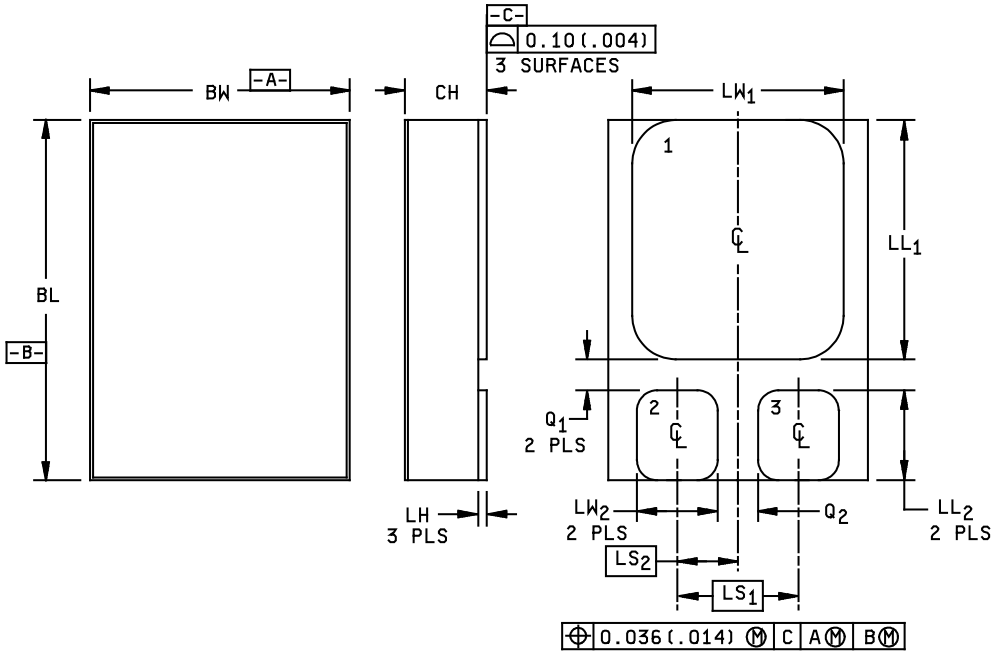
No SEB and SEGR were observed at surface LET (see table IV) .....≤ 59.9 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = -60 V and V_{GS} = -0 V)

For device type 2N7426U:

No SEB and SEGR were observed at surface LET (see table IV) .....≤ 28 MeV·cm^2/mg 2/
(In-situ Bias V_{DS} = -200 V and V_{GS} = 15 V)

1/ Manufacturer supplying device types 2N7424U, 2N7425U, AND 2N7426U has performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 300 krads(Si).

2/ Manufacturer also performed heavy ion SEB and SEGR test at Brookhaven National Lab Accelerator Radiation Effects Facility for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer. See 4.2.1.1



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
CH		.142		3.61
LH	.010	.020	0.25	0.51
LW1	.435	.445	11.05	11.30
LW2	.135	.145	3.43	3.68
LL1	.470	.480	11.94	12.19
LL2	.152	.162	3.86	4.11
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:
1. Dimensions are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate, and source.
4. In accordance with ASME Y14.5, diameters are equivalent to ϕx symbology.

FIGURE 1. Dimensions and configuration of SMD2 (U suffix).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.
* MIL-STD-883 - Test Method Standard for Microcircuits.

* (Copies of these documents are available online at https://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

I_{AS}.....Rated avalanche current, nonrepetitive
nC .....nano coulomb.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (SMD2) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

* 3.4.2 Internal construction. Multiple chip construction is not permitted.

* 3.4.3 Silicone die coating. The use of a silicone die coat requires a successful completion of MIL-STD-883, method 5011 on each silicone lot for its intended applications, and as part of the full MIL-PRF-19500 qualification process.

* 3.5 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of MIL-PRF-19500 to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

a. Devices should be handled on benches with conductive handling devices.

b. Ground test equipment, tools and personnel handling devices.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber or silk in MOS areas.

f. Maintain relative humidity above 50 percent if practical.

g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.

h. Gate must be terminated to source, R $\leq$ or 100 kΩ, whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE(SEB/SEGR) shall be performed in accordance with TM1080 of MIL-STD-750 at initial qualification and after process or design changes which may affect radiation hardness (see table III and table IV). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the performance specification sheet. End-point measurements shall be in accordance with table II. SEE (SEB/SEGR) characterization data shall be made available upon request of the qualifying or acquiring activity.

4.3 Screening (JANS and JANTXV). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

	Screen (see table E-IV of MIL-PRF-19500) (1)	Measurement	
		JANS level	JANTXV levels
	(2)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
	(2)	Method 3470 of MIL-STD-750 (see 4.3.2), E_{AS} test	Method 3470 of MIL-STD-750 (see 4.3.2), E_{AS} test
	(2) 3c	Method 3161 of MIL-STD-750 (see 4.3.3)	Method 3161 of MIL-STD-750 (see 4.3.3)
*	5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
*	9	Subgroup 2 of table I herein.	Not applicable
	10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
*	11	subgroup 2 of table I herein: ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater.	subgroup 2 of table I herein
	12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
	13	Subgroups 2 and 3 of table I herein; ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ± 20 percent of initial value. $\Delta V_{GS(th)1}$ = ± 20 percent of initial value.	Subgroup 2 of table I herein; ΔI_{GSSF1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{GSSR1} = ± 20 nA dc or ± 100 percent of initial value, whichever is greater. ΔI_{DSS1} = ± 10 μA dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1}$ = ± 20 percent of initial value. $\Delta V_{GS(th)1}$ = ± 20 percent of initial value.

(1) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1} and $V_{GS(th)1}$ shall be invoked.
(2) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements

4.3.1 Gate stress test. Apply V_{GS} = -24 V minimum for t = 250 µs minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

a. Peak current ..... $I_{AS} = I_{D1}$.

b. Inductance ..... $L = (2*E_{AS}/(I_{D1})^2)*((V_{BR}-V_{DD})/V_{BR})$ mH minimum.

c. Gate to source resistor..... R_{GS}: 25 Ω ≤ R_{GS} ≤ 200 Ω.

d. Supply voltage ..... V_{DD} = -25 V dc, except V_{DD} = -50 V dc for 2N7426U.

e. Initial case temperature..... T_C = +25° C, -5° C, +10° C.

f. Gate voltage ..... V_{GS} = -12 V dc.

g. Number of pulses to be applied ..... 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 µs max. See table III, group E, subgroup 4 herein.

* 4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and shall be evaluated for root cause and lot integrity.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows.

4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

	Subgroup	Method	Condition
	B3	1051	Test condition G, 100 cycles
	B3	2077	SEM
*	B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
	B4	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.
	B5	1042	Accelerated steady-state gate bias, condition B, V_{GS} = rated; T_A = +175°C, t = 24 hours minimum; or T_A = +150°C, t = 48 hours minimum.
	B5	1042	Accelerated steady-state reverse bias, condition A, V_{DS} = rated; T_A = +175°C, t = 120 hours minimum; or T_A = +150°C, t = 240 hours minimum.
	B5	2037	Bond strength, test condition D.

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

Subgroup	Method	Condition
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

Subgroup	Method	Condition
* C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	See 4.3.3, $R_{\theta JC(max)}$ = 0.42°C/W
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. t_{on} = 30 seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and table II herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal Impedance 2/	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source	3407	V_{GS} = 0V, I_D = -1 mA dc, bias condition C	$V_{(BR)DSS}$			
2N7424U				-60		V dc
2N7425U				-100		V dc
2N7426U				-200		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -1 mA dc	$V_{GS(TH)1}$	-2.0	-4.0	V dc
Gate current	3411	V_{GS} = ±20V dc, bias condition C, V_{DS} = 0V	I_{GSS1}		±100	nA dc
Drain current	3413	V_{GS} = 0V dc, bias condition C, V_{DS} = 80 percent of rated V_{DS},	I_{DSS1}		-25	µA dc
Static drain to source on state resistance	3421	V_{GS} = -12V dc, condition A, pulsed (see 4.5.1), I_D = I_{D2}	$r_{DS(ON)1}$			
2N7424U					0.045	Ω
2N7425U					0.068	Ω
2N7426U					0.154	Ω
Static drain to source on state resistance	3421	V_{GS} = -12V dc, condition A, pulsed (see 4.5.1), I_D = I_{D1}	$r_{DS(ON)2}$			
2N7424U					0.048	Ω
2N7425U					0.071	Ω
2N7426U					0.159	Ω
Forward voltage	4011	V_{GS} = 0V dc, condition A, pulsed (see 4.5.1), I_D = I_{D1}	V_{SD}			
2N7424U					-3.0	V dc
2N7425U					-3.3	V dc
2N7426U					-3.0	V dc

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 3						
High temperature operation		$T_C = T_J = +125°C$				
Gate current	3411	$V_{GS} = \pm 20V$ dc, bias condition C, $V_{DS} = 0V$	I_{GSS2}		±200	nA dc
Drain current	3413	$V_{GS} = 0V$ dc, bias condition C, V_{DS} = 80 percent of rated V_{DS}	I_{DSS2}		-0.25	mA dc
Static drain to source on-state resistance	3421	$V_{GS} = -12V$ dc, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)3}$			
2N7424U					0.085	Ω
2N7425U					0.135	Ω
2N7426U					0.35	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -1$ mA dc	$V_{GS(TH)2}$	-1.0		V dc
Low temperature operation		$T_C = T_J = -55°C$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS(TH)3}$, $I_D = -1$ mA dc	$V_{GS(TH)3}$		-5.0	V dc
Subgroup 4						
Switching time test	3472	$I_D = I_{D1}$, $V_{GS} = -12$ V dc, $R_G = 2.35$ Ω, V_{DD} = 50 percent of rated V_{DS}				
Turn-on delay time			$t_{D(on)}$			
2N7424U					35	ns
2N7425U					35	ns
2N7426U					37	ns
Rise time			t_r			
2N7424U					150	ns
2N7425U					170	ns
2N7426U					141	ns
Turn-off delay time			$t_{D(off)}$			
2N7424U					200	ns
2N7425U					190	ns
2N7426U					148	ns
Fall time			t_f			
2N7424U					200	ns
2N7425U					190	ns
2N7426U					220	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
Subgroup 4 - continued						
Forward transconductance	3475	I_D = rated I_{D2}, V_{DD} = 15 V (see 4.5.1)	g_{FS}			
2N7424U				18		S
2N7425U				15		S
2N7426U				14		S
Subgroup 5						
Safe operating area test (high voltage)	3474	See figure 4 t_p = 10 ms min. V_{DS} = 80 percent of max. rated V_{DS}				
Electrical measurements		See table I, subgroup 2				
Subgroup 6 Not applicable						
Subgroup 7						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{G(ON)}$			
2N7424U					300	nC
2N7425U					290	nC
2N7426U					300	nC
Gate to source charge			Q_{GS}			
2N7424U					70	nC
2N7425U					72	nC
2N7426U					65	nC
Gate to drain charge			Q_{GD}			
2N7424U					91	nC
2N7425U					90	nC
2N7426U					58	nC
Reverse recovery time	3473	Condition A, di/dt = -100 A/µs, $V_{DD} \leq$ -50 V $I_D = I_{D1}$	t_{rr}			
2N7424U					270	ns
2N7425U					300	ns
2N7426U					738	ns

1/ For sampling plan, see MIL-PRF-19500.

* 2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroups 2 and 6.
Group E, subgroup 1.

TABLE II. Group D inspection.

	Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
					R and F		R		F 4/		
		Method	Conditions		Min	Max	Min	Max	Min	Max	
	Subgroup 1										
	Not applicable										
	Subgroup 2		T_C = + 25°C								
*	Steady-state total dose irradiation (V_{GS} bias) 5/	1019	Condition A, V_{GS} = -12 V; V_{DS} = 0 V								
*	Steady-state total dose irradiation (V_{DS} bias) 5/	1019	Condition A, V_{GS} = 0 V; V_{DS} = 80 percent of rated V_{DS} (preirradiation)								
	End-point electricals										
	Breakdown voltage, drain to source	3407	V_{GS} = 0 V; I_D = -1 mA; bias condition C	$V_{(BR)DSS}$							
	2N7424U				-60		-60		-60		V dc
	2N7425U				-100		-100		-100		V dc
	2N7426U				-200		-200		-200		V dc
	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, I_D = -1 mA	$V_{GS(th)1}$							
	2N7424U				-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
	2N7425U				-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
	2N7426U				-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
	Gate current	3411	V_{GS} = -20 V, V_{DS} = 0 V, bias condition C	I_{GSSF1}		-100		-100		-100	nA dc
	Gate current	3411	V_{GS} = +20 V, V_{DS} = 0 V, bias condition C	I_{GSSR1}		100		100		100	nA dc
	Drain current	3413	V_{GS} = 0 V, V_{DS} = 80 percent of rated V_{DS} (preirradiation), bias condition C	I_{DSS}		-25		-25		-25	µA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbol	Pre-irradiation limits		Post-irradiation limits				Unit
				R and F		R		F 4/		
	Method	Conditions		Min	Max	Min	Max	Min	Max	
Subgroup 2 continued		T_C = + 25°C								
Static drain to source on-state voltage	3405	V_{GS} = -12 V, $I_D = I_{D2}$, condition A, pulsed (see 4.5.1)	$V_{DS(on)}$							
2N7424U					-1.35		-1.35		-1.35	V dc
2N7425U					-1.632		-1.632		-1.632	V dc
2N7426U					-2.772		-2.772		-2.88	V dc
* Forward voltage source drain diode	4011	V_{GS} = 0 V, $I_D = I_{D1}$, bias condition A	V_{SD}							
2N7424U					-3.0		-3.0		-3.0	V dc
2N7425U					-3.3		-3.3		-3.3	V dc
2N7426U					-3.0		-3.0		-3.0	V dc

1/ For sampling plan see MIL-PRF-19500.
2/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification utilizing the same die design.
3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.
4/ The "F" designation represents devices which pass end-points at R and F designated total-ionizing-dose (TID).
* 5/ Separate samples shall be pulled for each bias. Devices supplied to this specification sheet have been characterized through levels R and F of irradiation. Pre and Post irradiation values are identical unless otherwise specified in Table II. When performing post irradiation electrical measurements for any RHA level, TA = +25°C (see 1.6 herein).

TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I, subgroup 2	
Subgroup 2 1/			45 devices c = 0
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I, subgroup 2	
Subgroup 4			sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 10			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	22 devices c = 0
Subgroup 11			3 devices
SEE 2/ 3/	1080	See MIL-STD-750 method 1080 and 6.2.	

1/ A separate sample for each test shall be pulled.
2/ Group E qualification of SEE effect testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.
3/ Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

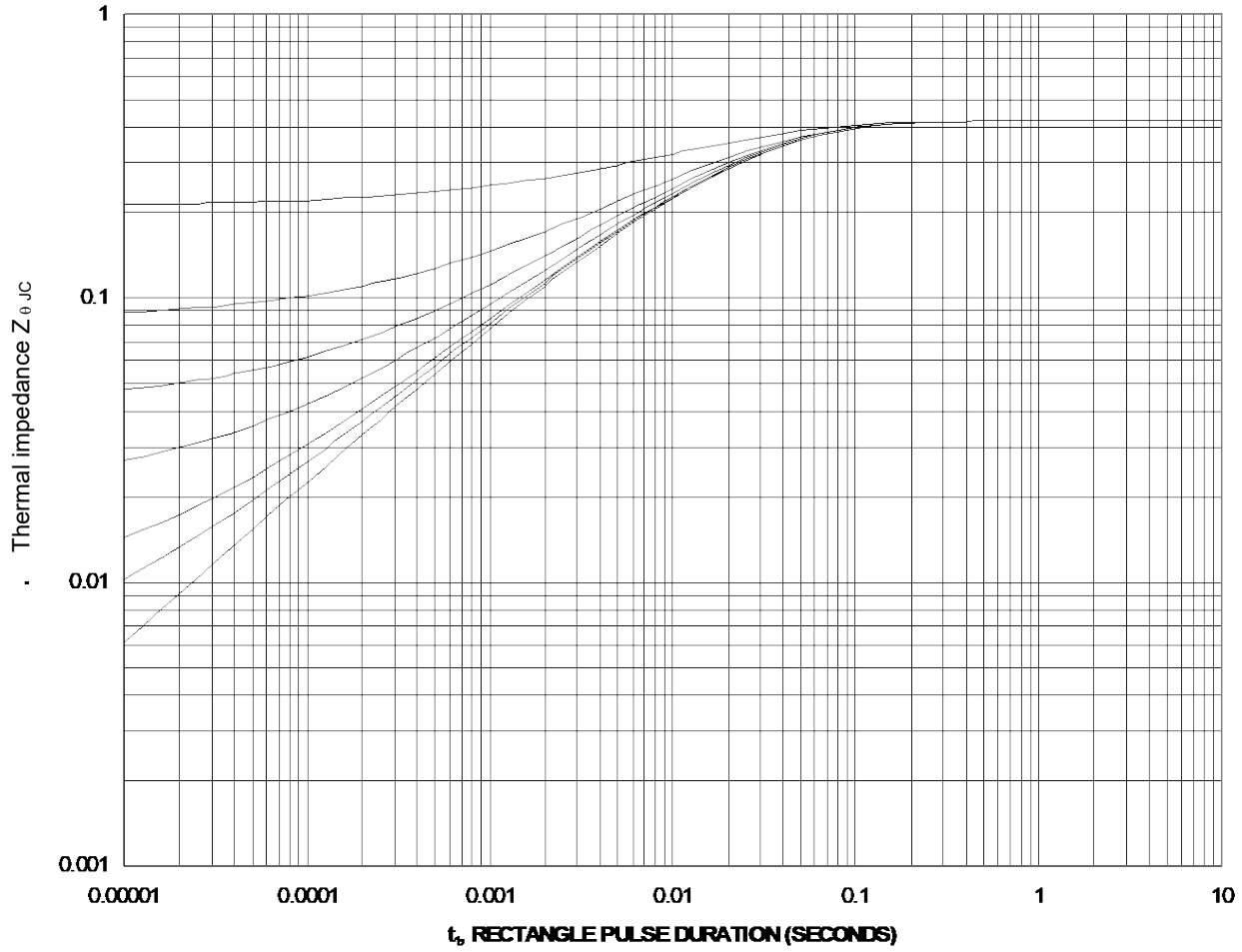
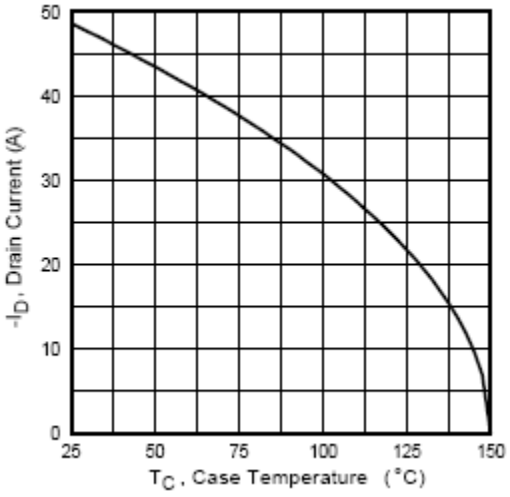
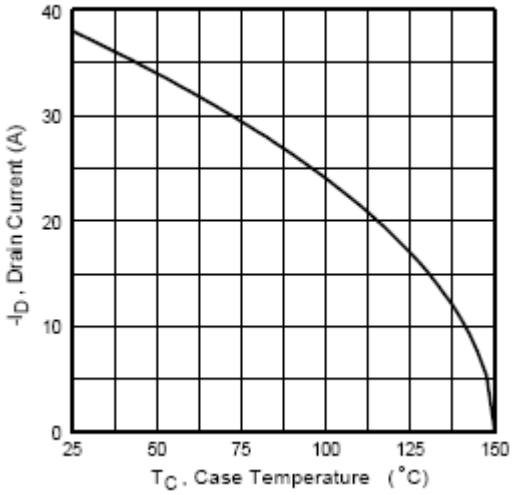


FIGURE 2. Thermal impedance curve.



2N7424U



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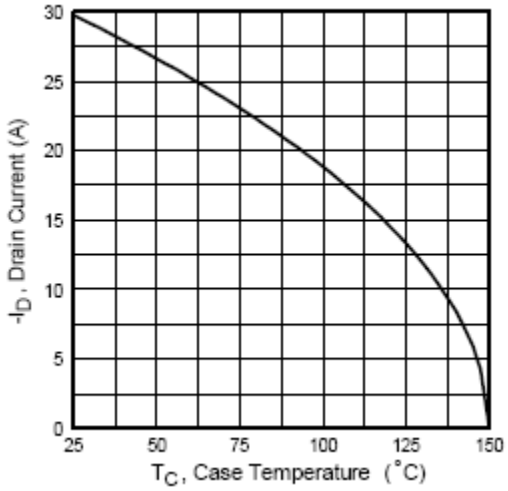
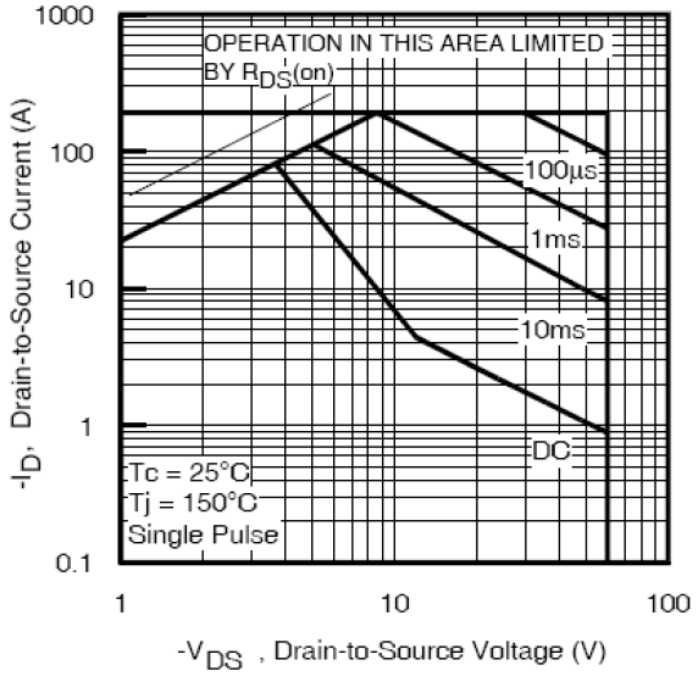


2N7426U

FIGURE 3. Maximum drain current versus case temperature graphs.

2N7424U



2N7425U

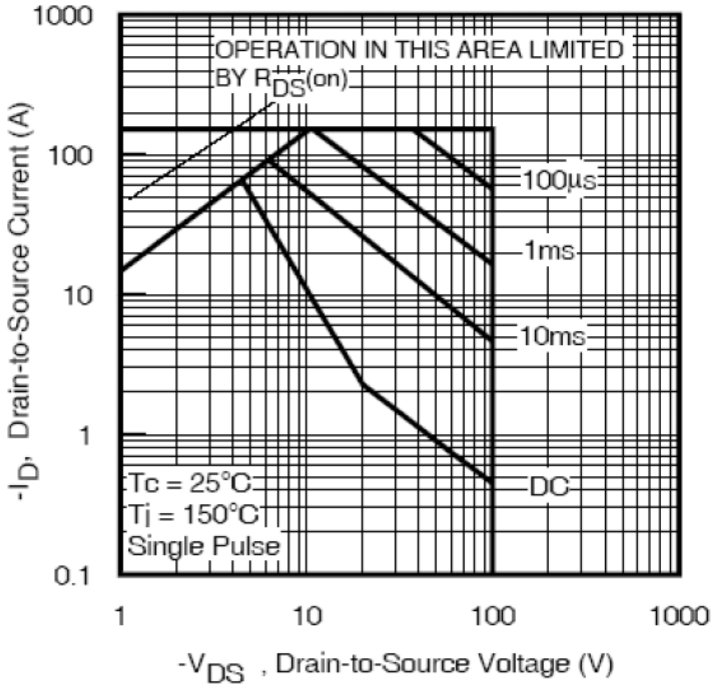
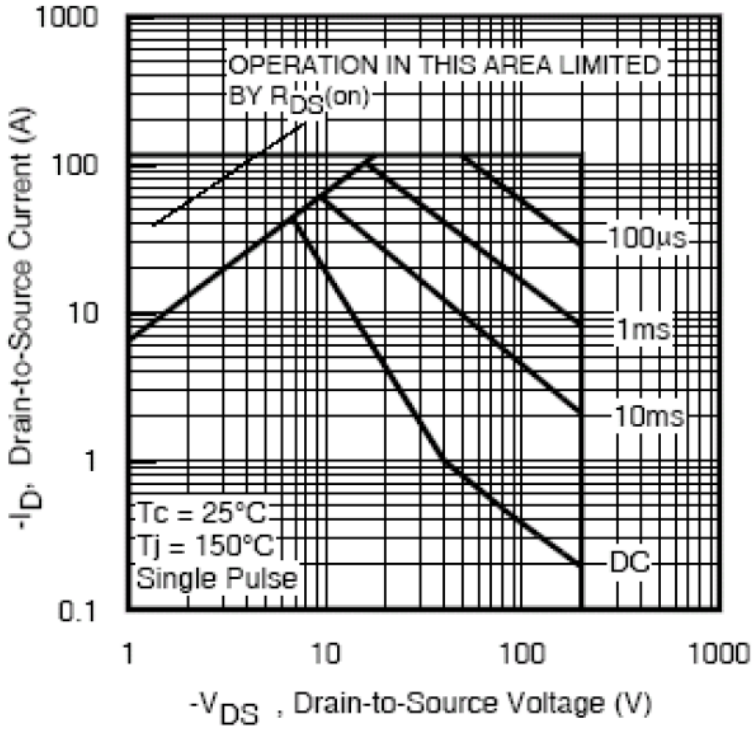


FIGURE 4 Safe operating area graph.



2N7426U

FIGURE 4. Safe operating area graph - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

c. Lead finish (see 3.4.1).

d. The complete PIN, see 1.5 and 6.5.

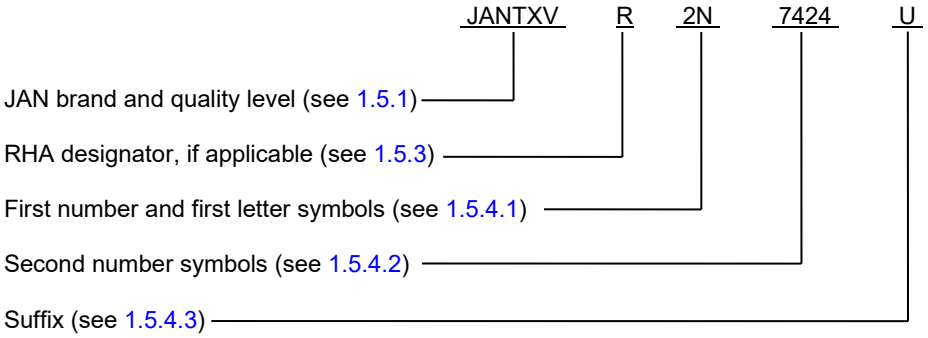
e. For acquisition of RHA designated devices, table II, subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it must be specified in the contract.

f. If SEE testing data is desired, it should be specified in the contract or order.

g. If specific SEE characterization conditions are desired (see section 6.8 and table IV), manufacturer's cage code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7424U	JANTXVF2N7424U	JANS2N7424U	JANS#2N7424U
JANTXV2N7425U	JANTXVF2N7425U	JANS2N7425U	JANS#2N7425U
JANTXV2N7426U	JANTXVF2N7426U	JANS2N7426U	JANS#2N7426U

(1) The number sign (#) represent one of two RHA designators available (R or F).

6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix).

Generic P/N	Military P/N
IRHNA9064	2N7424U
IRHNA9160	2N7425U
IRHNA9260	2N7426U

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under performance specification sheet MIL-PRF-19500/657.

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see table IV) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

* TABLE IV. Manufacturers characterization conditions.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of February 1998 and older)	SEE 1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 5	
	Pre SEB/SEGR Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	3 devices
	SEE irradiation:		Fluence = 3E5 percent ions/cm^2 Flux = 2E3 to 2E4 ions/cm^2/sec, temperature = 25º ±5 °C	
			Surface LET = 28 MeV-cm^2/mg, range = 42.8 µm, Cu ion beam energy = 283.3 MeV	
	2N7424U		In-situ bias conditions: V_{DS} = -60 V and V_{GS} = +5 V V_{DS} = -50 V and V_{GS} = +10 V V_{DS} = -35 V and V_{GS} = +15 V (typical 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7425U		In-situ bias conditions: V_{DS} = -100 V and V_{GS} = +10 V V_{DS} = -70 V and V_{GS} = +15 V V_{DS} = -60 V and V_{GS} = +20 V (nominal 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7426U		In-situ bias conditions: V_{DS} = -200 V and V_{GS} = +15 V (nominal 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
			Surface LET = 37 MeV-cm^2/mg, range = 39 µm, Br ion beam energy = 305 MeV	
	2N7424U		In situ bias conditions: V_{DS} = -55 V and V_{GS} = +0 V V_{DS} = -45 V and V_{GS} = +5 V V_{DS} = -35 V and V_{GS} = +10 V V_{DS} = -30 V and V_{GS} = +15 V (typical 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7425U		In situ bias conditions: V_{DS} = -100 V and V_{GS} = +5 V V_{DS} = -70 V and V_{GS} = +10 V V_{DS} = -50 V and V_{GS} = +15 V V_{DS} = -40 V and V_{GS} = +20 V (nominal 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)	
			Surface LET = 37 MeV-cm2/mg, range = 39 µm, Kr ion beam energy = 305 MeV	
	2N7426U		In situ bias conditions: V_{DS} = -200 V and V_{GS} = +5 V V_{DS} = -125 V and V_{GS} = +10 V V_{DS} = -75 V and V_{GS} = +15 V (nominal 3.63 MeV/nucleon at Brookhaven National Lab Accelerator)	

See footnotes at end of table.

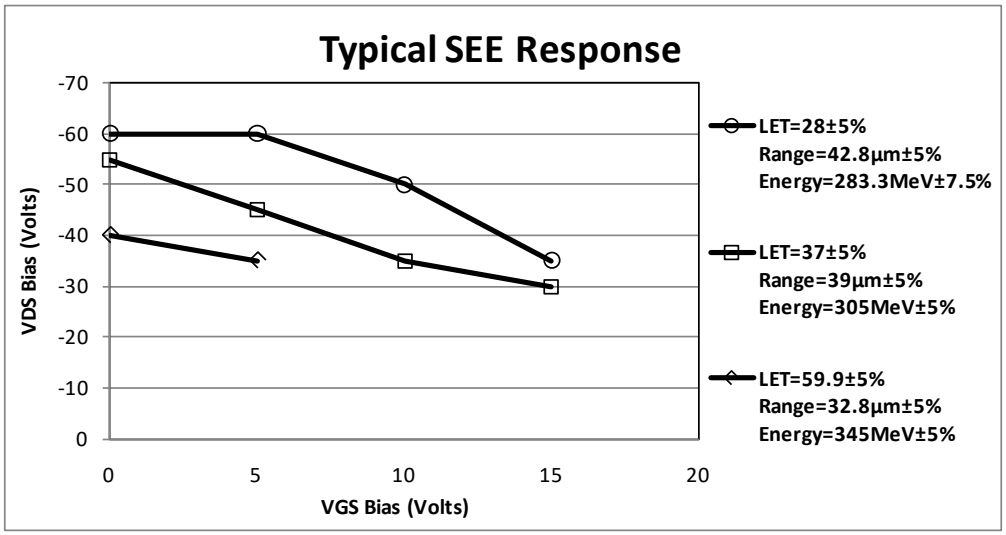
TABLE IV. Manufacturers characterization conditions - Continued.

Manufactures cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of February 1998 and older)	SEE - (Continued)1/	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 5	
	2N7424U		Surface LET = 59.9 MeV-cm^2/mg, range = 32.8 µm, I ion beam energy = 345 MeV In situ bias conditions: V_{DS} = -40 V and V_{GS} = 0 V V_{DS} = -35 V and V_{GS} = +5 V (typical 2.72 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7425U		In situ bias conditions: V_{DS} = -60 V and V_{GS} = 0 V (typical 2.72 MeV/nucleon at Brookhaven National Lab Accelerator)	
	Post SEB/SEGR Electrical measurements		I_{GSSF1}, I_{GSSR1}, and I_{DSS1} in accordance with table I, subgroup 2	
Upon qualification, all manufacturers should provide the verification test conditions to be added to this table.				

1/ I_{GSSF1}, I_{GSSR1}, and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

* 2/ Manufacturer performed heavy ion SEE(SEB/SEGR) test at Brookhaven National Lab Accelerator for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. No single event burnout (SEB) and Single event gate rupture (SEGR) were observed to surface LET as stated above table IV and safe operating area (see figure 5). Limits are characterized at initial qualification and after any design or process changes which may affect the SEE(SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.

2N7424U



2N7425U

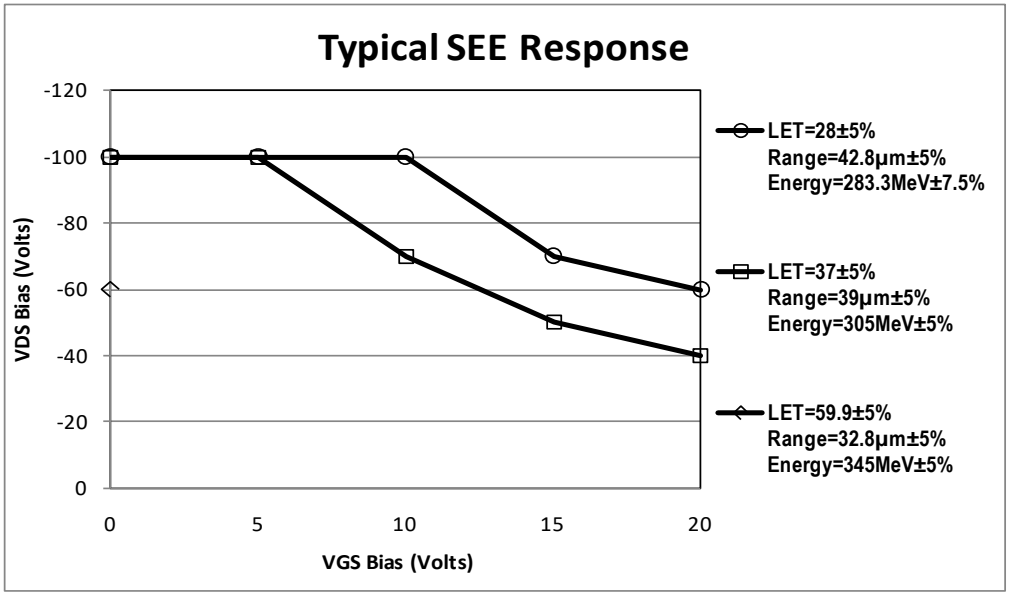
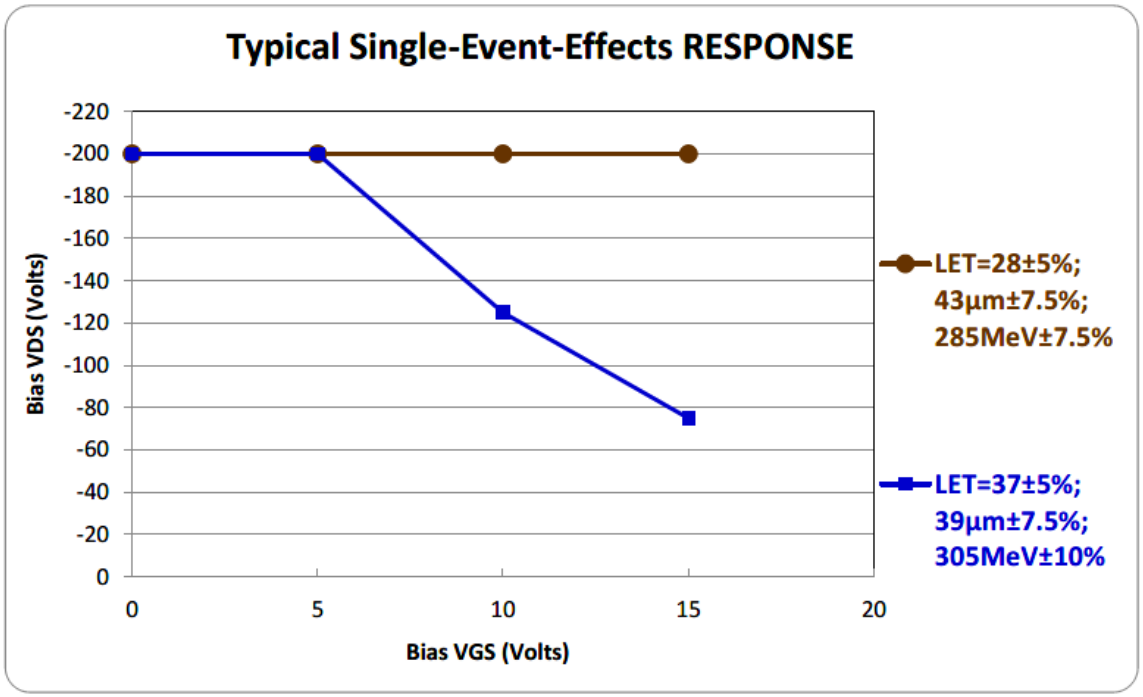


FIGURE 5. Typical single event effects safe operating area graphs.



* FIGURE 5. Typical single event effects safe operating area graphs - Continued.

* 6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

* 6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

Custodians:
Army - CR
* Navy - SH
Air Force - 85
* NASA - NA
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Preparing activity:
DLA - CC

(Project 5961-2020-075)

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