

The documentation and process conversion measures necessary to comply with this revision shall be completed by 7 August 2004.

INCH-POUND

MIL-PRF-19500/638B
 7 May 2004
 SUPERSEDING
 MIL-PRF-19500/638A
 29 November 1996

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT RADIATION HARDENED
 (TOTAL DOSE AND SINGLE EVENT EFFECTS) TRANSISTOR, N-CHANNEL
 SILICON, TYPE 2N7410,
 JANSR AND JANSR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

* The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for a N-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event characterization), power transistor. One level of product assurance is provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (similar to TO-205).

* 1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$	V_{DS}	V_{DG}	V_{GS}	I_{D1} (2) (3) $T_C = +25^\circ\text{C}$	I_{D2} $T_C = +100^\circ\text{C}$	I_S (2)	I_{DM} (4)	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A (pk)</u>	<u>°C</u>
2N7410	15	6	100	100	±20	3.5	2.5	3.5	10.5	-55 to +150

(1) Derate linearly 0.12 W/°C for $T_C > +25^\circ\text{C}$.

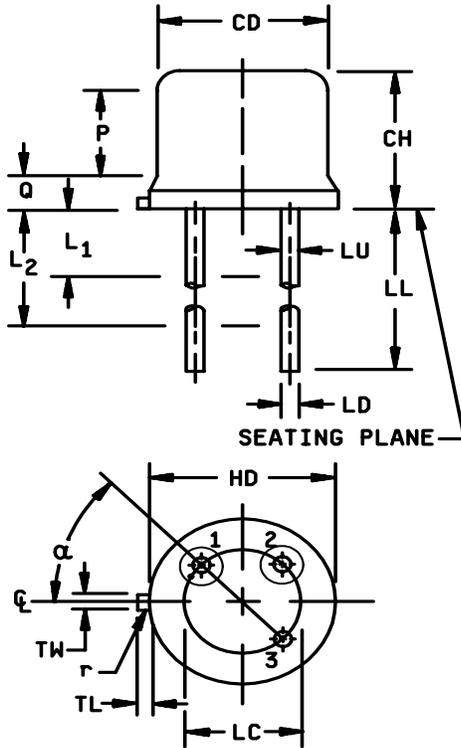
(2) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and internal wires and may be limited by pin diameter:

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

(3) See figure 2, maximum drain current graphs.

(4) $I_{DM} = 4 \times I_{D1}$ as calculated in note (2).

* Comments, suggestions, or questions on this document should be addressed to Defense Supply Center, Columbus, ATTN: DSCC-VAC, P.O. Box 3990, Columbus, OH 43216-5000, or emailed to Semiconductor@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://www.dodssp.daps.mil/>.



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
CD	.315	.335	8.01	8.50
CH	.160	.180	4.07	4.57
HD	.350	.370	8.89	9.39
LC	.190	.210	4.83	5.33
LD	.016	.023	0.41	0.58
LL	.500	.560	12.7	14.22
LU	.016	.021	0.41	0.53
L1		.050		1.27
L2		.250		6.35
P		.100		2.54
Q		.040		1.02
r		.010		0.018
TL	.029	.045	0.74	1.14
TW	.028	.034	0.72	0.86
α	45° TP		45° TP	
Term 1	Source			
Term 2	Gate			
Term 3	Drain			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Terminals 1 and 2 are isolated from case, terminal 3 is butt welded to stem base.
4. The preferred measurements used herein are the metric units. However, this transistor was designed using inch-pound units of measurement. In case of conflicts between the metric and inch-pound units, the inch-pound units shall be the rule.
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

* FIGURE 1. Dimensions and configuration (similar to TO-205).

1.4 Primary electrical characteristics at $T_C = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0 \text{ mA}$ dc	$V_{GS(TH)1}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0 \text{ mA}$ dc	Max I_{DSS1} $V_{GS} = 0$ $V_{GS} = 80$ percent of rated V_{DS}	Max $r_{DS(on)} (1)$ $V_{GS} = 12 \text{ V}$		$R_{\theta JC}$ Max	$I_{AS} = I_{DM}$
				$T_J = +25^\circ\text{C}$ at I_{D2}	$T_J = +125^\circ\text{C}$ at I_{D2}		
2N7410	<u>V dc</u> 100	<u>V dc</u> Min 1.5 Max 4.0	<u>$\mu\text{A dc}$</u> 25	<u>Ω</u> 0.600	<u>Ω</u> 0.960	<u>$^\circ\text{C/W}$</u> 8.3	<u>A (pk)</u> 10.5

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

* DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

* DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://www.dodssp.daps.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

- * 3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.
- * 3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).
- * 3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

I_{AS}Rated avalanche current, non-repetitive.
nC.....nano Coulomb.

- * 3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and figure 1 (similar to TO-205) herein.
- * 3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).
- 3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in paragraph 1.3, 1.4, and table I.
- * 3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.
- 3.7 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.7.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq$ or 100 k Ω , whenever bias voltage is applied drain to source.

- * 3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the transistor but shall be retained on the initial container.
- * 3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- * c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500. Alternate flow is allowed for qualification inspection in accordance with MIL-PRF-19500.

* 4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

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* 4.3 Screening (JANS only). Screening shall be in accordance with table IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table IV of MIL-PRF-19500) (1) (2)	Measurement
	JANS
(3)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, (see 4.3.3)
7	Optional.
9	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , subgroup 2 of table I herein.
10	Method 1042 of MIL-STD-750, test condition B
11	I_{GSSF1} , I_{GSSR1} , I_{DSS1} , $r_{DS(ON)}$, $V_{GS(TH)1}$ Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater.
12	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(ON)1} = \pm 20$ percent of initial value. $\Delta V_{GS(TH)1} = \pm 20$ percent of initial value.
14	Required.

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} , are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime before screen 9.

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* 4.3.1 Gate stress test. Apply $V_{GS} = 30$ V minimum for $t = 250$ μ s minimum.

* 4.3.2 Single pulse avalanche energy (E_{AS}).

- a. $I_{AS} = I_{DM}$.
- b. $L = 0.1$ mH.
- c. $E_{AS} = 1/2 LI_{AS}^2$.
- d. $V_{DD} = 50$ V to 150 V dc.
- e. Initial junction temperature = +25°C, -5°C, +10°C.

* 4.3.3 Thermal impedance (ΔV_{SD} measurement). The ΔV_{SD} measurement shall be performed in accordance with method 3161 of MIL-STD-750. The ΔV_{SD} conditions (I_H and V_H) and maximum limit shall be derived by each vendor from the thermal response curves (see figure 3) and shall be specified in the certificate of conformance prior to qualification. The following parameter measurements shall apply:

- a. Measuring current (I_M) 10 mA.
- b. Drain heating current (I_H) 1 A.
- c. Heating time (t_H) 10 ms.
- d. Drain-source heating voltage (V_H) 15 V.
- e. Measurement time delay (t_{MD}) 30 - 60 μ s.
- f. Sample window time (t_{SW}) 10 μ s maximum.

* 4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table V of MIL-PRF-19500 and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VIa (JANS) of MIL-PRF-19500, and as follows. End-point electrical measurements shall be in accordance with the applicable steps of table IV herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	SEM.
B4	1042	Intermittent operation life, condition D, 2,000 cycles. No heat sink nor or forced-air cooling on the device shall be permitted during the on cycle. $t_{ON} = 30$ seconds minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated; $T_A = +175^\circ\text{C}$; $t = 120$ hours, minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated; $T_A = +175^\circ\text{C}$; $t = 24$ hours.
B5	2037	Bond strength, test condition A.
B6	3161	Thermal resistance, see 4.5.2.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table VII of MIL-PRF-19500 and as follows. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table IV herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Terminal strength, test condition E, weight = 8 oz., 3 arcs.
* C5	3161	See 4.5.2.
C6	1042	Test condition D, 6,000 cycles; 1 cycle = 30 sec. min.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table VIII of MIL-PRF-19500 and table II herein.

4.4.4.1 Design parameters. Not tested on a per lot basis. Design shall be such that the devices shall be capable of meeting the requirements herein.

* 4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table IX of MIL-PRF-19500 and as specified in table III herein. Electrical measurements (end-points) and delta requirements shall be in accordance with the applicable steps of table IV herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be performed in accordance with method 3161 of MIL-STD-750. The maximum limit of $R_{\theta JC} = 8.3^{\circ}\text{C/W}$. The following parameters shall apply:

- a. Measuring current (I_M) 10 mA.
- b. Drain heating current (I_H) 1 A.
- c. Heating time (t_H) Steady-state (method 3161 of MIL-STD-750).
- d. Drain-source heating voltage (V_H) 15 V.
- e. Measurement time delay (t_{MD}) 30 to 60 μs .
- f. Sample window time (t_{SW}) 10 μs maximum.

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* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Breakdown voltage, drain to source	3407	Bias condition C $V_{GS} = 0 \text{ V}$, $I_D = 1.0 \text{ mA dc}$	$V_{(BR)DSS}$	100		V dc
Gate to source voltage (threshold)	3403	$V_{DG} \geq V_{GS}$,	$V_{GS(th)1}$	1.5	4.0	V dc
Gate current	3411	Bias condition C, $V_{GS} = +20 \text{ V dc}$, $V_{DS} = 0$	I_{GSSF1}		+100	nA dc
Gate current	3411	Bias condition C, $V_{GS} = -20 \text{ V dc}$, $V_{DS} = 0$	I_{GSSR1}		-100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V dc}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS1}		25	$\mu\text{A dc}$
Static drain to source on-state resistance	3421	Bias condition A, $V_{GS} = 12 \text{ V dc}$, $I_D = I_{D1}$, pulsed (see 4.5.1)	$r_{DS(ON)1}$		0.6	Ω
Static drain to source on-state voltage	3405	Bias condition A, $V_{GS} = 12 \text{ V dc}$, $I_D = I_{D1}$, pulsed (see 4.5.1)	$V_{DS(ON)}$		2.21	V dc
Forward voltage	4011	Bias condition A, pulsed (see 4.5.1), $I_D = I_{D1}$, $V_{GS} = 0 \text{ V dc}$	V_{SD}		1.8	V dc
<u>Subgroup 3</u>						
High temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Gate current	3411	Bias condition C, $V_{GS} = \pm 20 \text{ V dc}$, $V_{DS} = 0 \text{ V dc}$,	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0 \text{ V dc}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS2}		0.25	mA dc
Static drain to source on-state resistance	3421	$V_{GS} = 12 \text{ V dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)2}$		0.96	Ω

See footnote at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u> - Continued						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA}$	$V_{GS(th)2}$	0.5		V dc
Low temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA}$	$V_{GS(th)3}$		5.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D1}$; $V_{GS} = 12 \text{ V dc}$; $R_G = 7.5 \Omega$; $V_{DD} = 50 \text{ percent of rated } V_{DS}$				
Turn-on delay time			$t_{d(on)}$		30	ns
Rise time			t_r		60	ns
Turn-off delay time			$t_{d(off)}$		30	ns
Fall time			t_f		55	ns
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 4, $t_p = 10 \text{ ms}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$, $V_{DS} \leq 200 \text{ V dc max.}$				
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, 6, and 7				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge			$Q_{g(on)}$		8.5	nC
Gate to source charge			Q_{gs}		2.8	nC
Gate to drain charge			Q_{gd}		4.9	nC
Reverse recovery time	3473	$d_i/d_t \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq 30 \text{ V}$, $I_D = I_{D1}$	t_{rr}		220	ns

1/ For sampling plan, see MIL-PRF-19500.

TABLE II. Group D Inspection.

Inspection <u>1/ 2/ 3/ 4/</u>	MIL-STD-750		Symbol	Pre-irradiation limits		Post irradiation limits		Units
	Method	Conditions		Min.	Max.	Min.	Max.	
<u>Subgroup 1</u> Not applicable								
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$						
Steady-state total dose irradiation (V_{GS} bias)	1019	$V_{GS} = 12\text{V}, V_{DS} = 0\text{V}$						
Steady-state total dose irradiation (V_{DS} bias)	1019	$V_{GS} = 0\text{V}, V_{DS} = 80$ percent of rated V_{DS}						
Breakdown voltage drain to source	3407	$V_{GS} = 0\text{V}, I_D = 1 \text{ mA dc},$ bias condition C	$V_{(BR)DSS}$	100		100		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}, I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	1.5	4.0	1.5	4.0	V dc
Gate current	3411	$V_{GS} = \pm 20\text{V dc}, V_{DS} = 0 \text{ V},$ bias condition C	I_{GSS1}		± 100		± 100	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0\text{V}, V_{DS} = 80$ percent of rated V_{DS}	I_{DSS1}		25		25	$\mu\text{A dc}$
Static drain to source on-state resistance	3421	$V_{GS} = 12\text{V dc},$ condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.6		0.6	Ω
Static drain to source on-state voltage	3405	$V_{GS} = 12\text{V dc},$ condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{DS(ON)}$		2.21		2.21	V dc

1/ For sampling plan see MIL-PRF-19500.

2/ Electrical specifications are for 'D' and 'R' rad levels.

3/ Group D qualification may be performed prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification utilizing the same die design.

4/ At the manufacturer's option, group D samples need not be subjected to all the screening tests, but shall be assembled in its qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

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* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection <u>1/ 2/ 3/ 4/ 5/</u>	MIL-STD-750		Qualification and large lot quality conformance inspection.
	Method	Conditions	
<u>Subgroup 1</u>			12 devices c = 0
Temperature cycle	1051	Condition G, 500 cycles	
Hermetic seal	1071	Test conditions G or H	
Fine leak		Test conditions C or D	
Gross leak			
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, 6, and 7	
<u>Subgroup 2 1/</u>			45 devices c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, 6, and 7	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table IV, steps 1, 2, 3, 4, 5, 6, and 7	
<u>Subgroup 3</u>			3 devices, c = 0
DPA	2102		
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		Each supplier shall submit their qual-lot average and design maximum thermal impedance curves. In addition, the optimal test conditions and $Z_{\theta JX}$ limit shall be provided to the qualifying activity in the qualification report	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices
ESD	1020	Not required for devices classified as ESD class 1.	
<u>Subgroup 8</u>			
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476		22 devices c = 0

See footnotes at end of table.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only - Continued.

Inspection <u>1/ 2/ 3/ 4/ 5/</u>	MIL-STD-750		Qualification and large lot conformance inspection.
	Method	Conditions	
<u>Subgroup 9 3/</u> Electrical measurements <u>3/</u> SEE effect testing <u>4/</u> 2N7410 Electrical measurements <u>3/</u>	1080	See table IV, steps 3 and 4 See figure 5, Fluence = $3e5 \pm 20$ percent ions/cm ² Flux = $5e3$ to $2e4$ ions/cm ² sec Beam energy = 260 to 300 MeV Temperature = $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ LET = 26 to 30 MeV-cm ² /mg Ion range = 40 to 45 microns Insitu bias conditions: $V_{DS} = 100\text{V}$ and $V_{GS} = -20\text{V}$ LET = 36 to 40 MeV-cm ² /mg Ion range = 35 to 40 microns Insitu bias conditions: $V_{DS} = 100\text{V}$ and $V_{GS} = -10\text{V}$ $V_{DS} = 80\text{V}$ and $V_{GS} = -15\text{V}$ $V_{DS} = 50\text{V}$ and $V_{GS} = -20\text{V}$	3 devices <u>5/</u> c = 0
		See table IV, steps 3 and 4	

1/ A separate sample for each test may be pulled.

2/ Group E qualification of single event effect testing may be performed prior to lot formation. Wafers qualified to these group E QCI requirements may be used for any other specification utilizing the same die design.

3/ As a minimum, gate to source leakages and drain to source leakage are to be examined to verify the electrical performance of the DUT prior to and after test. At the manufacturer's option, the remaining static tests in table IV herein, with the exception of step 8, may be performed.

4/ Devices passing a given combination of drain and gate voltage for an LET of 36 to 40 MeV-cm²/mg qualify the same conditions for an LET of 26 to 30 MeV-cm²/mg

5/ This sampling plan applies to each bias condition defined.

* TABLE IV. Group A, B, C, and E electrical and delta measurements

Step	Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Limits		Units
		Method	Conditions		Min	Max	
1.	Breakdown voltage drain to source	3407	Bias condition C, $V_{GS} = 0V$, $I_D = 1 \text{ mA dc}$,	$V_{(BR)DSS}$	100		V dc
2.	Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1 \text{ mA dc}$	$V_{GS(TH)1}$	1.5	4.0	V dc
3.	Gate current	3411	$V_{GS} = \pm 20V \text{ dc}$, bias condition C, $V_{DS} = 0V$	I_{GSS1}		± 100	nA dc
4.	Drain current	3413	Bias condition C, $V_{GS} = 0V \text{ dc}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$	I_{DSS1}		25	$\mu A \text{ dc}$
5.	Static drain to source on-state resistance	3421	$V_{GS} = 12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(ON)1}$		0.6	Ω
6.	Static drain to source on-state voltage	3405	$V_{GS} = 12V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	$V_{DS(ON)}$		2.21	V dc
7.	Forward voltage	4011	$V_{GS} = 0V \text{ dc}$, condition A, pulsed (see 4.5.1), $I_D = I_{D1}$	V_{SD}		1.8	V dc
8.	Thermal impedance	3161	See 4.3.3	ΔV_{SD}		90	mV

1/ The electrical measurements for table VIa (JANS) of MIL-PRF-19500 are as follows:

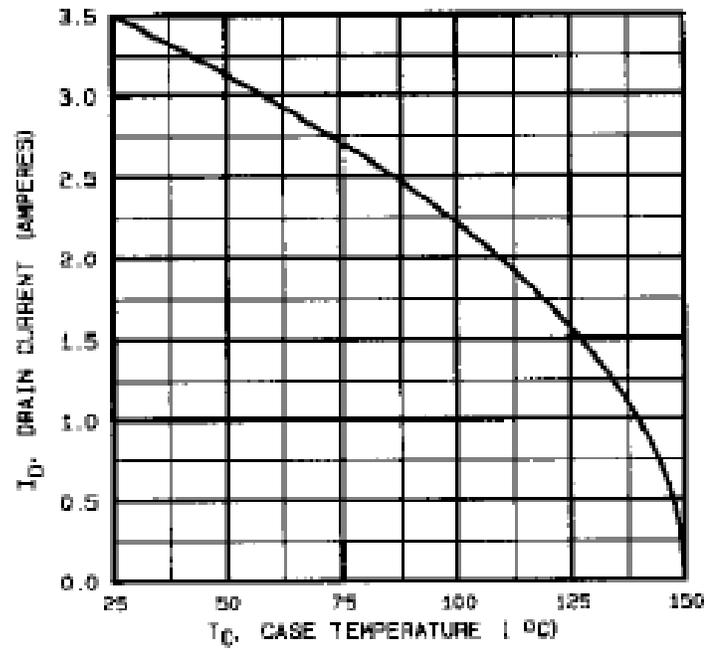
- a. Subgroup 3, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.
- b. Subgroup 4, see table IV herein, steps 1, 2, 3, 4, 5, 6, 7, and 8.
- c. Subgroup 5, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.

2/ The electrical measurements for table VII of MIL-PRF-19500 are as follows:

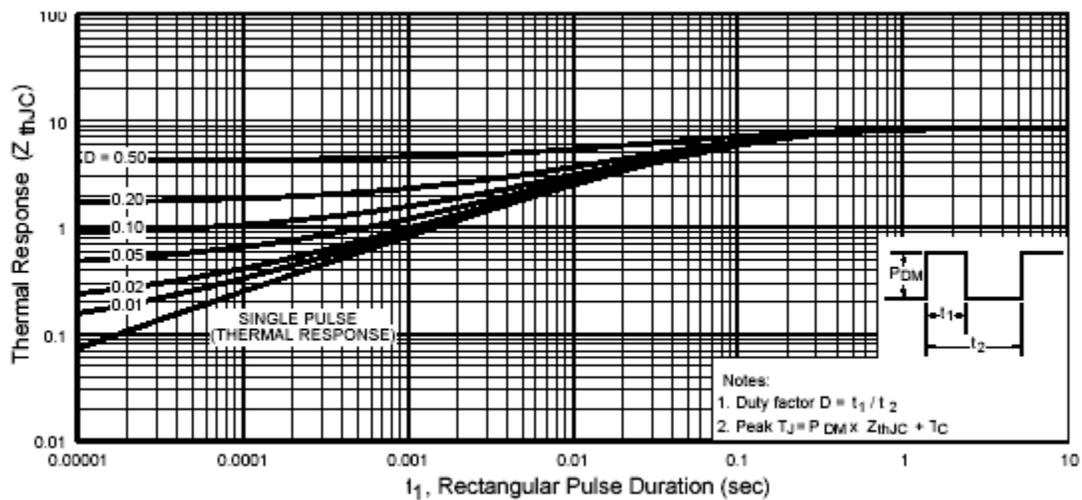
- a. Subgroup 2 and 3, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.
- b. Subgroup 6, see table IV herein, steps 1, 2, 3, 4, 5, 6, 7, and 8.

3/ The electrical measurements for table IX of MIL-PRF-19500 are as follows:

- a. Subgroup 1, see table IV herein, steps 1, 2, 3, 4, 5, 6, 7, and 8.
- b. Subgroup 2, see table IV herein, steps 1, 2, 3, 4, 5, 6, and 7.
- c. Subgroup 9, see table IV herein, steps 3 and 4.

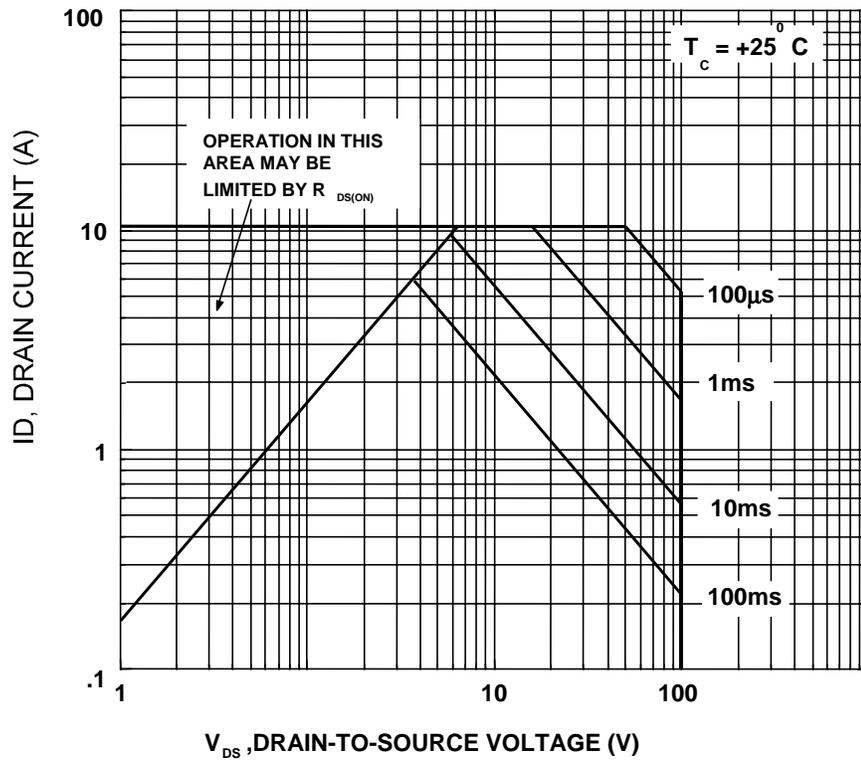


* FIGURE 2. Maximum drain current vs case temperature graph.



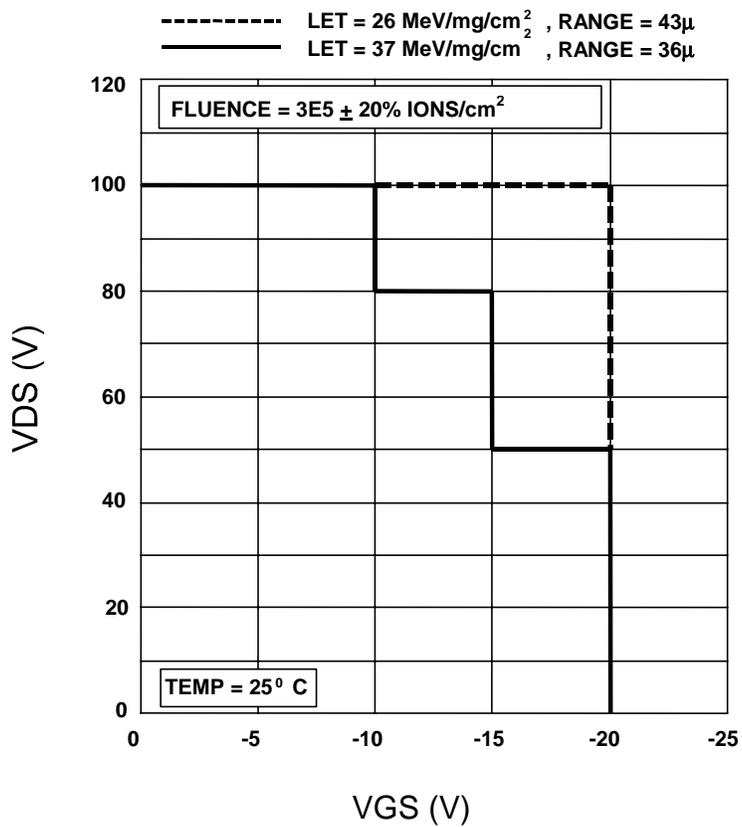
* FIGURE 3. Thermal response curves.

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* FIGURE 4. Safe operating area graphs.

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* FIGURE 5. Single event effects safe operating area graphs.

5. PACKAGING

* 5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

* 6.1 Intended use. The notes specified in MIL-PRF-19500 are applicable to this specification.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC/VQE, P.O. Box 3990, Columbus, OH 43216-5000 or e-mail vqe.chief@dla.mil.

* 6.4 Substitution information. Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PINs are suitable for the military PIN (without JAN and RHA prefix).

Generic P/N	Military PIN
SL110	2N7410

* 6.5 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 11
NASA - NA
DLA - CC

Preparing activity:
DLA - CC
(Project 5961-2858)

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://www.dodssp.daps.mil/>.