

The documentation and process conversion measures necessary to comply with this revision shall be completed by 23 October 2015.

INCH-POUND

MIL-PRF-19500/623E
 23 July 2015
 SUPERSEDING
 MIL-PRF-19500/623D
 25 March 2014

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, DARLINGTON, PNP SILICON,
 HIGH-POWER TYPE 2N7371 JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for PNP silicon, high-power Darlington transistor. Four levels of product assurance are provided for each encapsulated device (JAN, JANTX, JANTXV, and JANS).

1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	V_{CBO}	V_{CEO}	V_{EBO}	I_B	I_C	T_J and T_{STG}	$R_{\theta JC}$ (2)
	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>°C</u>	<u>°C/W</u>
2N7371	100	-100	-100	-5.0	-0.2	-12	-65 to +200	1.5

(1) See [figure 2](#) for temperature-power derating curves.

(2) See [figure 3](#), transient thermal impedance graph.

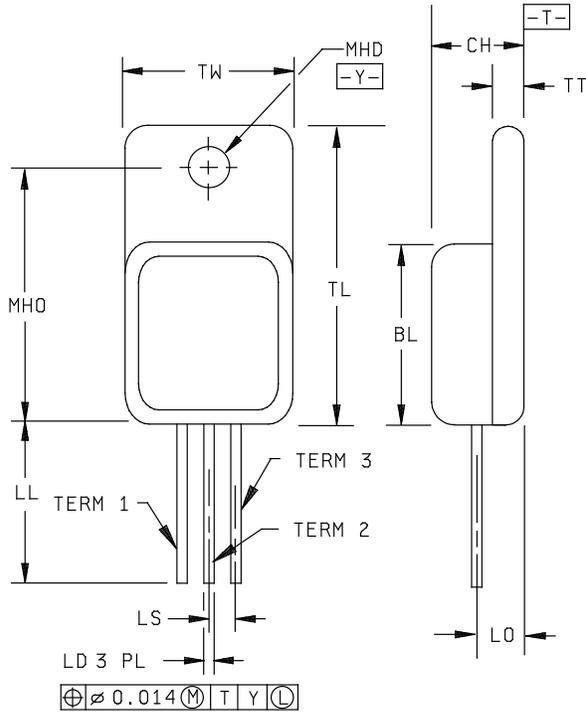
1.4 Primary electrical characteristics. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Limit	h_{FE1} (1) $V_{CE} = -3.0$ V dc $I_C = -6.0$ A dc	$V_{BE(SAT)}$ (1) $I_C = -12.0$ A dc $I_B = -120$ mA dc	$V_{CE(SAT)}$ (1) $I_C = -12.0$ A dc $I_B = -120$ mA dc	$ h_{fe} $ $V_{CE} = -3.0$ V dc $I_C = -5.0$ A dc $f = 1$ MHz
		<u>V dc</u>	<u>V dc</u>	
Min	1,000			10
Max	18,000	-4.0	-3.0	250

(1) Pulsed see [4.5.1](#).

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Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.535	.545	13.59	13.84
CH	.249	.260	6.32	6.60
LD	.035	.045	0.89	1.14
LL	.510	.570	12.94	14.48
LO	.150 BSC		3.81 BSC	
LS	.150 BSC		3.81 BSC	
MHD	.139	.149	3.53	3.78
MHO	.665	.685	16.89	17.40
TL	.790	.800	20.07	20.32
TT	.040	.050	1.02	1.27
TW	.535	.545	13.59	13.84
Term 1	Base			
Term 2	Collector			
Term 3	Emitter			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Dimensions and configuration (T0-254AA).

- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.
- * 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".
- * 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
- * 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
- * 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet is as follows: "7371".
- * 1.5.6 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 or 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 or 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on [figure 1](#). Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent ceramic AL_2O_3 or equivalent. Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-STD-750](#), [MIL-PRF-19500](#), and herein. Where a choice of lead finish or formation is desired, it shall be specified in the acquisition requirements (see [6.2](#)). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with table E-IV, screen 14, of [MIL-PRF-19500](#).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.6 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.7 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I and II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

- * 4.3 Screening (JANS, JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
9	I _{CEX1} and h _{FE1}	Not applicable
11	Subgroup 2 of table I herein; I _{CEX1} and h _{FE1} ; ΔI _{CEX1} = 100 percent of initial value or -2 μA dc, whichever is greater. Δh _{FE1} = ± 40 percent of initial value.	I _{CEX1} and h _{FE1}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; I _{CEX1} and h _{FE1} ; ΔI _{CEX1} = 100 percent of initial value or -2 μA dc, whichever is greater. Δh _{FE1} = ± 40 percent of initial value.	Subgroup 2 of table I herein; I _{CEX1} and h _{FE1} ; ΔI _{CEX1} = 100 percent of initial value or -2 μA dc, whichever is greater. Δh _{FE1} = ± 40 percent of initial value.

- * (1) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:

$$T_J = +175^\circ\text{C min, } V_{CE} = -10 \text{ to } -30 \text{ V dc, } T_A = +30 \pm 5^\circ\text{C.}$$

4.3.2 Thermal impedance (Z_{θJX} measurements). The Z_{θJX} measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, and t_{MD} (and V_C where appropriate). The Z_{θJX} limit used in screen 3c shall comply with the thermal impedance graph on figure 3 (less than or equal to the curve value at the same t_H time) and/or shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with appendix E, table V of MIL-PRF-19500, and table I herein.

- * 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500, and herein.

- * 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B4	1037	$V_{CB} \geq -10$ V dc.

- * B5 2037 Bond strength, test condition D.

B6	3131	See 4.5.2.
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- * 4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
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- * B3 1037 $V_{CB} \geq -10$ V dc.

B5	3131	See 4.5.2.
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B6	1032	$T_A = +200^\circ\text{C}$.
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- * 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
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C2	1056	Test condition B.
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C2	2036	Test condition A, weight = 4.5 kg, t = 10 seconds.
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C6	1037	$V_{CB} \geq -10$ V dc.
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- * 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurement shall be conducted in accordance with test method 3131 of MIL-STD-750. The following details shall apply:

- Collector current magnitude during power application shall be -1.0 A dc.
- Collector to emitter voltage magnitude shall be ≥ -10 V dc.
- Reference temperature measuring point shall be the case.
- Reference point temperature shall be $+25^\circ\text{C} \leq T_R \leq +75^\circ\text{C}$ and recorded before the test is started.
- Mounting arrangement shall be with heat sink to header.
- Maximum limit of $R_{\theta JC}$ shall be 1.5°C/W .

*

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.2	$Z_{\theta JC}$			
Collector - emitter breakdown voltage	3011	Bias condition D; $I_C = -100$ mA dc pulsed (see 4.5.1)	$V_{CE(sus)}$	-100		V dc
Collector - emitter cutoff current	3036	Bias condition D; $V_{CE} = -50$ V dc	I_{CEO}		-1.0	mA dc
Emitter - base cutoff current	3061	Bias condition D; $V_{EB} = -5$ V dc	I_{EBO}		-2.0	mA dc
* Collector - emitter cutoff current	3041	Bias condition A, $V_{BE} = +1.5$ V dc, $V_{CE} = -100$ V dc	I_{CEX1}		-20	μ A dc
Base - emitter saturated voltage	3066	Test condition A; $I_C = -12$ A dc; $I_B = -120$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$		-4.0	V dc
Collector - emitter saturated voltage	3071	$I_C = -12$ A dc; $I_B = -120$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)}$		-3.0	V dc
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc; $I_C = -6.0$ A dc pulsed (see 4.5.1)	h_{FE1}	1000	18,000	
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc; $I_C = -12$ A dc pulsed (see 4.5.1)	h_{FE2}	150		
<u>Subgroup 3</u>						
High - temperature operation:		$T_A = +150^\circ\text{C}$				
* Collector to emitter cutoff current	3041	Bias condition C, $V_{BE} = +1.5$ V dc, $V_{CE} = -100$ V dc;	I_{CEX2}		-1.0	mA dc
Low - temperature operation:		$T_A = -55^\circ\text{C}$				
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc $I_C = -6.0$ A dc pulsed (see 4.5.1)	h_{FE3}	300		

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

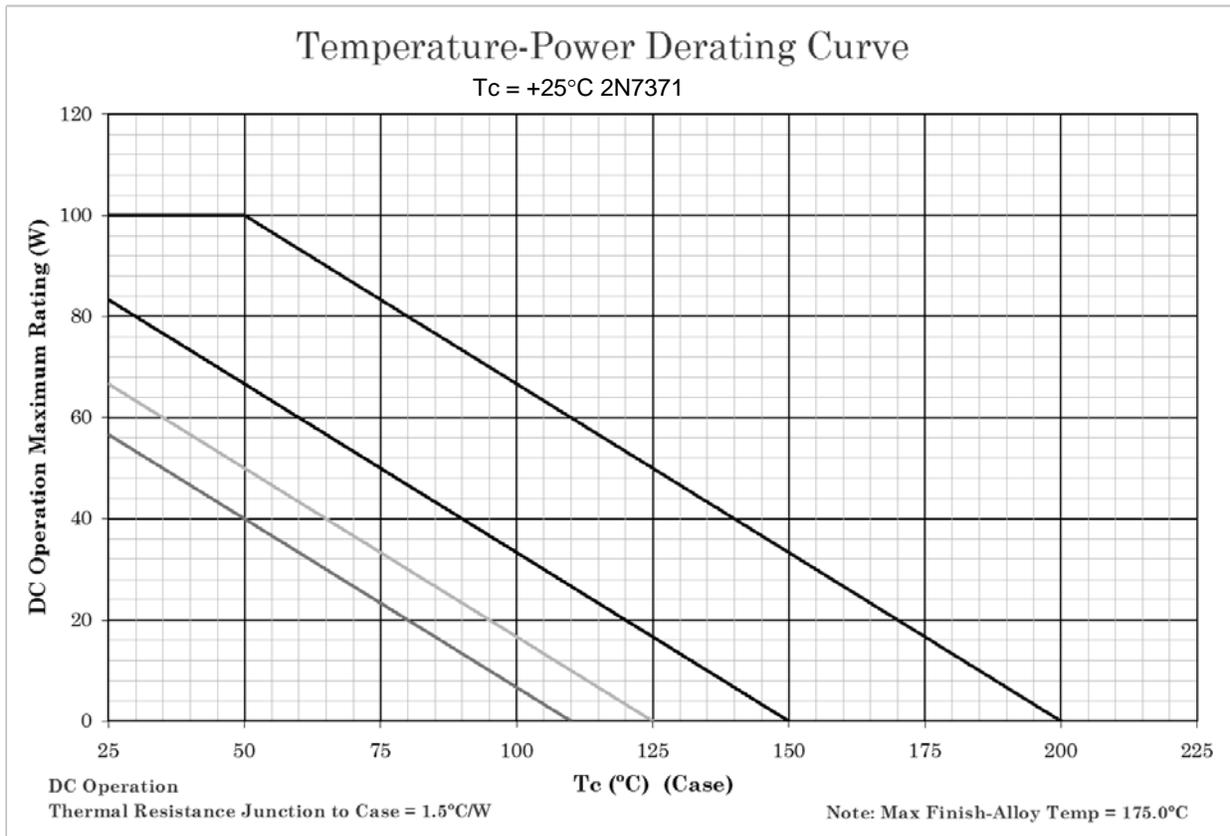
Inspection ^{1/}	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Switching parameters		See figure 4	t_{on}	2.0		μs
Turn-on		See figure 4	t_{off}	10		μs
Turn-off						
Magnitude of small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = -3.0$ V dc; $I_C = -5.0$ A dc; $f = 1$ MHz	$ h_{fe} $	10	250	
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = 25^\circ C$; $t \geq 1$ s; 1 cycle; (see figure 5)				
Test 1		$V_{CE} = -8.3$ V dc; $I_C = -12.0$ A dc				
Test 2		$V_{CE} = -30$ V dc; $I_C = -3.3$ A dc				
Test 3		$V_{CE} = -90$ V dc; $I_C = -150$ mA dc				
Safe operating area (clamped inductive)	3053	Load condition B (clamped inductive load); $T_A = +25^\circ C$; $t_r + t_f \leq 1.0$ μs ; duty cycle ≤ 2 percent; $t_p = 1$ ms; (vary to obtain I_C); $R_s = 0.10$ ohms; $R_{BB1} = 80$ ohms; $V_{BB1} = -16$ V dc; $R_{BB2} = 100$ ohms; $V_{BB2} = -1.5$ V dc; $I_C = -12$ A dc; $V_{CC} = -20$ V dc; $R_L \leq 2$ ohms; $L = 10$ mH; (Stancor C-2688 or equivalent) clamp voltage = -100 +0, -5 V dc; Device fails if clamp voltage not reached.				
Electrical measurements		See table I, subgroup 2				
<u>Subgroups 6 and 7</u>						
Not applicable						

^{1/} For sampling plan, see MIL-PRF 19500.

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* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	500 cycles.	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
High temperature reverse bias	1039	Condition A; 1,000 hours.	
Electrical measurements		See table I , subgroup 2 herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See table E-IX of MIL-PRF-19500 , group E, subgroup 4.	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B for devices < 400 V.	

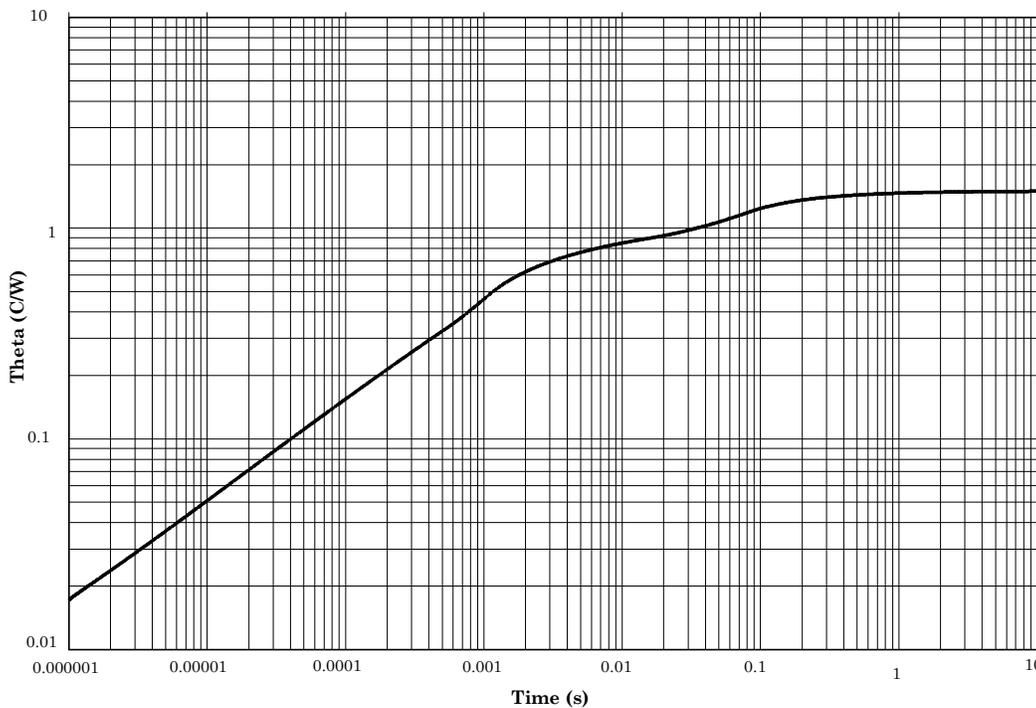


NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-power derating graph.

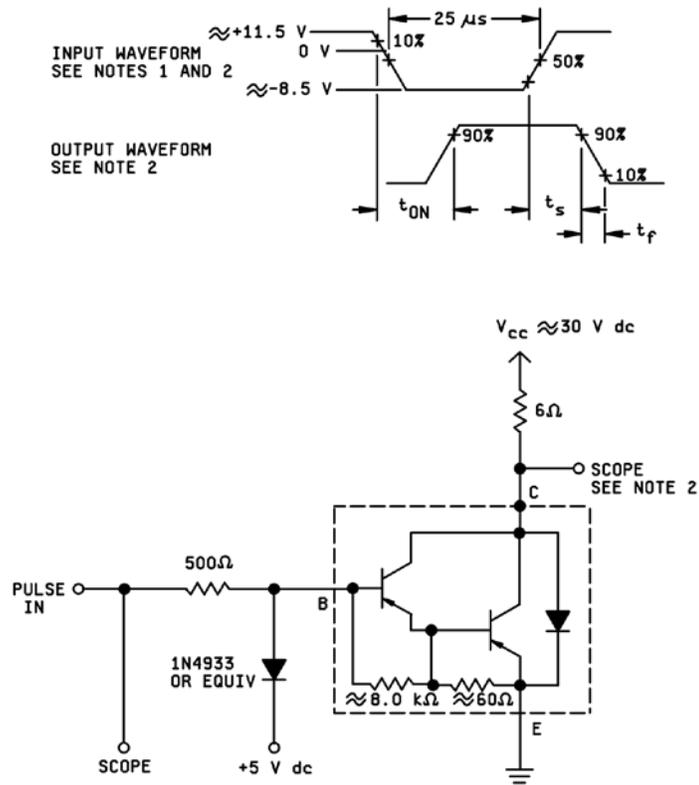
Maximum Thermal Impedance



$T_C = +25^{\circ}\text{C}$. Thermal resistance = $1.5^{\circ}\text{C}/\text{W}$.

FIGURE 3. Transient thermal impedance graph.

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NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics:
 $t_r \leq 20 \text{ ns}$, $t_f \leq 20 \text{ ns}$, $Z_{OUT} = 50 \Omega$, $PW = 25 \mu\text{s}$, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics:
 $t_r \leq 20 \text{ ns}$, $Z_{IN} \geq 20 \text{ k}\Omega$, $C_{IN} \leq 11.5 \text{ pF}$.
3. Resistors shall be noninductive types.
4. The dc power supplies may require additional by-passing in order to minimize ringing.

FIGURE 4. Pulse response test circuit.

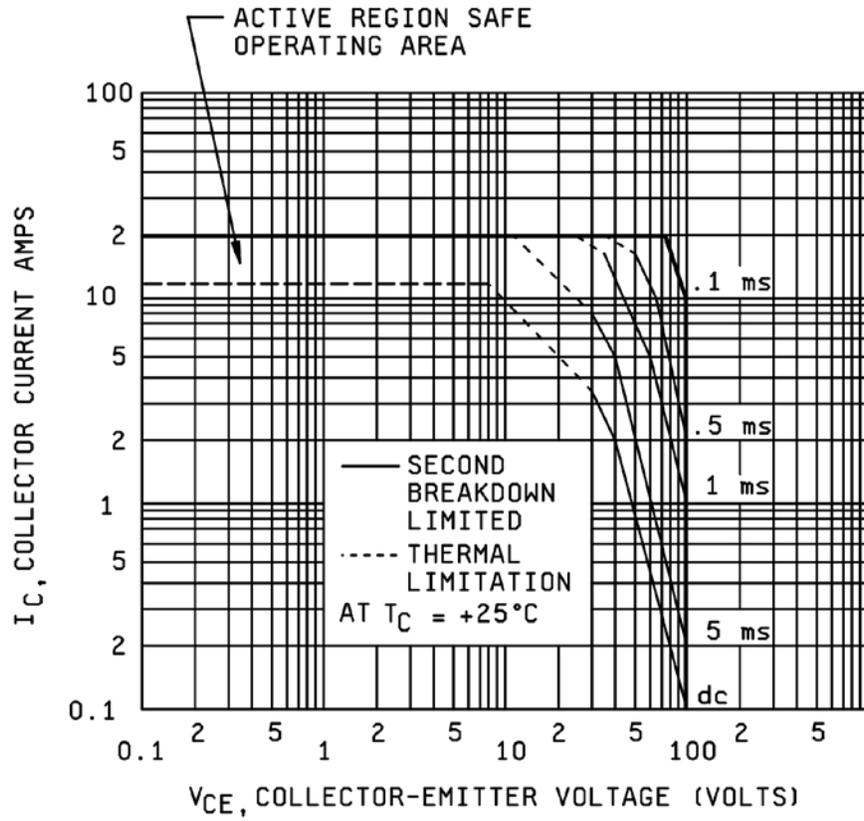


FIGURE 5. Safe operating area.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

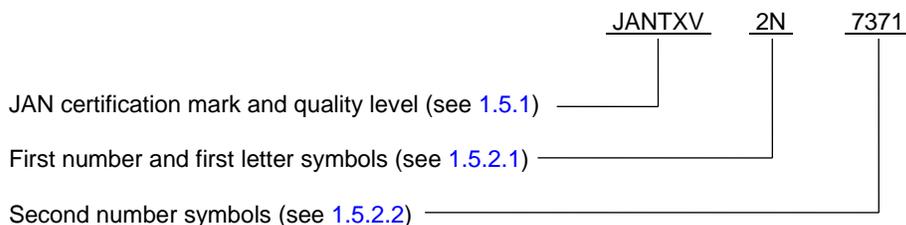
- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- * d. The complete Part or Identifying Number (PIN), see 1.5 and 6.6.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ([QML 19500](#)) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Interchangeability information. MIL-PRF-19500/623 is a TO-254 package version of [MIL-PRF-19500/501](#), which is a TO-3 package version. The military 2N7371 contains the same die as the military 2N6052. The MIL-PRF-19500/623 is preferred over the [MIL-PRF-19500/501](#) whenever interchangeability is not a problem. For new design use 2N7371. The 2N6052 is inactive for new design.

* 6.5 PIN construction example.

* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.6 List of PINs.

* 6.6.1 List of PINs for unencapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N7371	JANTX2N7371	JANTXV2N7371	JANS2N7371

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2015-074)

Review activities:
 Army - AR, MI, SM
 Navy - AS
 Air Force - 19, 99

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