

The documentation and process conversion measures necessary to comply with this revision shall be completed by 8 December 2021.

INCH-POUND

MIL-PRF-19500/614L
w/AMENDMENT 1
8 September 2021
SUPERSEDING
MIL-PRF-19500/614L
30 August 2018

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, FIELD EFFECT RADIATION HARDENED
ENCAPSULATED (THROUGH-HOLE AND SURFACE MOUNT PACKAGES)
N-CHANNEL, SILICON, TYPES 2N7380, AND 2N7381,
JANTXV AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for an N-channel, radiation hardened (total dose and single event effects (SEE)), enhancement mode, MOSFET, power transistors intended for use in high density power switching applications. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in [MIL-PRF-19500](#), with avalanche energy ratings (E_{AS}) and maximum avalanche current (I_{AS}). See 6.7 for JANHC and JANKC die versions.

1.2 Package outlines. The device package outlines are as follows: TO-257AA in accordance with [figure 1](#) and SMD-0.5 TO-276AA (U3) in accordance with [figure 2](#) for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in specification sheet [MIL-PRF-19500/657](#).

1.3 Maximum ratings. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

Type	P_T (1) $T_C = +25^\circ\text{C}$	P_T $T_A = +25^\circ\text{C}$ (free air)	$R_{\theta JC}$ (2)	Min $V_{(BR)DSS}$ $V_{GS} = 0\text{ V}$ $I_D = 1.0\text{ mA dc}$	I_{D1} (3) (4) $T_C = +25^\circ\text{C}$	I_{D2} (3) (4) $T_C = +100^\circ\text{C}$	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>$^\circ\text{C}$</u>
2N7380, 2N7380U3	75	2	1.67	100	14.4	9.1	-55 to +150
2N7381	75	2	1.67	200	9.4	6.0	-55 to +150

Type	I_S	I_{DM} (5)	V_{GS}	E_{AS} max	I_{AS}
	<u>A dc</u>	<u>A(pk)</u>	<u>V dc</u>	<u>mJ</u>	<u>A dc</u>
2N7380, 2N7380U3	14.4	57.6	± 20	150	14.4
2N7381	9.4	37.6	± 20	150	9.4

(See notes next page)

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1.3 Maximum ratings, continued

- (1) Derate linearly by 0.6 W/°C for T_C > +25°C.
- (2) See [figure 3](#), thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package and device construction.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See [figure 4](#), maximum drain current graph.
- (5) I_{DM} = 4 X I_{D1} as calculated in note (3).

1.4 Primary electrical characteristics. Unless otherwise specified, T_C = +25°C.

Type	Min V _{(BR)DSS} V _{GS} = 0 I _D = 1.0 mA dc	V _{GS(th)1} V _{DS} ≥ V _{GS} I _D = 1.0 mA dc		I _{DSS} max V _{GS} = 0	Max r _{DS(on)1} (1) V _{GS} = 12 V; I _D = I _{D2}	
				V _{DS} = 80 percent of rated V _{DS}	T _J = +25°C	T _J = +150°C
	V dc	V dc		μA dc	Ω	Ω
		Min	Max			
2N7380, 2N7380U3	100	2.0	4.0	25	0.18	0.36
2N7381	200	2.0	4.0	25	0.40	0.84

- (1) Pulsed (see [4.5.1](#)).

1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See [6.5](#) for PIN construction example and [6.6](#) for a list of available PINs.

1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See [6.7](#) for unencapsulated devices.

* 1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest are as follows: "M", "D", "R", "F".

1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7380" and "7381".

1.5.4.3 Suffix letters. No suffix letters are used on devices that are packaged in the TO-257AA package of [figure 1](#). The suffix letters "U3" are used on devices that are packaged in the SMD-0.5 TO-276AA package of [figure 2](#).

1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

1.5.6 Unencapsulated devices. See [6.7](#) for JANHC and JANKC die versions.

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* 1.6 Radiation features:

Maximum total ionizing dose (TID) available (Dose rate = 50-300 rad(Si)/s):

For device type 2N7380, 2N7380U3, 2N7381: 500 krads(Si) 1/

Heavy Ion Single Event Effect (SEE) SEB and SEGR test:

For device type 2N7380, 2N7380U3:

No SEB and SEGR were observed at surface LET (see table IV) $\leq 37 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ 2/

(In-situ Bias $V_{DS} = 100 \text{ V}$ and $V_{GS} = 0 \text{ V}$)

(In-situ Bias $V_{DS} = 90 \text{ V}$ and $V_{GS} = -5 \text{ V}$)

(In-situ Bias $V_{DS} = 70 \text{ V}$ and $V_{GS} = -10 \text{ V}$)

(In-situ Bias $V_{DS} = 50 \text{ V}$ and $V_{GS} = -15 \text{ V}$)

For device type 2N7381:

No SEB and SEGR were observed at surface LET (see table IV) $\leq 37 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ 2/

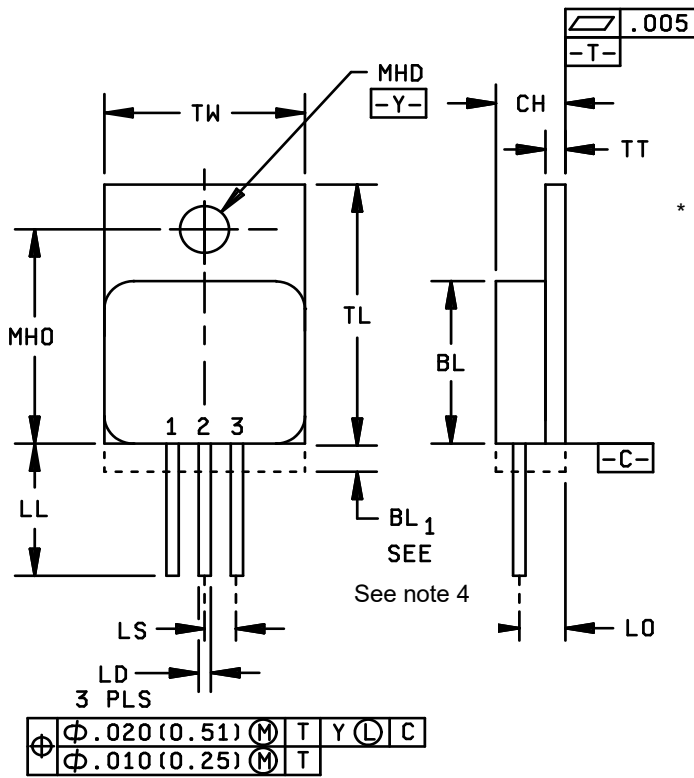
(In-situ Bias $V_{DS} = 100 \text{ V}$ and $V_{GS} = -10 \text{ V}$)

(In-situ Bias $V_{DS} = 50 \text{ V}$ and $V_{GS} = -15 \text{ V}$)

1/ Manufacturer supplying device types 2N7380, 2N7380U3, and 2N7381 has performed characterization testing in accordance with MIL-STD-750, method 1019, condition A (dose rate = 50 - 300 rad(Si)/s). The radiation end point limits are guaranteed only for the conditions as specified in MIL-STD-750, method 1019, condition A to a maximum total ionizing dose level of 500 krads(Si).

2/ Manufacturer also performed heavy ion SEB and SEGR test at Brookhaven National Lab Accelerator for the MOSFET technology devices in accordance with TM1080 of MIL-STD-750. Limits are characterized at initial qualification and after any design or process changes which may affect the SEE (SEB/SEGR) characteristics. For more information on SEE (SEB/SEGR) test results, customers are requested to contact the manufacturer.

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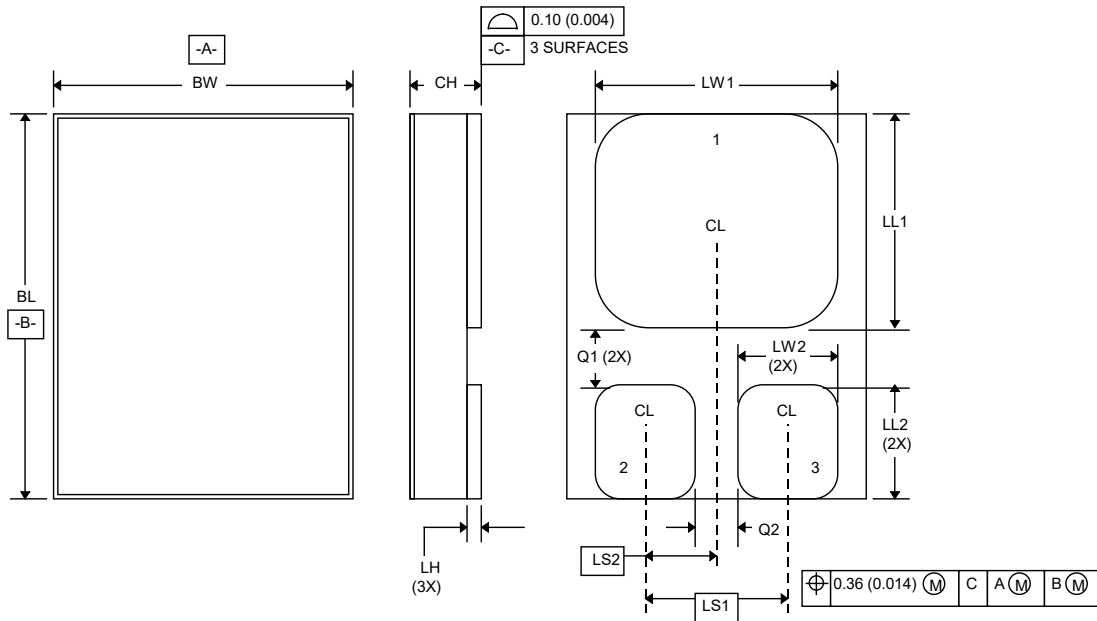
Ltr	Inches		Millimeters	
	Min	Max	Min	Max
BL	.410	.430	10.41	10.92
BL ₁		.028		0.71
CH	.190	.200	4.83	5.08
LD	.025	.035	0.64	0.89
LL	.500	.650	12.70	16.51
LO	.120 BSC		3.05 BSC	
LS	.100 BSC		2.54 BSC	
MHD	.140	.150	3.56	3.81
MHO	.527	.537	13.39	13.64
TL	.645	.665	16.38	16.89
TT	.035	.045	0.89	1.14
TW	.410	.420	10.41	10.67
Term 1	Drain			
Term 2	Source			
Term 3	Gate			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from case.
4. This area is for the lead feed-through eyelets (configuration is optional, but will not extend beyond this zone).
5. In accordance with ASME Y14.5, diameters are equivalent to ϕ x symbology.

* FIGURE 1. Dimensions and configuration (TO-257AA).

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Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.395	.405	10.04	10.28
BW	.291	.301	7.40	7.64
CH		.124		3.15
LH	.010	.020	0.25	0.51
LW1	.281	.291	7.14	7.39
LW2	.090	.100	2.29	2.54
LL1	.220	.230	5.59	5.84
LL2	.115	.125	2.93	3.17
LS1	.150 BSC		3.81 BSC	
LS2	.075 BSC		1.91 BSC	
Q1	.030		0.762	
Q2	.030		0.762	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimension are in inches.
2. Millimeters are given for information only.
3. The lid shall be electrically isolated from the drain, gate, and source.
4. In accordance with ASME Y14.5, diameters are equivalent to ϕ x symbology.

* FIGURE 2. Dimensions and configuration (TO-276AA, SMD-0.5).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

* [MIL-STD-750](#) - Test Methods for Semiconductor Devices.
[MIL-STD-883](#) - Test Methods Standard Microcircuits.

(Copies of these documents are available online at <https://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

IAS Rated avalanche current, non-repetitive.
nC nano Coulomb.
PIND Particle impact noise detector.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#) (TO-257AA) and [figure 2](#) (TO-276AA) herein. Methods used for electrical isolation of the terminal feedthroughs shall employ materials that contain a minimum of 90 percent Al₂O₃ (ceramic). Examples of such construction techniques are metallized ceramic eyelets or ceramic walled packages.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

* 3.4.3 Silicone Die coating. The use of a silicone die coat requires a successful completion of [MIL-STD-883](#), method [5011](#) on each silicone lot for its intended applications, and as part of the full [MIL-PRF-19500](#) qualification process.

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3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.6 Electrostatic discharge sensitive (ESDS). The devices covered by this specification sheet have been classified as ESDS. The devices shall be handled in accordance with the ESD program established to comply with the requirements of [MIL-PRF-19500](#) to avoid damage due to the accumulation of static charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent, if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source. $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.8 Electrical test requirements. The electrical test requirements shall be [table I](#) as specified herein.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I and II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE (SEB/SEGR) shall be performed in accordance with TM1080 of [MIL-STD-750](#) at initial qualification and after process or design changes which may affect radiation hardness (see [table III](#) and [table IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with [table II](#). SEE (SEB/SEGR) characterization data shall be made available upon request of the qualifying or acquiring activity.

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4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750. (see 4.3.2)	Method 3470 of MIL-STD-750. (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750 (see 4.3.3)	Method 3161 of MIL-STD-750 (see 4.3.3)
5	Method 2052 of MIL-STD-750, PIND (see MIL-PRF-19500 and 4.3.4)	Not applicable
9	Subgroup 2 of table I herein	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein.
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroup 2 and 3 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.	Subgroup 2 of table I herein. $\Delta I_{GSSF1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{GSSR1} = \pm 20$ nA dc or ± 100 percent of initial value, whichever is greater. $\Delta I_{DSS1} = \pm 25$ μ A dc or ± 100 percent of initial value, whichever is greater. $\Delta r_{DS(on)1} = \pm 20$ percent of initial value. $\Delta V_{GS(th)1} = \pm 20$ percent of initial value.
17	For TO-257AA packages: Method 1081 of (see 4.3.5), Endpoints: Subgroup 2 of table I herein	For TO-257AA packages: Method 1081 of (see 4.3.5), Endpoints: Subgroup 2 of table I herein

- (1) At the end of the test program, I_{GSSF1} , I_{GSSR1} , and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1} , I_{GSSR1} , I_{DSS1} , and $V_{GS(th)1}$ shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTXV level does not need to be repeated in screening requirements.

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4.3.1 Gate stress test. Apply $V_{GS} = \pm 30$ V minimum for $t = 250$ μ s minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current (I_{AS})..... I_{D1} .
- b. Peak gate voltage (V_{GS}).....12 V.
- c. Gate to source resistor (R_{GS})..... $25 \leq R_{GS} \leq 200 \Omega$.
- d. Initial case temperature $+25^{\circ}\text{C} +10^{\circ}\text{C}, -5^{\circ}\text{C}$.
- e. Inductance $\left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- f. Number of pulses to be applied1 pulse minimum.
- g. Supply voltage $V_{DD} = 50$ V, or 25 V for 100 V devices.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of [MIL-STD-750](#) using the guidelines in that method for determining I_M , I_H , t_H , t_{MD} , t_{SW} , (and V_H where appropriate). See [table III](#), group E, subgroup 4 herein.

4.3.4 PIND. Not applicable in screening when devices are processed using alternative method and flow requirements approved by the qualifying activity, that includes incorporating the use of certified clean processing and silicone die coat. Instead, the PIND test performance shall be performed in group B3 and group C3, on a lot sample basis. PIND failures detected in group B or C will represent lot jeopardy and be evaluated for root cause and lot integrity.

4.3.5 Dielectric withstanding voltage.

- a. Magnitude of test voltage800 V dc for TO-257AA, 600 V dc for TO-276AA.
- b. Duration of application of test voltage15 seconds (min).
- c. Points of application of test voltageAll leads to case (bunch connection).
- d. Method of connectionMechanical.
- e. Kilovolt-ampere rating of high voltage source1,200 V/1.0 mA (min).
- f. Maximum leakage current.....1.0 mA.
- g. Voltage ramp up time.....500 V/second

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein.

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4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of [MIL-PRF-19500](#), and as follows.

4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Condition G.
B3	2052	PIND, required if not performed in screening. (22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
B4	1042	The heating cycle shall be 1 minute minimum.
B5	1042	Condition A; $V_{DS} = 100$ percent of rated; $T_A = +175^\circ\text{C}$, $t = 120$ hours or $T_A = +150^\circ\text{C}$, $t = 240$ hours; read and record $V_{BR(DSS)}$ (pre and post) at $I_D = 1$ mA; read and record I_{DSS} (pre and post), in accordance with table I , subgroup 2.
B5	1042	Condition B; $V_{GS} = 100$ percent of rated $T_A = +175^\circ\text{C}$, $t = 24$ or $T_A = +150^\circ\text{C}$, $t = 48$ hours.
B6	3161	$R_{\theta JC(\text{max})} = 1.67^\circ\text{C/W}$ (not applicable for U3 device)

4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Condition G.
B3	1042	The heating cycle shall be 1 minute minimum.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition A, weight = 10 lbs (4.54 kg), $t = 10$ seconds (TO-257AA package only).
C3	2052	PIND, required if not performed in screening. (JANS only, 22 devices, c = 0 for large lots, 12 devices, c = 0 for small lots).
C5	3161	See 4.3.3 , $R_{\theta JC(\text{max})} = 1.67^\circ\text{C/W}$ (not required if test was performed in group B)
C6	1042	The heating cycle shall be 1 minute minimum. No heat sink nor forced air cooling on the device shall be permitted.

4.4.4 Group D Inspection. Group D inspection shall be conducted in accordance with table E-VIII of [MIL-PRF-19500](#) and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of [MIL-STD-750](#).

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TABLE I. Group A inspection.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3161	See 4.3.3	$Z_{\theta JC}$			°C/W
Breakdown voltage drain to source 2N7380, 2N7380U3 2N7381	3407	$V_{GS} = 0$, $I_D = 1$ mA dc, bias condition C	$V_{(BR)DSS}$	100 200		V dc V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1.0$ mA	$V_{GS(th)1}$	2.0	4.0	V dc
Gate current	3411	$V_{GS} = +20$ V dc, $V_{DS} = 0$, bias condition C	I_{GSSF1}		+100	nA dc
Gate current	3411	$V_{GS} = -20$ V dc, $V_{DS} = 0$, bias condition C	I_{GSSR1}		-100	nA dc
Drain current	3413	$V_{GS} = 0$, $V_{DS} = 80$ percent of rated V_{DS} , bias condition C	I_{DSS1}		25	μA dc
Static drain to source on-state resistance 2N7380, 2N7380U3 2N7381	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$ (see 1.3)	$r_{DS(on)1}$		0.18 0.40	Ω Ω
Static drain to source on-state resistance 2N7380, 2N7380U3 2N7381	3421	$V_{GS} = 12$ V dc, condition A, pulsed (see 4.5.1), $I_D = \text{rated } I_{D1}$ (see 1.3)	$r_{DS(on)2}$		0.20 0.49	Ω Ω
Forward voltage (source drain diode) 2N7380 2N7380U3 2N7381	4011	Condition A, $V_{GS} = 0$, $I_D = \text{rated } I_{D1}$	V_{SD}		1.8 1.5 1.4	V dc V dc V dc

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:						
Gate current	3411	Bias condition C, $V_{GS} = \pm 20$ V dc, $V_{DS} = 0$	I_{GSS2}		± 200	nA dc
Drain current	3413	Bias condition C, $V_{GS} = 0$, $V_{DS} = 80$ percent of rated V_{DS}	I_{DSS2}		0.25	mA dc
Static drain to source on-state	3421	Condition A, $V_{GS} = 12$ V dc, pulsed (see 4.5.1), $I_D = \text{rated } I_{D2}$	$r_{DS(on)3}$			
2N7380, 2N7380U3 2N7381					0.36 0.75	Ω Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1.0$ mA dc	$V_{GS(th)2}$	1.0		V dc
Low temperature operation:						
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = 1.0$ mA dc	$V_{GS(th)3}$		5.0	V dc
<u>Subgroup 4</u>						
Switching time test	3472	$I_D = \text{rated } I_{D1}$, $V_{GS} = 12$ V dc, gate drive impedance = 7.5Ω , $V_{DD} = 50$ percent of $V_{BR(DSS)}$				
Turn-on delay time 2N7380, 2N7381 2N7380U3			$t_{d(on)}$		25 35	ns ns
Rise time 2N7380 2N7380U3 2N7381			t_r		60 75 50	ns ns ns
Turn-off delay time 2N7380, 2N7380U3 2N7381			$t_{d(off)}$		40 70	ns ns
Fall time 2N7380, 2N7380U3 2N7381			t_f		30 60	ns ns

See footnotes at end of table.

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TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Condition		Min	Max	
<u>Subgroup 4</u> - Continued.						
Forward transconductance	3475	$I_D = I_{D2}$, $V_{DD} = 15$ V dc see 4.5.1	g_{fs}	2.5		s
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 5, $t_p = 10$ ms, $V_{DS} = 80$ percent of rated $V_{BR(DSS)}$, $V_{DS} \leq 200$ V maximum				
Electrical measurements		See table I, subgroup 2				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B				
On-state gate charge 2N7380, 2N7380U3 2N7381			$Q_{g(on)}$		40 50	nC nC
Gate to source charge			Q_{gs}		10	nC
Gate to drain charge 2N7380, 2N7380U3 2N7381			Q_{gd}		20 25	nC nC
Reverse recovery time	3473	$di/dt \leq 100$ A/ μ s, $V_{DD} \leq 50$ V, $I_D = I_{D1}$	t_{rr}			
2N7380, 2N7380U3 2N7381					275 460	ns ns

1/ For sampling plan, see MIL-PRF-19500.

2/ For end-point measurements, this test is required for the following subgroups:
Group B, subgroups 3 and 4 (JANS).
Group B, subgroups 2 and 3 (JANTXV).
Group C, subgroup 2 and 6.
Group E, subgroup 1.

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TABLE II. Group D inspection.

Inspection <u>1/ 2/ 3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits				Post-irradiation limits				Unit
	Method	Conditions		M, D, P, L, and R		F, G, and H <u>4/</u>		M, D, P, L, and R		F, G, and H <u>4/</u>		
				Min	Max	Min	Max	Min	Max	Min	Max	
<u>Subgroup 2</u>		T _C = +25°C										
* Steady-state total dose irradiation (V _{GS} bias)	1019	Condition A, V _{GS} = 12 V, V _{DS} = 0										
* Steady-state total dose irradiation (V _{DS} bias)	1019	Condition A, V _{GS} = 0, V _{DS} = 80 percent of rated V _{DS} (pre-irradiation)										
End-point electrical:												
Breakdown voltage, drain to source 2N7380, 2N7380U3 2N7381	3407	V _{GS} = 0, I _D = 1 mA, bias condition C	V _{(BR)DSS}	100 100 200		100 100 200		100 100 200		100 100 200		V dc V dc V dc
Gate to source voltage (threshold) <u>4/</u>	3403	V _{DS} ≥ V _{GS} , I _D = 1 mA	V _{GS(th)}	2.0	4.0	2.0	4.0	2.0	4.0	1.25	4.5	V dc
Gate current	3411	V _{GS} = 20 V, V _{DS} = 0 V, bias condition C	I _{GSSF1}		100		100		100		100	nA dc
Gate current	3411	V _{GS} = -20 V, V _{DS} = 0, bias condition C	I _{GSSR1}		-100		-100		-100		-100	nA dc

See footnotes at end of table.

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TABLE II. Group D inspection - Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbol	Pre-irradiation limits				Post-irradiation limits				Unit
	Method	Conditions		M, D, P, L, and R		F, G, and H <u>4/</u>		M, D, P, L, and R		F, G, and H <u>4/</u>		
				Min	Max	Min	Max	Min	Max	Min	Max	
<u>Subgroup 2</u> - Continued		T _C = +25°C										
Drain current	3413	V _{GS} = 0, bias condition C, V _{DS} = 80 percent of rated V _{DS} (pre- irradiation)	I _{DSS}		25	25		25		50	μA dc	
2N7380, 2N7380U3 2N7381				25	25		25		50	μA dc		
Static drain to source on-state voltage	3405	V _{GS} = 12 V, condition A pulsed, see 4.5.1. I _D = I _{D2}	V _{DS(ON)}		1.638	1.638		1.638		2.184	V dc	
2N7380, 2N7380U3 2N7381				2.4	2.4		2.4		3.18	V dc		
Forward voltage source drain diode	4011	V _{GS} = 0, I _D = I _{D1} , bias condition A	V _{SD}									
2N7380, 2N7380U3 2N7381				1.8	1.8		1.8		1.8	V		
* 2N7380, 2N7380U3 2N7381				1.5	1.5		1.5		1.5	V		
				1.4	1.4		1.4		1.4	V		

1/ For sampling plan, see MIL-PRF-19500.

2/ Separate samples shall be pulled for each bias.

3/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

4/ The "H" designation represents devices which pass end-points at M, D, P, L, R, F, G, and H designated total-ionizing-dose (TID).

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TABLE III. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices, c = 0
Temperature cycling	1051	Test condition G, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 2</u> ^{1/}			45 devices, c = 0
Steady-state reverse bias	1042	Condition A, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
Steady-state gate bias	1042	Condition B, 1,000 hours	
Electrical measurements		See table I , subgroup 2	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 10</u>			22 devices, c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer	
<u>Subgroup 11</u>			3 devices
SEE ^{2/} ^{3/}	1080	See method 1080 of MIL-STD-750 .	

^{1/} A separate sample for each test shall be pulled.

^{2/} Group E qualification of SEE testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

^{3/} Device qualification to a higher level LET is sufficient to qualify all lower level LETs.

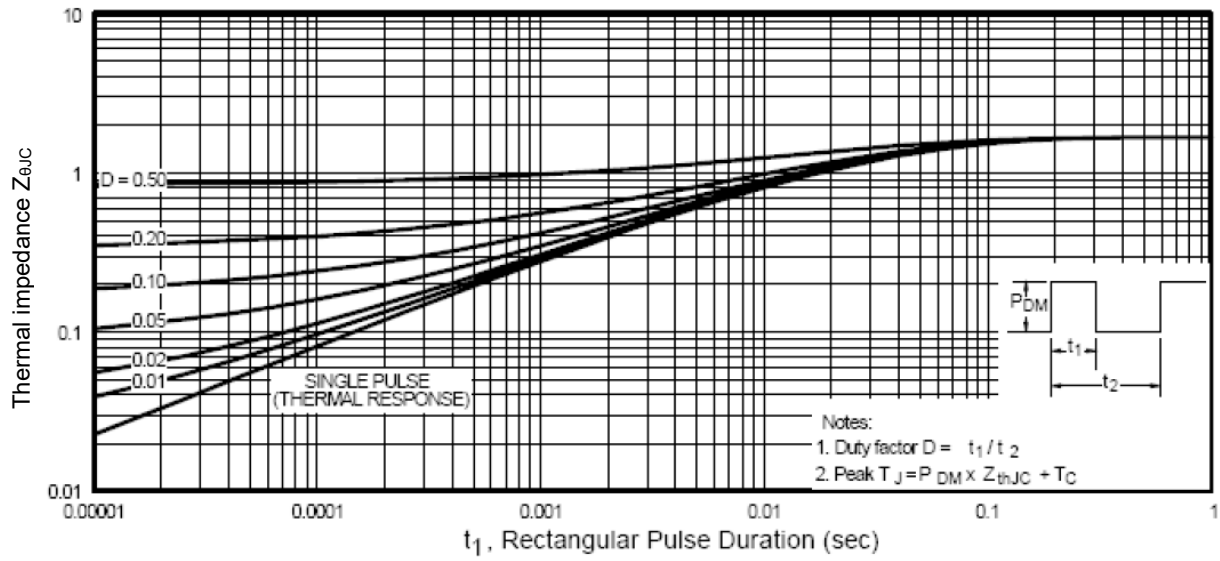
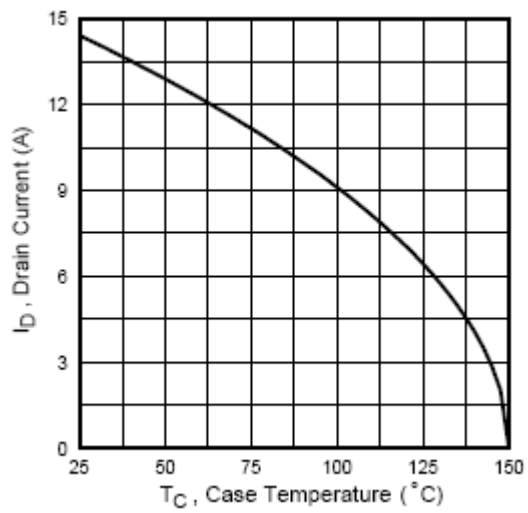


FIGURE 3. Thermal impedance curves.

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2N7380, 2N7380U3



2N7381

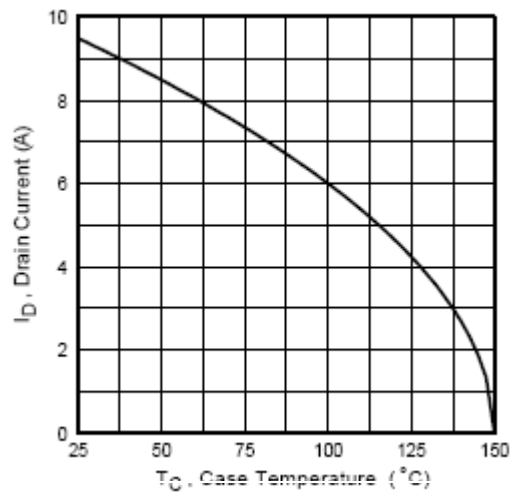
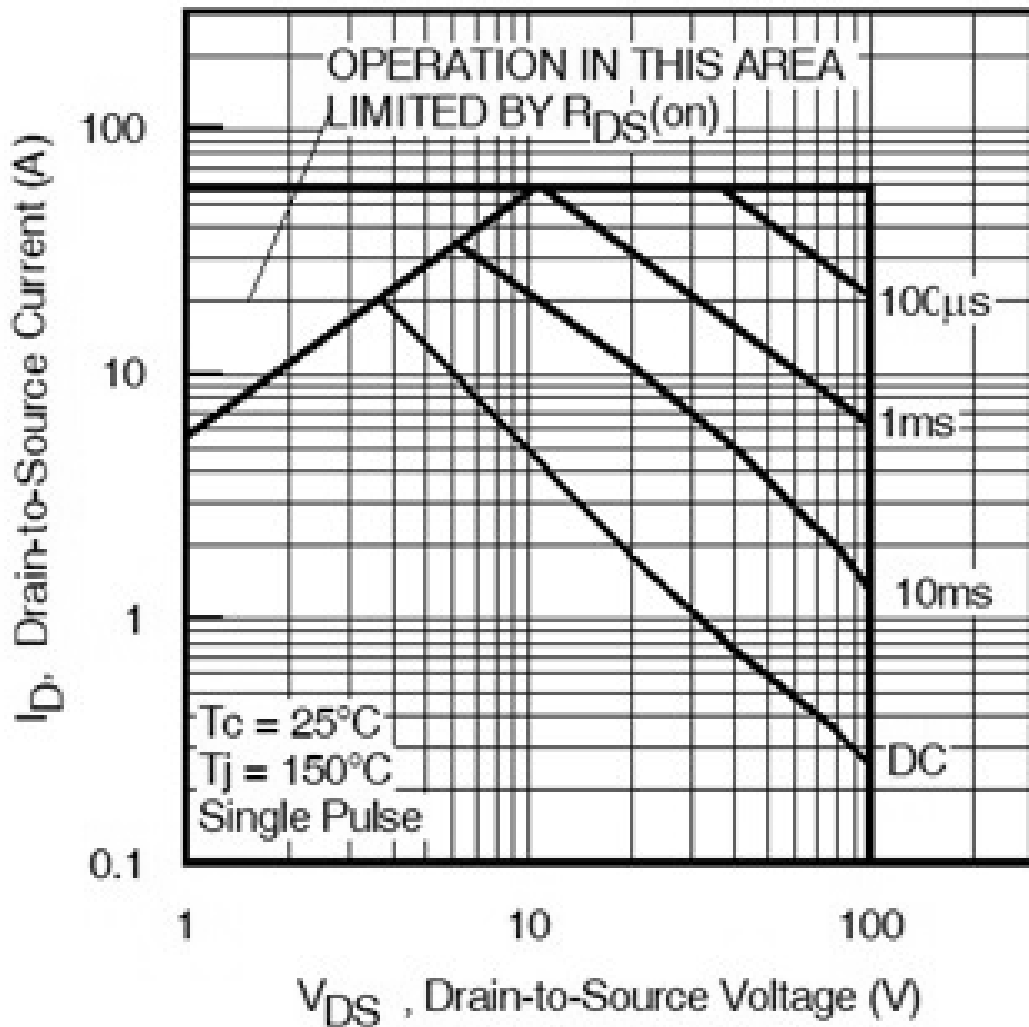
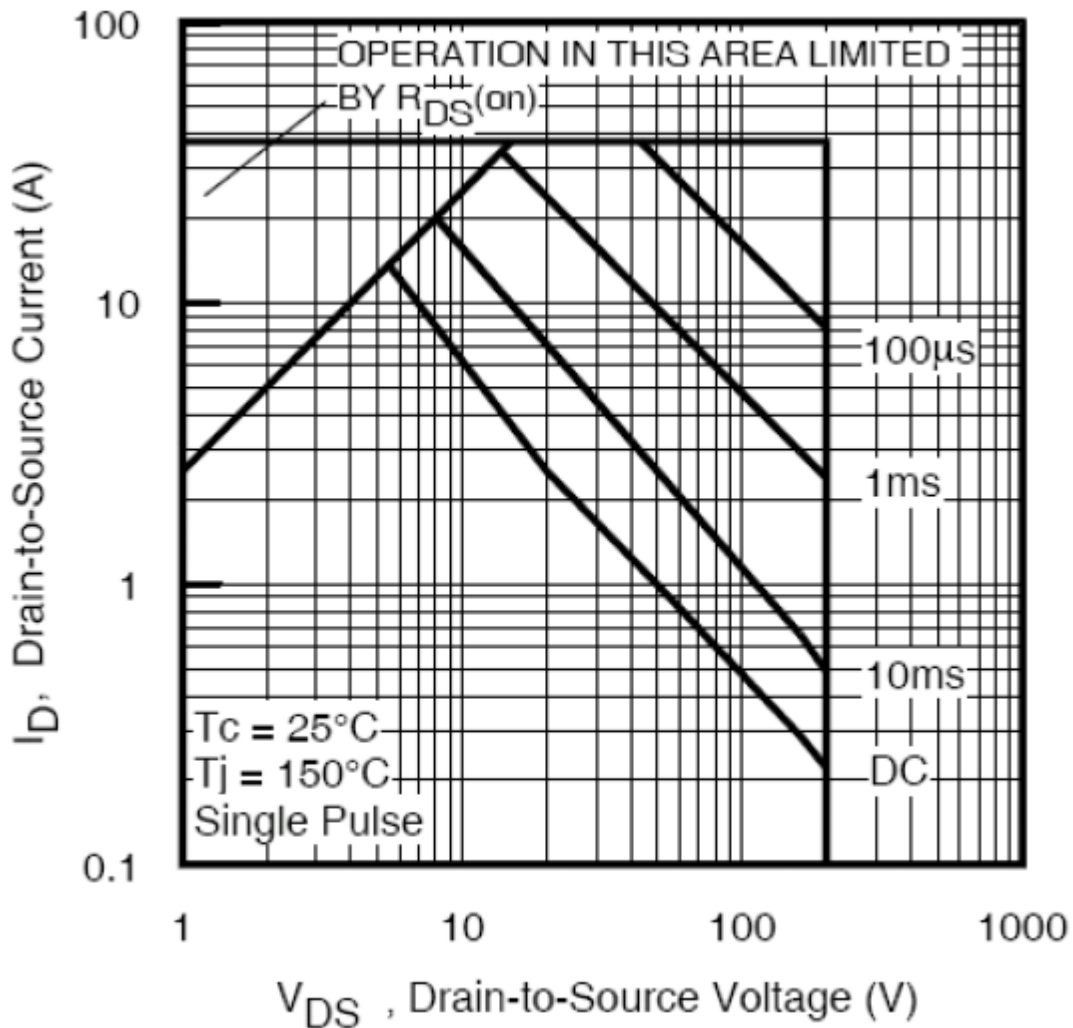


FIGURE 4. Derating drain current graphs.



2N7380, 2N7380U3

* FIGURE 5. Safe operating area graphs.



2N7381

FIGURE 5. Safe operating area graphs - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

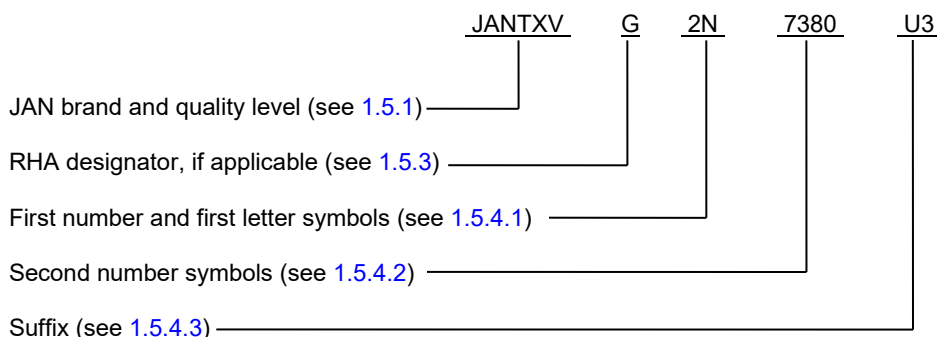
- a. Title, number, and date of this specification.
- b. Packaging requirements (see [5.1](#)).
- c. Lead finish (see [3.4.1](#)).
- d. The complete Part or Identifying Number (PIN), see [1.5](#) and [6.5](#).
- e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If SEE testing data is desired, it should be specified in the contract or order.
- g. If specific SEE characterization conditions are desired (see section [6.8](#) and [table IV](#)), manufacturer's CAGE code should be specified in the contract or order.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 Supersession data. This specification supersedes DESC drawing [89009](#), dated 19 December 1989.

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6.5 PIN construction example. The PINs for encapsulated devices are construction using the following form.



6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7380	JANTXV#2N7380	JANS2N7380	JANS#2N7380
JANTXV2N7380U3	JANTXV#2N7380U3	JANS2N7380U3	JANS#2N7380U3
JANTXV2N7381	JANTXV#2N7381	JANS2N7381	JANS#2N7381

(1) The number sign (#) represent one of eight RHA designators available (M, D, P, L, R, F, G, or H). The PIN is also available without a RHA designator.

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/657](#).

6.8 Application data.

* 6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of [MIL-STD-750](#) method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the [MIL-STD-750](#) method 1080 revision version date and conditions used by each manufacturer for characterization have been listed here (see [table IV](#)) for information only. SEE (SEB and SEGR) conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

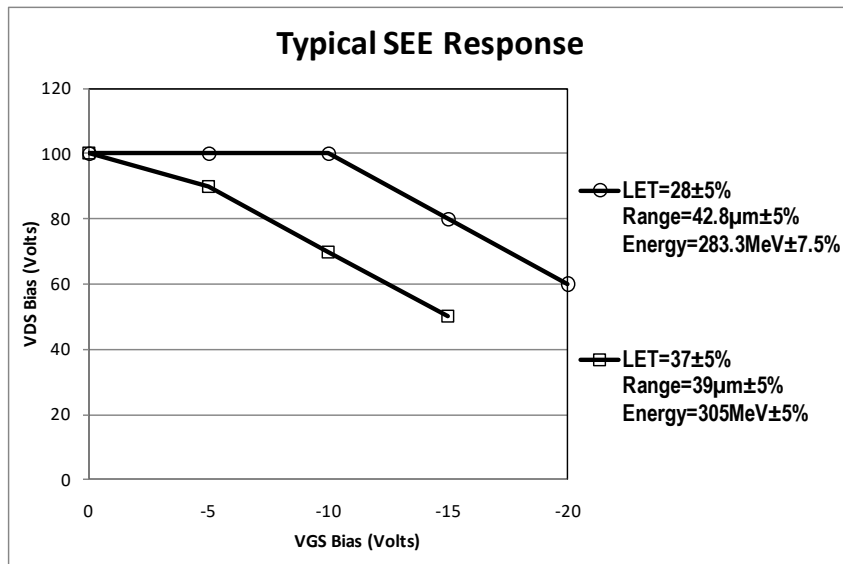
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TABLE IV. Manufacturers characterization conditions.

Manufacturers cage	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of 16 June 1998 and older)	SEE <u>1/</u>	1080	See MIL-STD-750E method 1080.0 dated 20 November 2006. See figure 6	3 devices
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² Flux = $2E3$ to $2E4$ ions/cm ² /sec, temperature = $25^\circ \pm 5$ °C Surface LET = 28 MeV-cm ² /mg $\pm 5\%$, range = $42.8 \mu\text{m} \pm 7.5\%$, Kr ion energy = 283.3 MeV $\pm 7.5\%$	
	2N7380, 2N7380U3		In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 80 \text{ V}$ and $V_{GS} = -15 \text{ V}$ $V_{DS} = 60 \text{ V}$ and $V_{GS} = -20 \text{ V}$ (typical 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
	2N7381		In-situ bias conditions: $V_{DS} = 190 \text{ V}$ and $V_{GS} = 0 \text{ V}$ $V_{DS} = 180 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 170 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 125 \text{ V}$ and $V_{GS} = -15 \text{ V}$ (nominal 4.53 MeV/nucleon at Brookhaven National Lab Accelerator)	
2N7380, 2N7380U3	Surface LET = 37 MeV-cm ² /mg $\pm 5\%$, range = $39 \mu\text{m} \pm 5\%$, Cu ion energy = 305 MeV $\pm 5\%$ In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = 0 \text{ V}$ $V_{DS} = 90 \text{ V}$ and $V_{GS} = -5 \text{ V}$ $V_{DS} = 70 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 50 \text{ V}$ and $V_{GS} = -15 \text{ V}$ (typical 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)			
2N7381	In-situ bias conditions: $V_{DS} = 100 \text{ V}$ and $V_{GS} = -10 \text{ V}$ $V_{DS} = 50 \text{ V}$ and $V_{GS} = -15 \text{ V}$ (typical 3.77 MeV/nucleon at Brookhaven National Lab Accelerator)			
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> <p>Upon qualification, all manufacturers should provide the verification test conditions to be added to this table.</p> </div>				

1/ I_{GSSF1} , I_{GSSR1} , and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias condition. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

2N7380, 2N7380U3



2N7381

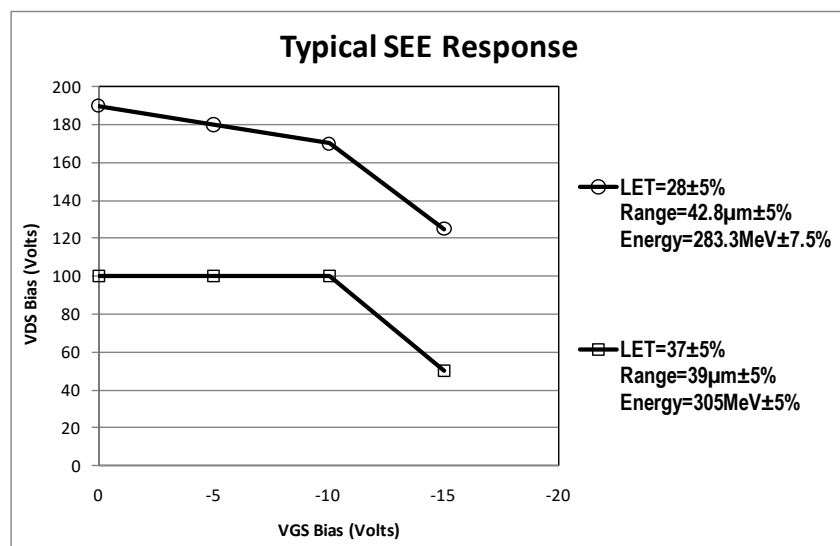


FIGURE 6. Single event effects safe operating area graphs.

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6.9 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@dla.mil or by facsimile (614) 692-6939 or DSN 850-6939.

* 6.10 Amendment notations. The margins of this specification are marked with asterisks to indicate modifications generated by this amendment. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - SH
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2021-092)

Review activities:

Army - SM
Navy - AS, MC, OS
Air Force - 19

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.