

The documentation and process conversion measures necessary to comply with this revision shall be completed by 23 March 2016.

INCH-POUND

MIL-PRF-19500/527F  
 23 December 2015  
 SUPERSEDING  
 MIL-PRF-19500/527E  
 22 February 2010

PERFORMANCE SPECIFICATION SHEET

\* TRANSISTOR, DARLINGTON, PNP, SILICON, POWER, ENCAPSULATED (THROUGH-HOLE MOUNT PACKAGE) TYPES 2N6648, 2N6649, AND 2N6650, QUALITY LEVELS JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

\* 1.1 Scope. This specification covers the performance requirements for PNP silicon, Darlington power transistors. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each encapsulated device.

\* 1.2 Package outlines. The device package outlines are as follows: TO-3 in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings unless otherwise specified  $T_A = +25^\circ\text{C}$ .

Types	$P_T$ (1) $T_A = +25^\circ\text{C}$	$P_T$ (2) $T_C = +25^\circ\text{C}$	$V_{CBO}$	$V_{CEO}$	$V_{EBO}$	$I_B$	$I_C$	$T_J$ and $T_{STG}$	$R_{\theta JC}$
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>°C</u>	<u>°C/W</u>
2N6648	5.0	85	-40	-40	-5.0	-0.25	-10	-65 to +175	1.76
2N6649	5.0	85	-60	-60	-5.0	-0.25	-10	-65 to +175	1.76
2N6650	5.0	85	-80	-80	-5.0	-0.25	-10	-65 to +175	1.76

(1) Derate linearly 33.3 mW/°C above  $T_A > +25^\circ\text{C}$ .

(2) Derate linearly 567 mW/°C above  $T_C > +25^\circ\text{C}$ .

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.4 Primary electrical characteristics.

	$h_{FE1}$ (1)	$h_{FE2}$ (1)	$V_{CE(SAT)1}$ (1)	$V_{CE(SAT)2}$ (1)	$V_{BE(ON)1}$ (1)
	$V_{CE} = -3$ V dc $I_C = -1$ A dc	$V_{CE} = -3$ V dc $I_C = -5$ A dc	$I_C = -5.0$ A dc $I_B = -10$ mA dc	$I_C = -10$ A dc $I_B = -0.1$ A dc	$V_{CE} = -3.0$ V dc $I_C = -5.0$ A dc
Minimum	300	1,000	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>
Maximum		20,000	-2.0	-3.0	-2.8

	$C_{obo}$	$ h_{fe} $	Pulse response	
	$V_{CB} = 10$ V dc $I_E = 0$ $100$ kHz $\leq f \leq 1$ MHz	$V_{CE} = -5.0$ V dc $I_C = -1.0$ A dc $f = 1$ MHz	$t_{on}$	$t_{off}$
Minimum	<u>pF</u>	30	<u><math>\mu</math>S</u>	<u><math>\mu</math>S</u>
Maximum	300	400	2.5	10.0

(1) Pulsed (see 4.5.1).

- \* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- \* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".
- \* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
- \* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
- \* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "6648", "6649" and "6650".
- \* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on [QPDSIS-19500](#).

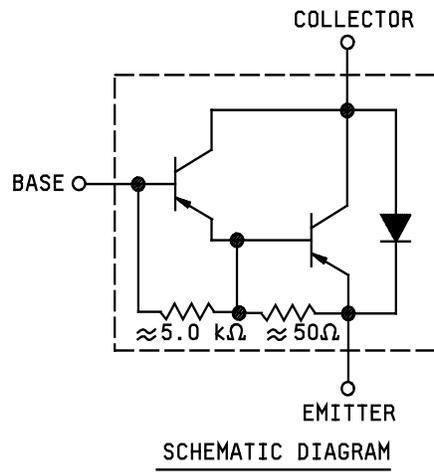
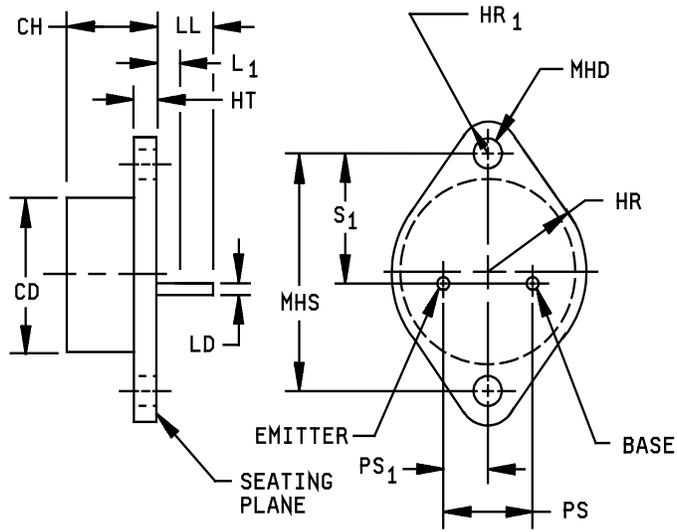


FIGURE 1. Dimensions and configuration (TO-3).

## MIL-PRF-19500/527F

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.23	
CH	.250	.450	6.35	11.43	
HR	.495	.525	12.57	13.34	
HR <sub>1</sub>	.131	.188	3.33	4.78	
HT	.050	.135	1.27	3.43	
LD	.038	.043	0.97	1.09	
LL	.312	.500	7.92	12.70	
L <sub>1</sub>		.050		1.27	
MHD	.151	.161	3.84	4.09	
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	3
PS <sub>1</sub>	.205	.225	5.21	5.72	3
s <sub>1</sub>	.655	.675	16.64	17.15	

## NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) and .055 inch (1.40 mm) below seating plane. When gauge is not used measurement will be made at the seating plane.
4. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
5. Mounting holes shall be deburred on the seating plane side.
6. Collector is electrically connected to the case.
7. In accordance with AMSE Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 1. Dimensions and configuration (TO-3) - Continued.

## 2. APPLICABLE DOCUMENTS

- \* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- \* (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

$R_{\theta JC}$  Thermal resistance junction to case.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.6 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.7 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

\* 4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (table E-IV) of MIL-PRF-19500.	Measurement
	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.2)
7	Optional
11	$I_{CEX1}$ and $h_{FE1}$
12	See 4.3.1
13	Subgroup 2 of table I herein; $\Delta I_{CEX1}$ = 100 percent of initial value or -2 $\mu$ A dc, whichever is greater. $\Delta h_{FE1}$ = $\pm$ 25 percent of initial value.
14	Required

(1) May be performed anytime before screen 9.

4.3.1 Burn-in conditions.  $T_J = 162.5 \pm 12.5^\circ\text{C}$ , 2N6648 =  $V_{CB} = -30$  V dc, 2N6649 =  $V_{CB} = -40$  V dc, 2N6650 =  $V_{CB} = -60$  V dc.

- \* 4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of [MIL-STD-750](#) using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$  ( $V_C$  and  $V_H$  where appropriate). See [table II](#), group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#), and as specified herein.

- \* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of [MIL-PRF-19500](#), and [table I](#) herein.
- \* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB of [MIL-PRF-19500](#) and herein.
- \* 4.4.2.1 Quality levels JAN, JANTX and JANTXV, table E-VIB of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
-----------------	---------------	-------------------

- |      |      |   |
|------|------|---|
| * B3 | 1037 | For solder die attach: $V_{CB} \geq -10$ V dc, $T_A \leq 35^\circ\text{C}$ .  |
| B3   | 1026 | For eutectic die attach: $V_{CB} \geq -10$ V dc, $T_A \leq 35^\circ\text{C}$ adjust $P_T$ to achieve $T_J = 150^\circ\text{C}$ minimum. |
| B6   | 1032 | $T_{STG} = + 175^\circ\text{C}$   |
- \* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
-----------------	---------------	-------------------

- |      |      |  |
|------|------|--|
| * C2 | 2036 | Test condition A, weight = 10 pounds (4.5 kg), $t = 15$ s.                 |
| C5   | 3131 | $R_{\theta JC} = 1.76^\circ\text{C/W}$ . See <a href="#">4.3.2</a> herein. |
- \* C6
 1037 | For solder die attach:  $V_{CB} \geq -10$  V dc,  $T_A \leq 35^\circ\text{C}$ . |
  - C6
 1026 | For eutectic die attach:  $V_{CB} \geq -10$  V dc,  $T_A \leq 35^\circ\text{C}$  adjust  $P_T$  to achieve  $T_J = 150^\circ\text{C}$  minimum. |

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection.

\*

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2</u> /	3131	See 4.3.2	$Z_{\theta JX}$			$^{\circ}\text{C/W}$
Collector – emitter breakdown voltage	3011	Bias condition D; $I_C = -200$ mA dc pulsed (see 4.5.1).	$V_{(BR)CEO}$	-40 -60 -80		V dc
2N6648 2N6649 2N6650						
Collector - emitter breakdown voltage	3011	Bias condition B; $I_C = -200$ mA dc $R_{BB} = 100$ ohms, pulsed (see 4.5.1).	$V_{(BR)CER}$	-40 -60 -80		V dc
2N6648 2N6649 2N6650						
Collector - emitter cutoff current	3041	Bias condition D	$I_{CEO}$		-1	mA dc
2N6648 2N6649 2N6650		$V_{CE} = -40$ V dc $V_{CE} = -60$ V dc $V_{CE} = -80$ V dc				
Emitter - base cutoff current	3061	Bias condition D; $V_{EB} = -5$ V dc	$I_{EBO}$		-10	mA dc
* Collector - emitter cutoff current	3041	Bias condition A; $V_{BE} = +1.5$ V dc	$I_{CEX1}$		-10	$\mu\text{A}$ dc
2N6648 2N6649 2N6650		$V_{CE} = -40$ V dc $V_{CE} = -60$ V dc $V_{CE} = -80$ V dc				
* Collector - base cutoff current	3036	Bias condition D	$I_{CBO}$		-1	mA dc
2N6648 2N6649 2N6650		$V_{CB} = -40$ V dc $V_{CB} = -60$ V dc $V_{CB} = -80$ V dc				

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Base - emitter voltage (non- saturated)	3066	Test condition B; $V_{CE} = -3.0$ V dc, $I_C = -5.0$ A dc; pulsed (see 4.5.1)	$V_{BE(on)1}$		-2.8	V dc
Base - emitter voltage (non- saturated)	3066	Test condition B; $V_{CE} = -3.0$ V dc, $I_C = -10$ A dc; pulsed (see 4.5.1)	$V_{BE(on)2}$		-4.5	V dc
Collector - emitter saturated voltage	3071	$I_C = -5.0$ A dc; $I_B = -10$ mA dc	$V_{CE(sat)1}$		-2.0	V dc
Collector - emitter saturated voltage	3071	$I_C = -10$ A dc; $I_B = -0.1$ A dc, pulsed (see 4.5.1)	$V_{CE(sat)2}$		-3.0	V dc
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc; $I_C = -1.0$ A dc pulsed (see 4.5.1)	$h_{FE1}$	300		
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc; $I_C = -5$ A dc pulsed (see 4.5.1)	$h_{FE2}$	1,000	20,000	
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc; $I_C = -10$ A dc pulsed (see 4.5.1)	$h_{FE3}$	100		
<u>Subgroup 3</u>						
High - temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current	3041	Bias condition A; $V_{BE} = +1.5$ V dc	$I_{CEX2}$		-3.0	mA dc
2N6648		$V_{CE} = -40$ V dc				
2N6649		$V_{CE} = -60$ V dc				
2N6650		$V_{CE} = -80$ V dc				
Low - temperature operation:		$T_A = -65^\circ\text{C}$				
Forward - current transfer ratio	3076	$V_{CE} = -3.0$ V dc $I_C = -5.0$ A dc pulsed (see 4.5.1)	$h_{FE4}$	200		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Pulse response:	3251	Test condition A, except test circuit and pulse requirements in accordance with <a href="#">figure 2</a> .				
Turn-on time		$V_{CE} = -30$ V dc; $I_C = -5.0$ A dc; $I_{B1} = -20$ mA dc	$t_{on}$		2.5	$\mu$ s
Turn-off time		$V_{CE} = -30$ V dc; $I_C = -5.0$ A dc; $I_{B1} = -I_{B2} = 20$ mA dc	$t_{off}$		10.0	$\mu$ s
Magnitude of small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = -5.0$ V dc; $I_C = -1.0$ A dc, $f = 1.0$ MHz	$ h_{fe} $	30	400	
Open circuit output capacitance	3236	$V_{CB} = 10$ V dc, $I_E = 0$ , $100$ kHz $\leq f \leq 1$ MHz	$C_{obo}$		300	pF
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = 25^\circ$ C; $t = 1$ s; 1 cycle; (see <a href="#">figure 3</a> )				
Test 1		$V_{CE} = 8.5$ V dc; $I_C = -10$ A dc				
Test 2		$V_{CE} = 25$ V dc; $I_C = -3.4$ A dc				
Test 3		$V_{CE} = -40$ V dc; $I_C = -0.9$ A dc				
2N6648		$V_{CE} = -60$ V dc; $I_C = -0.3$ A dc				
2N6649		$V_{CE} = -80$ V dc; $I_C = -0.14$ A dc				
2N6650						
Electrical measurements		See <a href="#">table 1</a> , subgroup 2				
Safe operating area (switching)	3053	Load condition C (unclamped inductive load) (see <a href="#">figure 4</a> ); $T_C = +25^\circ$ C; duty cycle $\leq 10$ percent; $R_s \leq 0.1$ ohms.				
Test 1		$t_p = 1$ ms; (vary to obtain $I_C$ ); $R_{BB1} = 1$ k ohms; $V_{BB1} = -10$ V dc; $R_{BB2} = \infty$ ; $V_{BB2} = 0$ ; $I_C = -10$ A dc; $V_{CC} = -30$ V dc; $R_L = 0.5$ ohms; $L = 0.25$ mH at 10 A dc				
Test 2		$t_p = 1$ ms; (vary to obtain $I_C$ ); $R_{BB1} = 10$ k ohms; $V_{BB1} = -10$ V dc; $R_{BB2} = \infty$ ; $V_{BB2} = 0$ ; $I_C = -0.2$ A dc; $V_{CC} = -30$ V dc; $R_L = 0.5$ ohms; $L = 20$ mH at 0.2 A dc				

See footnotes at end of table.

\*

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> - Continued Safe operating area (switching)  2N6648 2N6649 2N6650  Electrical measurements  <u>Subgroups 6 and 7</u>  Not applicable		Load condition B (clamped inductive load) (see <a href="#">figure 5</a> ); $T_A = +25^\circ\text{C}$ ; $t_r + t_f \leq 1.0 \mu\text{s}$ ; duty cycle $\leq 10$ percent; $t_p = 5 \text{ ms}$ ; (vary to obtain $I_C$ ); $R_s = 0.1 \text{ ohms}$ ; $V_{CC} = -10 \text{ V dc}$ ; $I_C = -10 \text{ A dc}$  Clamp voltage = -40 V dc Clamp voltage = -60 V dc Clamp voltage = -80 V dc Device fails if clamp voltage not reached.  See <a href="#">table I</a> , subgroup 2				

1/ For sampling plan see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:

Group B, subgroups 2 and 3.

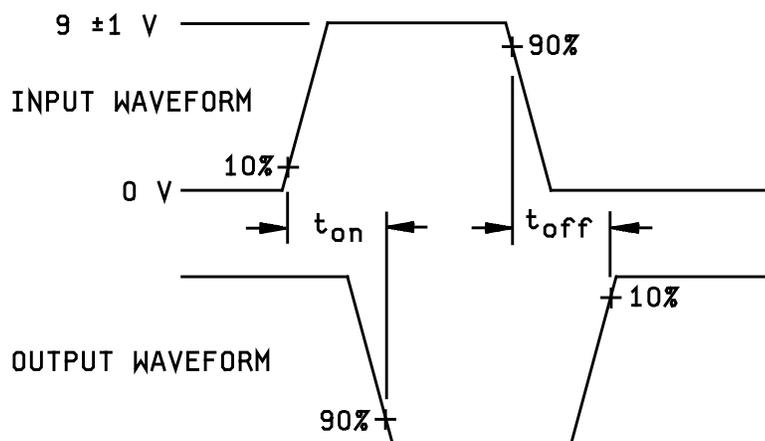
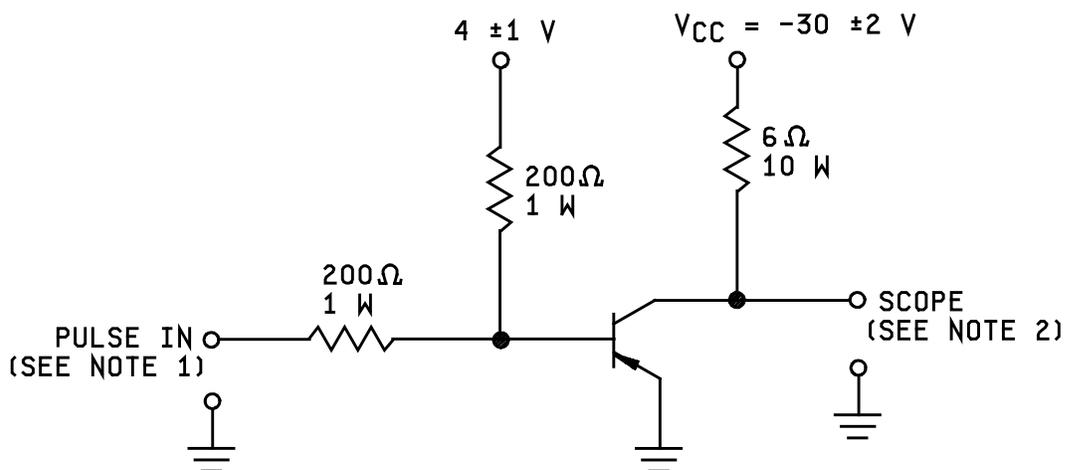
Group C, subgroups 2 and 6.

Group E, subgroup 1.

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\* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
DC blocking life	1048	T <sub>A</sub> = +150°C, V <sub>CB</sub> = 80 percent of rated voltage, 1,000 hours.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See <a href="#">MIL-PRF-19500</a> .	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	



## NOTES:

1. The rise time ( $t_r$ ) and fall time ( $t_f$ ) of the applied pulse shall be each  $< 20\ \text{ns}$ ; duty cycle  $< 2$  percent; generator source impedance shall be  $50\ \Omega$ ; pulse width =  $20\ \text{ns}$ .
2. Output sampling oscilloscope:  $Z_{IN} > 100\ \text{k}\Omega$ ;  $C_{IN} < 50\ \text{pF}$ ; rise time  $< 20\ \text{ns}$ .

FIGURE 2. Pulse response test circuit.

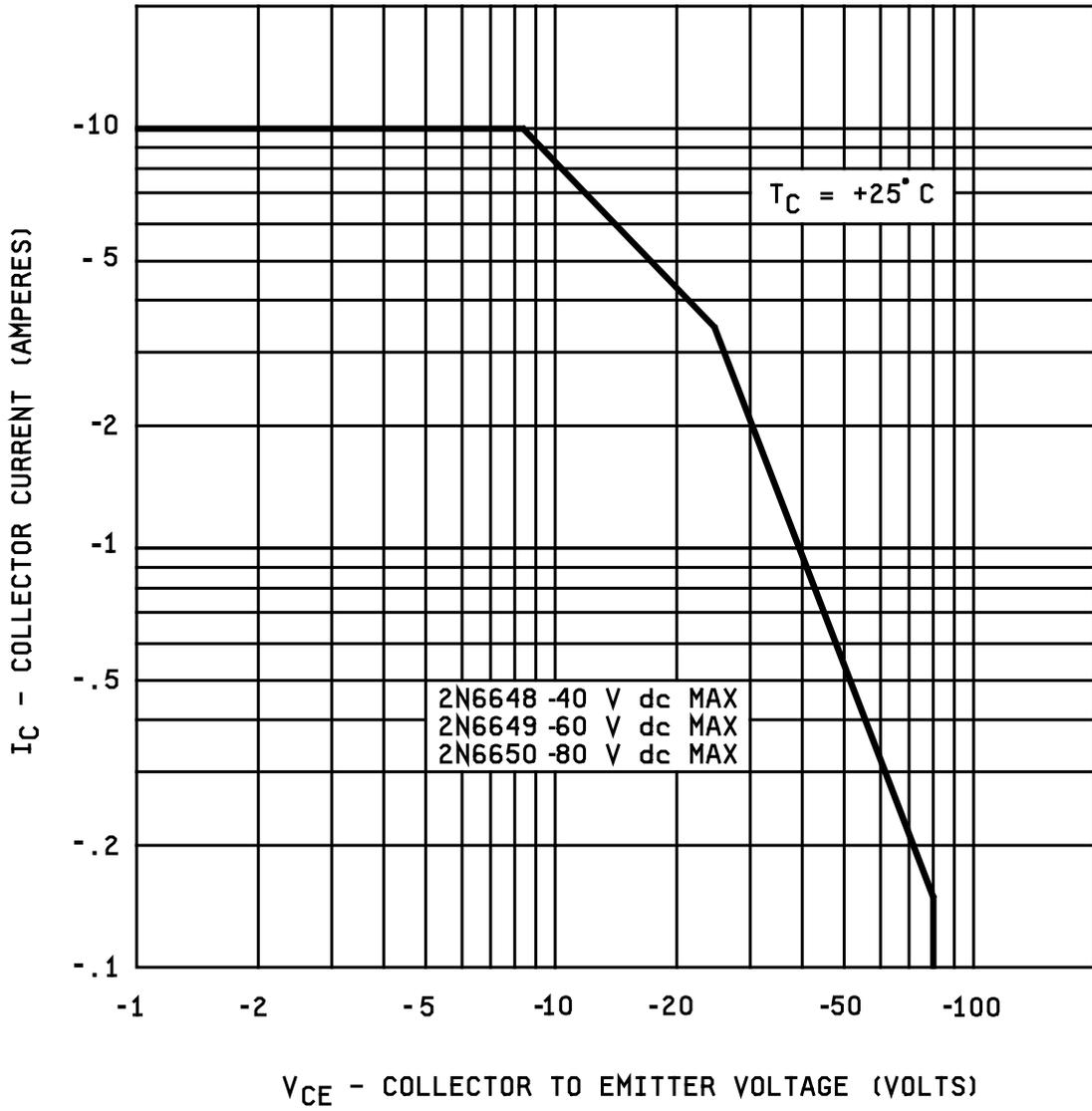


FIGURE 3. Maximum safe operating area graph (continuous dc).

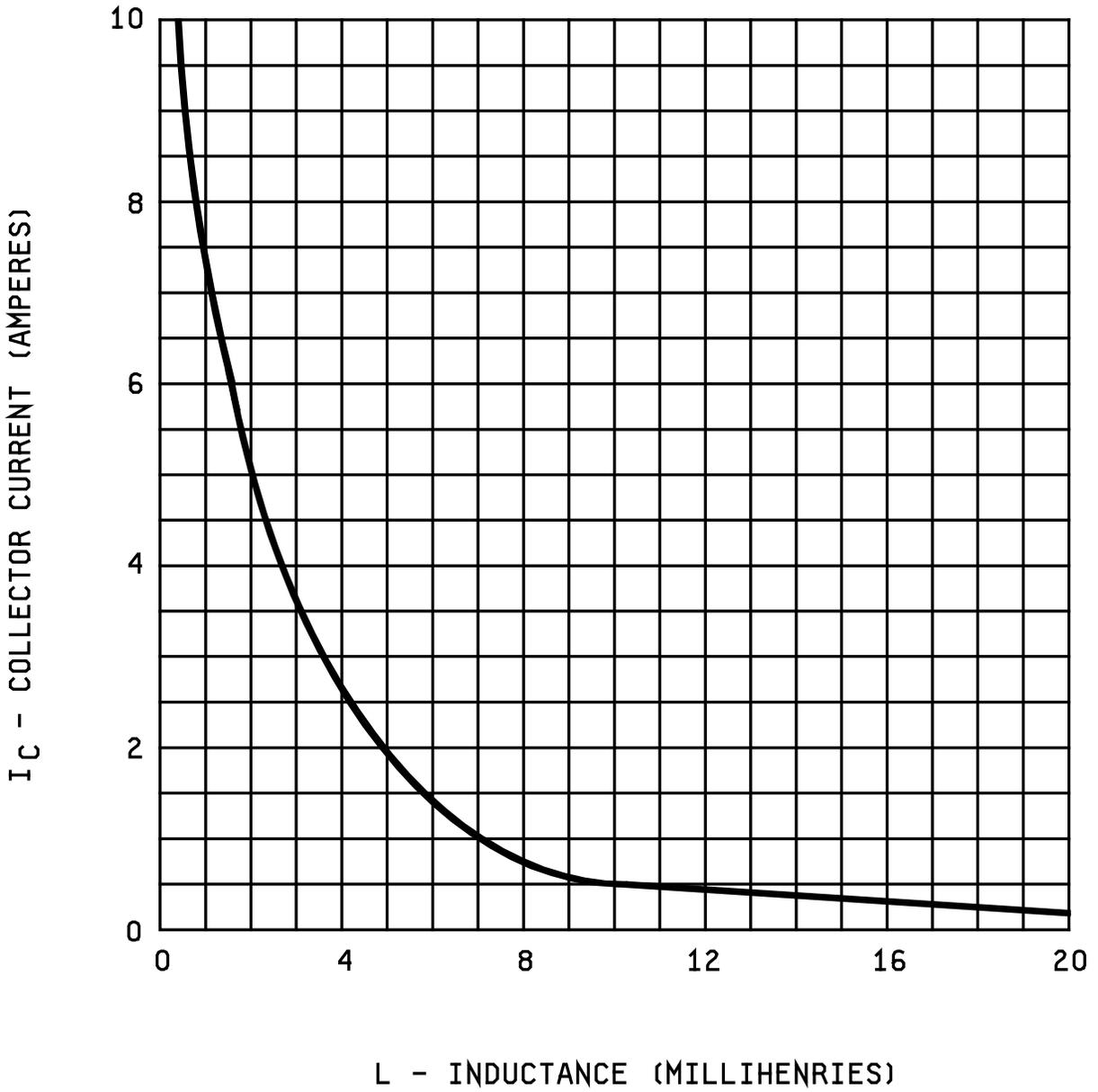
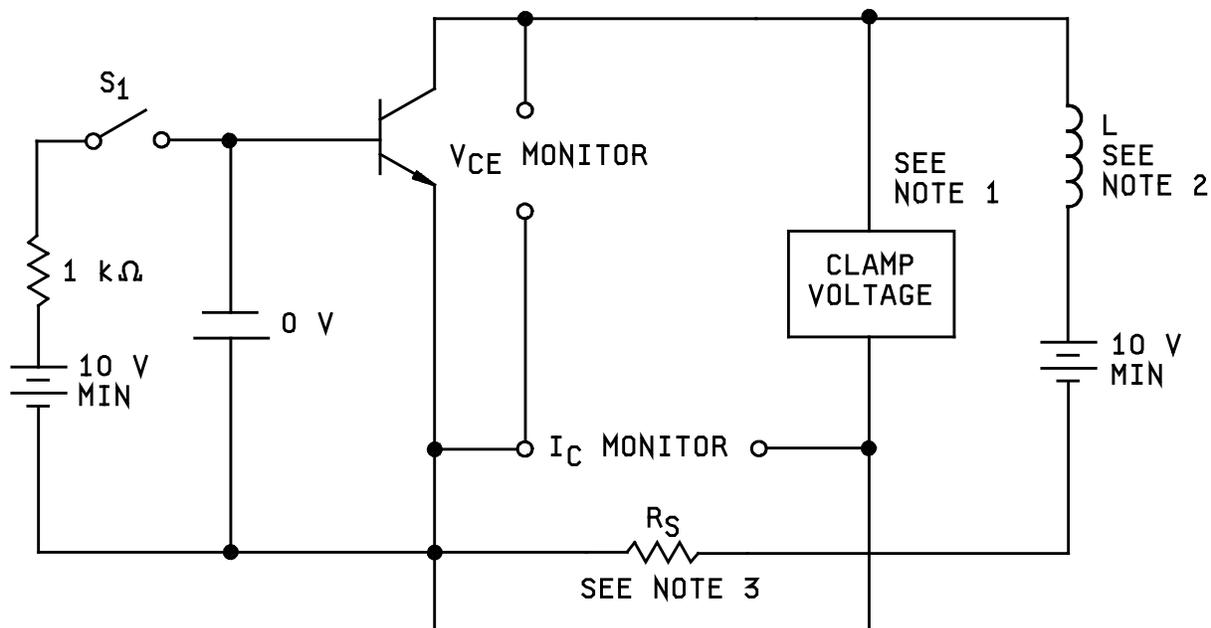


FIGURE 4. Safe operating area for switching between saturation and cutoff (unclamped inductive load).



## Procedures:

1. With switch S1 closed, set the specified test conditions.
2. Open S1. Device fails if clamp voltage not reached and maintained until the current returns to zero.
3. Perform specified end-point tests.

## NOTES:

1. Either a clamping circuit or clamping diode may be used.
2. The coil used shall provide a minimum inductance of 0.25 mH at 10 A with a maximum dc resistance of 0.1Ω.
3.  $R_S \leq 0.1\Omega$ . 12 W, 1 percent tolerance maximum (noninductive).

FIGURE 5. Clamped inductive sweep test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

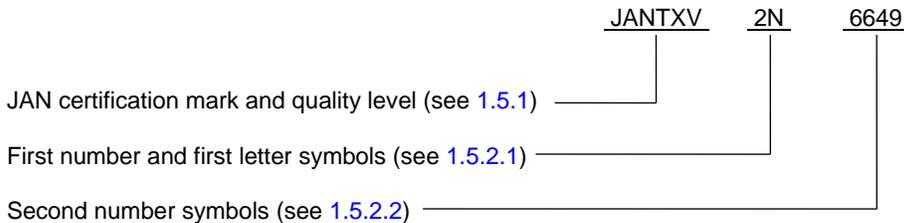
- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).

\* d. The complete PIN, see 1.5 and 6.5.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 PIN construction example.

\* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



\* 6.5 List of PINs.

\* 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN2N6648	JANTX2N6648	JANTXV2N6648
JAN2N6649	JANTX2N6649	JANTXV2N6649
JAN2N6650	JANTX2N6650	JANTXV2N6650

\* 6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218–3990 or by electronic mail at [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil) or by facsimile (614) 693-1642 or DSN 850-6939.

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:  
 Army - CR  
 Navy - EC  
 Air Force - 85  
 NASA - NA  
 DLA - CC

Preparing activity:  
 DLA - CC  
 (Project 5961-2016-005)

Review activities:  
 Navy - MC  
 Air Force - 19

\* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.