

The documentation and process conversion measures necessary to comply with this revision shall be completed by 19 March 2015.

INCH POUND

MIL-PRF-19500/505F  
 19 January 2015  
 SUPERSEDING  
 MIL-PRF-19500/505E  
 22 July 2009

PERFORMANCE SPECIFICATION SHEET

\* TRANSISTOR, PNP, DARLINGTON, SILICON, POWER, DEVICE TYPES 2N6286 AND 2N6287, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

\* 1.1 Scope. This specification covers the performance requirements for PNP, Darlington, power transistors for use in particular power-switching applications. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

\* 1.2 Package outlines. The device package outlines are as follows: similar to TO-3 in accordance with [figure 1](#) for all encapsulated device types.

1.3 Maximum ratings at  $T_C = +25^\circ\text{C}$  unless otherwise specified.

Type	$P_T$		$R_{\theta JC}$	$V_{CBO}$	$V_{CEO}$	$V_{EBO}$	$I_C$	$I_B$	$T_J$ and $T_{STG}$
	$T_C = +25^\circ\text{C}$ (1)	$T_C = +100^\circ\text{C}$							
	<u>W</u>	<u>W</u>	<u><math>^\circ\text{C/W}</math></u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u><math>^\circ\text{C}</math></u>
2N6286	175	87.5	0.855	-80	-80	-7	-20	-0.5	-65 to +175
2N6287	175	87.5	0.855	-100	-100	-7	-20	-0.5	-65 to +175

(1) Derate linearly at 1.16 W/ $^\circ\text{C}$  above  $T_C > +25^\circ\text{C}$ .

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.4 Primary electrical characteristics.

Limit	$h_{FE2}$ (1) $V_{CE} = -3$ V dc $I_C = -10$ A dc	$h_{FE3}$ (1) $V_{CE} = -3$ V dc $I_C = -20$ A dc	$V_{CE(sat)1}$ $I_C = -20$ A dc $I_B = -200$ mA dc	$V_{CE(sat)2}$ $I_C = -10$ A dc $I_B = -40$ mA dc	$V_{BE(sat)}$ $I_C = -20$ A dc $I_B = -200$ mA dc	Switching	
						$t_{on}$	$t_{off}$
Min	1,250	300	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>μs</u>	<u>μs</u>
Max	18,000		-3.0	-2.0	-4.0	2	10

Limit	$C_{obo}$ $V_{CB} = -10$ V dc $I_E = 0$ $100$ kHz $\leq f \leq 1$ MHz	$h_{fe}$ $V_{CE} = -3$ V dc $I_C = -10$ A dc $f = 1$ kHz	$ h_{fe} $ $V_{CE} = -3$ V dc $I_C = -10$ A dc $f = 1$ MHz
Max	400		80

(1) Pulsed (see 4.5.1).

- \* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- \* 1.5.1 JAN brand and quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".
- \* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
- \* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".
- \* 1.5.2.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "6286" and "6287".



Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.23	3
CH	.250	.360	6.35	9.14	
HR	.495	.525	12.57	13.34	
HR <sub>1</sub>	.131	.188	3.33	4.78	
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	5, 9
LL	.312	.500	7.92	12.7	5
L <sub>1</sub>		.050		1.27	5, 9
MHD	.151	.165	3.84	4.19	7
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	4
PS <sub>1</sub>	.205	.225	5.21	5.72	
S <sub>1</sub>	.655	.675	16.64	17.15	

FIGURE 1. Physical dimensions (similar to TO-3) - Continued.

## 2. APPLICABLE DOCUMENTS

- \* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- \* (Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

- \* 3.4.2 Pin-out. The pin-out of the device types shall be as shown on [figure 1](#). Terminal 1 is the emitter, terminal 2 is base. The collector shall be electrically connected to the case.

3.5 Marking. Devices shall be marked in accordance with [MIL-PRF-19500](#).

3.6 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in [table I](#).

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I and II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening. Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#), and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurements
	JANTX and JANTXV levels
(1) 3c	Thermal impedance method 3131 of MIL-STD-750 (see <a href="#">4.3.2</a> )
7	Optional
11	$I_{CEX1}$ and $h_{FE1}$
12	See <a href="#">4.3.1</a>
13	Subgroup 2 of <a href="#">table I</a> herein; $\Delta I_{CEX1}$ = 100 percent of initial value or 2 $\mu$ A dc, whichever is greater; $\Delta h_{FE1}$ = $\pm$ 40 percent of initial value
14	Required

- (1) Shall be performed anytime after temperature cycling, screen 3a of 4.3 herein; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:  $T_J = +162.5^\circ\text{C} \pm 12.5^\circ\text{C}$ ,  $V_{CE} \geq -10$  V dc. NOTE: No heat sink or forced air cooling on the devices shall be permitted.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{SW}$  ( $V_C$  and  $V_H$  where appropriate). Measurement delay time ( $t_{MD}$ ) = 70  $\mu\text{s}$  max.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

	<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
*	B3	1037	For solder die attach: $V_{CB} \geq -10$ V dc; $T_A \leq +35^\circ\text{C}$ .
	B3	1027	For eutectic die attach: $T_A \leq +35^\circ\text{C}$ adjust $P_T$ to achieve $T_J = +150^\circ\text{C}$ minimum, $V_{CB} \geq -10$ V dc.
	B5	3131	$R_{\theta JC} = 0.855^\circ\text{C/W}$ (maximum).

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500.

	<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
	C2	2036	Tension: Test condition A; weight = 10 lbs; time = 15 s.
*	C6	1037	For solder die attach: $V_{CB} \geq -10$ V dc; $T_A \leq 35^\circ\text{C}$ .
	C6	1026	For eutectic die attach: $T_A \leq +35^\circ\text{C}$ adjust $P_T$ to achieve $T_J = +150^\circ\text{C}$ minimum, $V_{CB} \geq -10$ V dc.

\* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

\* 4.5.1 Pulse response measurements. Conditions for pulse response measurement shall be as specified in section 4 of MIL-STD-750.

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TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector - emitter 2N6286 2N6287	3011	Bias condition D; $I_C = -100$ mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-80 -100		V dc V dc
Collector - emitter cutoff current 2N6286 2N6287	3041	Bias condition A; $V_{BE} = +1.5$ V dc  $V_{CE} = -80$ V dc $V_{CE} = -100$ V dc	$I_{CEX1}$		10	$\mu$ A
Collector - emitter cutoff current 2N6286 2N6287	3041	Bias condition D  $V_{CE} = -40$ V dc $V_{CE} = -50$ V dc	$I_{CEO}$		-1.0	mA dc
Emitter - base cutoff current	3061	Bias condition D; $V_{EB} = -7$ V dc	$I_{EBO}$		-2.5	mA dc
Base - emitter (nonsaturated)	3066	Test condition B; $V_{CE} = -3$ V dc; $I_C = -10$ A dc	$V_{BE}$		-2.8	V dc
Base - emitter voltage (saturated)	3066	Test condition A; $I_C = -20$ A dc; $I_B = -200$ mA dc; pulsed (see 4.5.1)	$V_{BE(sat)}$		-4.0	V dc
Collector - emitter saturated voltage	3071	$I_C = -20$ A dc; $I_B = -200$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		-3.0	V dc
Collector - emitter saturated voltage	3071	$I_C = -10$ A dc; $I_B = -40$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		-2.0	V dc
Forward-current transfer ratio	3076	$V_{CE} = -3$ V dc; $I_C = -1$ A dc; pulsed (see 4.5.1)	$h_{FE1}$	1,500		
Forward-current transfer ratio	3076	$V_{CE} = -3$ V dc; $I_C = -10$ A dc; pulsed (see 4.5.1)	$h_{FE2}$	1,250	18,000	
Forward-current transfer ratio	3076	$V_{CE} = -3$ V dc; $I_C = -20$ A dc; pulsed (see 4.5.1)	$h_{FE3}$	300		

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High-temperature operation:		$T_A = +150^\circ\text{C}$				
Collector - emitter cutoff current	3041	Bias condition A; $V_{BE} = +1.5\text{ V dc}$ ;	$I_{CEX2}$		-5.0	mA dc
2N6286 2N6287		$V_{CE} = -80\text{ V dc}$ $V_{CE} = -100\text{ V dc}$				
Collector - emitter saturated voltage	3071	$I_C = -10\text{ A dc}$ ; $I_B = -40\text{ mA dc}$ ; pulsed (see 4.5.1)	$V_{CE(sat)3}$		-2.0	V dc
Low-temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = -3\text{ V dc}$ ; $I_C = -10\text{ A dc}$ ; pulsed (see 4.5.1)	$h_{FE4}$	150		
<u>Subgroup 4</u>						
Pulse response:	3251	Test condition A, except test circuit and pulse requirements in accordance with figure 2.				
Turn-on time		$V_{CC} = -30\text{ V dc}$ ; $I_C = -10\text{ A dc}$ ; $I_B = -40\text{ mA dc}$	$t_{on}$		2.0	$\mu\text{s}$
Turn-off time		$V_{CC} = -30\text{ V dc}$ ; $I_C = -10\text{ A dc}$ ; $I_{B1} = I_{B2} = -40\text{ mA dc}$	$t_{off}$		10	$\mu\text{s}$
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = -3\text{ V dc}$ ; $I_C = -10\text{ A dc}$ ; $f = 1.0\text{ MHz}$	$ h_{fe} $	8	80	
Small-signal short-circuit forward-current transfer ratio	3206	$V_{CE} = -3\text{ V dc}$ ; $I_C = -10\text{ A dc}$ ; $f = 1.0\text{ kHz}$	$h_{fe}$	300		
Open circuit output capacitance	3236	$V_{CB} = -10\text{ V dc}$ ; $I_E = 0$ ; $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$C_{obo}$		400	pF

See footnote at end of table.

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TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}$ ; $t = 1 \text{ s}$ ; 1 cycle; (see <a href="#">figure 3</a> )				
<u>Test 1</u>		$V_{CE} = -8.75 \text{ V dc}$ ; $I_C = -20 \text{ A dc}$				
<u>Test 2</u>		$V_{CE} = -30 \text{ V dc}$ ; $I_C = -5.8 \text{ A dc}$				
<u>Test 3</u>						
2N6286		$V_{CE} = -80 \text{ V dc}$ ; $I_C = -100 \text{ mA dc}$				
2N6287		$V_{CE} = -100 \text{ V dc}$ ; $I_C = -100 \text{ mA dc}$				
Electrical measurements		See <a href="#">table I</a> , subgroup 2				
Safe operating area (switching)	3053	Load condition C; (unclamped inductive load); (see <a href="#">figure 4</a> ) $T_A = +25^\circ\text{C}$ ; $R_s \leq 0.1 \ \Omega$ ; $t_r + t_f \leq 15 \text{ ns}$ ; duty cycle $\leq 2$ percent				
<u>Test 1</u>		$t_p = 80 \ \mu\text{s}$ ; (vary to obtain $I_C$ ); $R_{BB1} \geq 50 \ \Omega$ ; $V_{BB1} \geq -10 \text{ V dc}$ ; $R_{BB2} = \infty$ ; $V_{BB2} = 0$ ; $I_C = -20 \text{ A dc}$ ; $V_{CC} \geq -50 \text{ V dc}$ ; The coil used shall provide a minimum inductance of 1 mH at 20 A. (For reference only; two coils in parallel (Super Electric Corporation type S16884 or equivalent).)				
<u>Test 2</u>		$t_p = 1 \text{ ms}$ ; (vary to obtain $I_C$ ); $R_{BB1} \geq 50 \ \Omega$ ; $V_{BB1} \geq -10 \text{ V dc}$ ; $R_{BB2} = \infty$ ; $V_{BB2} = 0$ ; $I_C = -500 \text{ mA dc}$ ; $V_{CC} \geq -50 \text{ V dc}$ ; The coil used shall provide a minimum inductance of 100 mH at 500 mA. (For reference only; two coils in series, 80 mH and 20 mH windings (Triad C-48u or equivalent).)				
Electrical measurements		See <a href="#">table I</a> , subgroup 2				

See footnote at end of table.

TABLE I. Group A inspection - Continued.

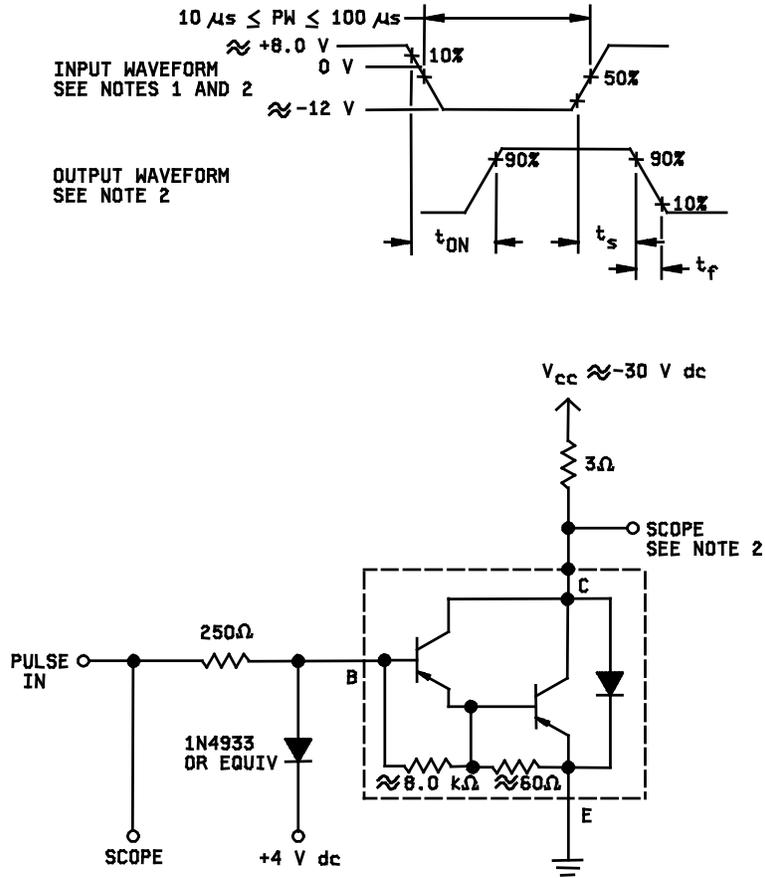
Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> Safe operating area (switching)  2N6286 2N6287  Electrical measurements  <u>Subgroups 6 and 7</u> Not applicable	3053	Load condition B; (clamped inductive load); $T_A = +25^\circ\text{C}$ ; $R_s = 0.1 \Omega$ ; $t_r + t_f \leq 1.0 \mu\text{s}$ ; duty cycle $\leq 2$ percent; $t_p = 1 \text{ ms}$ (vary to obtain $I_C$ ); $R_{BB1} = 50 \Omega$ ; $V_{BB1} = -10 \text{ V dc}$ ; $R_{BB2} = 100 \Omega$ ; $V_{BB2} = +1.5 \text{ V dc}$ ; $V_{CC} = -25 \text{ V dc}$ ; $I_C = -20 \text{ A dc}$ ; $R_L \leq 2 \Omega$ ; $L = 5 \text{ mH}$ ; (Four coils in parallel, 20 mH windings (Triad C-48u or equivalent)).  Clamp voltage = 80 +0, -5 V dc Clamp voltage = 100 +0, -5 V dc  Device fails if clamp voltage is not reached  See <a href="#">table I</a> , subgroup 2				

1/ For sampling plan, see [MIL-PRF-19500](#).

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\* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification and large lot quality conformance inspection
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition C, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071		
End-point electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} \geq 10$ V dc, 6,000 cycles.	
<u>Subgroup 4</u>			
Thermal impedance curves		See table E-IX of <a href="#">MIL-PRF-19500</a> , group E, subgroup 4.	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics:  $t_r \leq 20$  ns,  $t_f \leq 20$  ns,  $Z_{out} = 50 \Omega$ , PW = 23  $\mu\text{s}$ , duty cycle  $\leq 2$  percent.
2. The output waveform is monitored on a sampling oscilloscope with  $Z_{in} \geq 20$  M $\Omega$ ,  $C_{in} \leq 11.5$  pF,  $t_r \leq 2$  ns.
3. Resistors shall be noninductive types.
4. The dc power supplies may require additional by-passing in order to minimize ringing.

FIGURE 2. Pulse response test circuit.

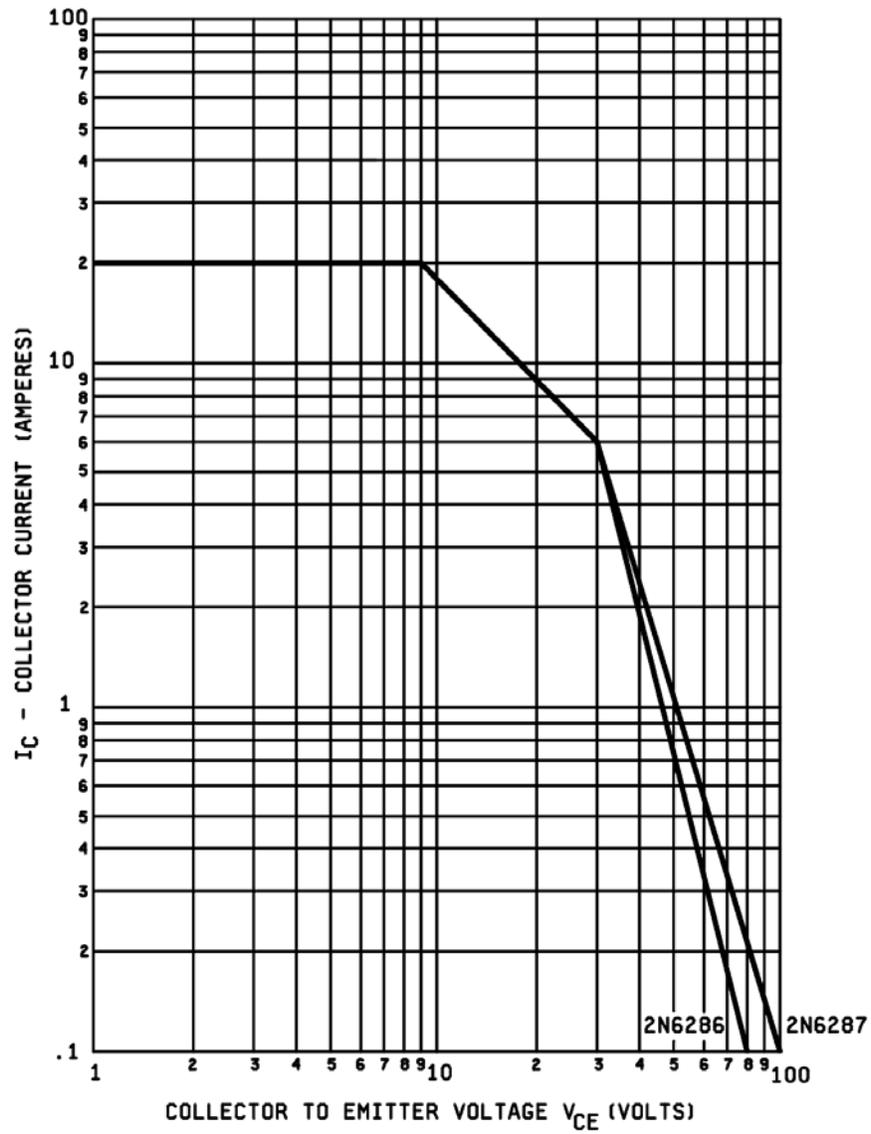


FIGURE 3. Maximum safe operating area (continuous dc).

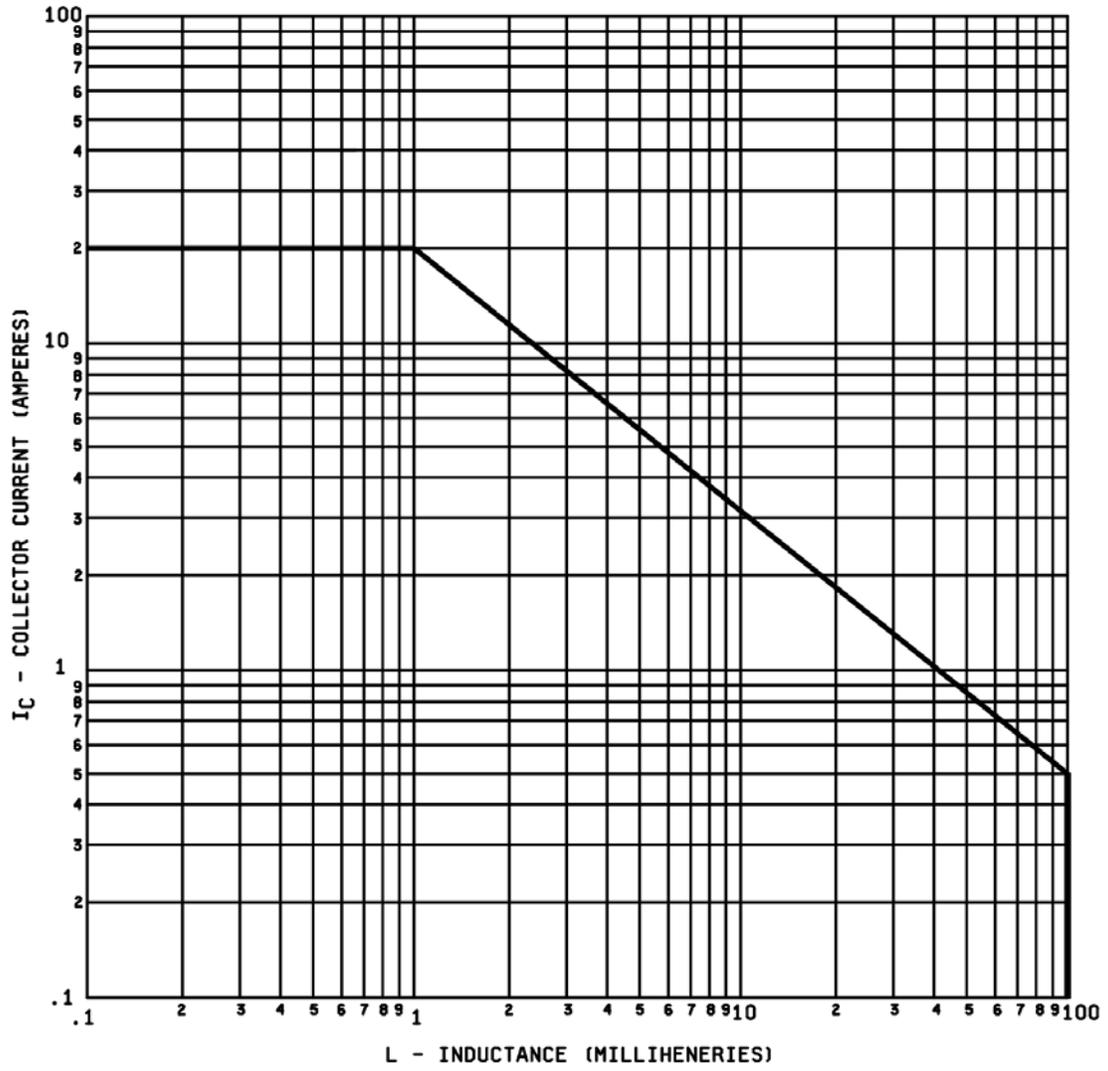


FIGURE 4. Safe operating area for switching between saturation and cutoff (unclamped inductive load).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

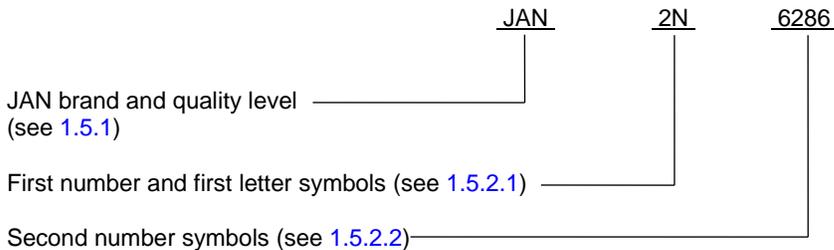
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- \* d. The complete Part or Identifying Number (PIN), see 1.5 and 6.4.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



- \* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN2N6286	JANTX2N6286	JANTXV2N6286
JAN2N6287	JANTX2N6287	JANTXV2N6287

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodian:  
Air Force - 85  
NASA - NA  
DLA - CC

Preparing activity:  
DLA - CC

(Project 5961-2014-129)

Review activities:  
Air Force - 19, 99

- \* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.