

The documentation and process conversion measures necessary to comply with this revision shall be completed by 13 March 2014.

INCH-POUND

MIL-PRF-19500/476F
 13 December 2013
 SUPERSEDING
 MIL-PRF-19500/476E
 23 January 2012

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, FIELD EFFECT TRANSISTORS, P-CHANNEL, SILICON,
 TYPES 2N5114 THROUGH 2N5116 AND 2N5114UB THROUGH 2N5116UB,
 JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for P-channel, junction, silicon field-effect transistors. Three levels of product assurance are provided for each device type as specified in [MIL-PRF-19500](#).

1.2 Physical dimensions. See [figure 1](#) (similar to TO-18) and [figure 2](#) (UB, surface mount).

1.3 Maximum ratings. $T_A = +25^\circ\text{C}$, unless otherwise specified.

P_T (1) $T_A = +25^\circ\text{C}$	V_{GS} (2)	V_{DS}	V_{DG} (2)	I_G	T_{STG}
<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>°C</u>
0.500	30	30	30	50	-65 to +200

- (1) Derate linearly 3.0 mW/°C for $T_A = +25^\circ\text{C}$.
- (2) Symmetrical geometry allows operation of those units with source/drain leads interchanged.

1.4 Primary electrical characteristics.

Limits	I_{DSS} (1)			$V_{DS(on)}$		
	$V_{DS} = -18\text{ V dc}$ $V_{GS} = 0$	$V_{DS} = -15\text{ V dc}$ $V_{GS} = 0$	$V_{DS} = -15\text{ V dc}$ $V_{GS} = 0$	$I_D = -15\text{ mA dc}$ $V_{GS} = 0$	$I_D = -7\text{ mA dc}$ $V_{GS} = 0$	$I_D = -3\text{ mA dc}$ $V_{GS} = 0$
	2N5114 2N5114UB	2N5115 2N5115UB	2N5116 2N5116UB	2N5114 2N5114UB	2N5115 2N5115UB	2N5116 2N5116UB
	<u>mA dc</u>	<u>mA dc</u>	<u>mA dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>
Min	-30	-15	-5.0	-1.3	-0.8	-0.6
Max	-90	-60	-25			

See notes on next page.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

* 1.4 Primary electrical characteristics - Continued.

Limits	$V_{GS(off)}$			$r_{ds(on)2}$		
	$V_{DS} = 15 \text{ V dc}$ $I_D = -1.0 \text{ nA dc}$			$V_{GS} = 0, I_D = 0$ $f = 1 \text{ kHz}$		
	2N5114 2N5114UB	2N5115 2N5115UB	2N5116 2N5116UB	2N5114 2N5114UB	2N5115 2N5115UB	2N5116 2N5116UB
	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>Ω</u>	<u>Ω</u>	<u>Ω</u>
Min	5	3	1			
Max	10	6	4	75	100	175

(1) For $T_A > +25^\circ\text{C}$, derate linearly 1.67 mW/ $^\circ\text{C}$ one section, 2.67 mW/ $^\circ\text{C}$ both sections.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

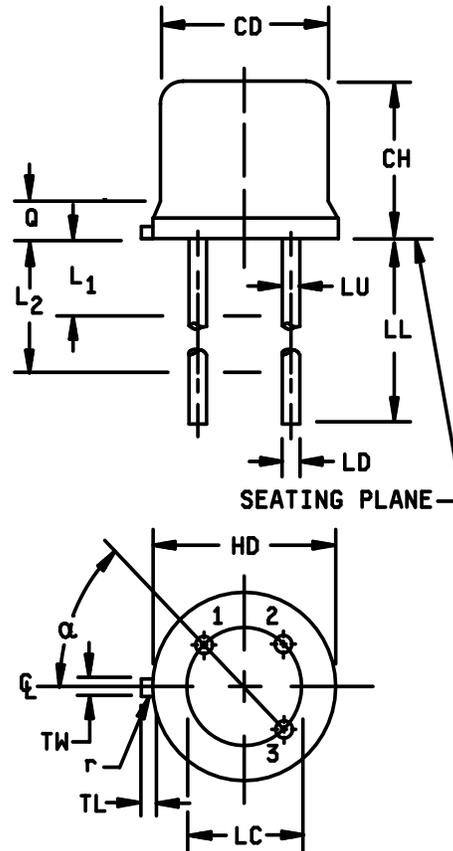
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <http://quicksearch.dla.mil/> or <https://assist.dla.mil/> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.7	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L ₁		.050		1.27	7,8
L ₂	.250		6.35		7,8
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	
r		.010		0.25	10
α	45° TP		45° TP		6

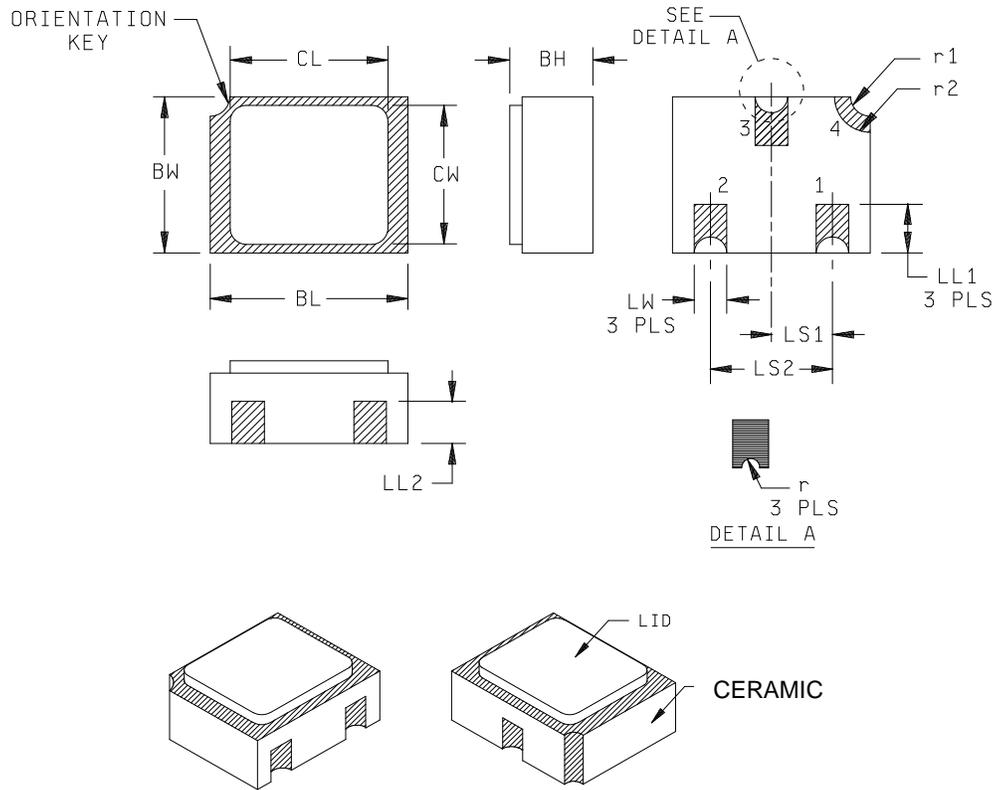


NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L₁ and L₂. Dimension LD applies between L₂ and LL minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. All three leads.
9. The gate shall be electrically connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.
12. Lead 1 = source, lead 2 = gate, lead 3 = drain.

FIGURE 1. Physical dimensions (similar to TO-18).

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Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
BH	.046	.056	1.17	1.42	
BL	.115	.128	2.92	3.25	
BW	.085	.108	2.16	2.74	
CL		.128		3.25	
CW		.108		2.74	
LL1	.022	.038	0.56	0.96	
LL2	.017	.035	0.43	0.89	
LS1	.036	.040	0.91	1.02	
LS2	.071	.079	1.81	2.01	
LW	.016	.024	0.41	0.61	
r		.008		.203	
r1		.012		.305	
r2		.022		.559	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas (tungsten with gold plating 60 micro inches min over 80 micro inches min nickel).
4. Pad 1 = drain, Pad 2 = source, Pad 3 = gate, Pad 4 = shielding connected to the lid.

FIGURE 2. Physical dimensions, surface mount (UB version).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figures 1](#) (similar to TO-18) and [2](#) (UB, surface mount) herein.

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#), except for the UB suffix package. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturers symbol or logo. The prefixes JAN, JANTX, and JANTXV can be abbreviated as J, JX, and JV respectively. The "2N" prefix and the "UB" suffix can also be omitted.

3.6 Electrostatic discharge protection. The devices covered by this specification require electrostatic protection.

3.6.1 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of electrostatic charge. The following handling practices shall be followed:

- a. Devices shall be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent, if practical.
- g. Care shall be exercised, during test and troubleshooting, to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.7 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.8 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4 VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement
	JANTX and JANTXV levels
9 and 10	Not applicable
11	$I_{D(off)1}$, $r_{ds(on)1}$
12	See 4.3.1
13	Subgroup 2 of table I herein; $\Delta I_{D(off)1} = \pm 0.5 \text{ nA dc}$ or ± 100 percent of initial value, whichever is greater. $\Delta r_{ds(on)1} = \pm 20$ percent of initial value.

4.3.1 Power burn-in. Power burn-in conditions are in accordance with method 1039 of MIL-STD-750, condition A and as follows: $T_A = +150^\circ\text{C}$; $V_{GS} = 24 \text{ V dc}$; $V_{DS} = 0$.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and 4.4.2.1 herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV of MIL-PRF-19500).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1027	$V_{GS} = 24 \text{ V dc}; T_A = +125^\circ\text{C}; V_{DS} = 0.$
B6	1032	$T_A = +175^\circ\text{C}.$

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	1056	Thermal shock: Test condition C, time at temperature extremes = 15 minutes minimum.
C2	2036	Lead fatigue: Test condition E (not applicable to UB suffix devices.)
C6	1026	$V_{GS} = 24 \text{ V dc}; T_A = +125^\circ\text{C}; V_{DS} = 0.$

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in [table II](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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* TABLE I. Group A inspection.

Inspection 1/ <u>Subgroup 1</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Gate to source breakdown voltage	3401	Bias condition C; $I_G = 1.0 \mu\text{A dc}$; $V_{DS} = 0$	$V_{(BR)GSS}$	30		V dc
Gate reverse current	3411	Bias condition C; $V_{GS} = 20 \text{ V dc}$; $V_{DS} = 0$	I_{GSS}		500	pA dc
Drain cutoff current 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB	3413	Bias condition A $V_{DS} = -15 \text{ V dc}$; $V_{GS} = 12 \text{ V dc}$ $V_{DS} = -15 \text{ V dc}$; $V_{GS} = 7.0 \text{ V dc}$ $V_{DS} = -15 \text{ V dc}$; $V_{GS} = 5.0 \text{ V dc}$	$I_{D(off)1}$		-500 -500 -500	pA dc pA dc pA dc
Zero-gate-voltage drain current 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB	3413	Bias condition C; V_{DS} to be pulsed see 4.5.1 $V_{DS} = -18 \text{ V dc}$; $V_{GS} = 0$ $V_{DS} = -15 \text{ V dc}$; $V_{GS} = 0$ $V_{DS} = -15 \text{ V dc}$; $V_{GS} = 0$	I_{DSS}	-30 -15 -5.0	-90 -60 -25	mA dc mA dc mA dc
* Drain to source on voltage 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB	3405	Bias condition B $I_D = -15 \text{ mA dc}$; $V_{GS} = 0$ $I_D = -7.0 \text{ mA dc}$; $V_{GS} = 0$ $I_D = -3.0 \text{ mA dc}$; $V_{GS} = 0$	$V_{DS(on)}$		-1.3 -0.8 -0.6	V dc V dc V dc
Gate to source cutoff voltage 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB	3403	$V_{DS} = -15 \text{ V dc}$; $I_D = -1.0 \text{ nA dc}$ $V_{DS} = -15 \text{ V dc}$; $I_D = -1.0 \text{ nA dc}$ $V_{DS} = -15 \text{ V dc}$; $I_D = -1.0 \text{ nA dc}$	$V_{GS(off)}$	5.0 3.0 1.0	10 6.0 4.0	V dc V dc V dc
Small-signal drain to source on resistance 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB	3423	$V_{GS} = 0$; $I_D = -1 \text{ mA dc}$	$r_{ds(on)1}$		75 100 175	Ω Ω Ω
Small-signal drain to source on resistance 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB	3423	$V_{GS} = 0$; $I_D = 0$; $f = 1 \text{ kHz}$	$r_{ds(on)2}$		75 100 175	Ω Ω Ω

See footnote at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:						
Gate reverse current	3411	$T_A = +150^\circ\text{C}$ Bias condition C, $V_{GS} = 20\text{ V dc}; V_{DS} = 0$	I_{GSS}		1.0	$\mu\text{A dc}$
Drain cutoff current	3413	Bias condition A; $V_{GS} = 12\text{ V dc}; V_{DS} = -15\text{ V dc}$ $V_{GS} = 7.0\text{ V dc}; V_{DS} = -15\text{ V dc}$ $V_{GS} = 5.0\text{ V dc}; V_{DS} = -15\text{ V dc}$	$I_{D(off)2}$		-1.0	$\mu\text{A dc}$
2N5114, 2N5114UB					-1.0	$\mu\text{A dc}$
2N5115, 2N5115UB					-1.0	$\mu\text{A dc}$
2N5116, 2N5116UB					-1.0	$\mu\text{A dc}$
<u>Subgroup 4</u>						
Small-signal common-source short-circuit input capacitance	3431	$V_{DS} = -15\text{ V dc}; V_{GS} = 0$ $f = 1\text{ MHz}$	C_{iss}			
2N5114, 2N5114UB					25	pF
2N5115, 2N5115UB					25	pF
2N5116, 2N5116UB					27	pF
Small-signal common-source short-circuit reverse transfer capacitance	3433		C_{rss}			
2N5114, 2N5114UB		$V_{DS} = 0; V_{GS} = 12\text{ V dc}$			7.0	pF
2N5115, 2N5115UB		$V_{DS} = 0; V_{GS} = 7.0\text{ V dc}$			7.0	pF
2N5116, 2N5116UB		$V_{DS} = 0; V_{GS} = 5.0\text{ V dc}$			7.0	pF
Turn-on delay time	3459	See figure 3	$t_{d(on)}$			
2N5114, 2N5114UB					6	ns
2N5115, 2N5115UB					10	ns
2N5116, 2N5116UB					25	ns
Rise time	3459	See figure 3	t_r			
2N5114, 2N5114UB					10	ns
2N5115, 2N5115UB					20	ns
2N5116, 2N5116UB					35	ns
Turn-off delay time	3459	See figure 3	$t_{d(off)}$			
2N5114, 2N5114UB					6	ns
2N5115, 2N5115UB					8	ns
2N5116, 2N5116UB					20	ns

See footnote at end of table

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* TABLE I. Group A inspection - Continued.

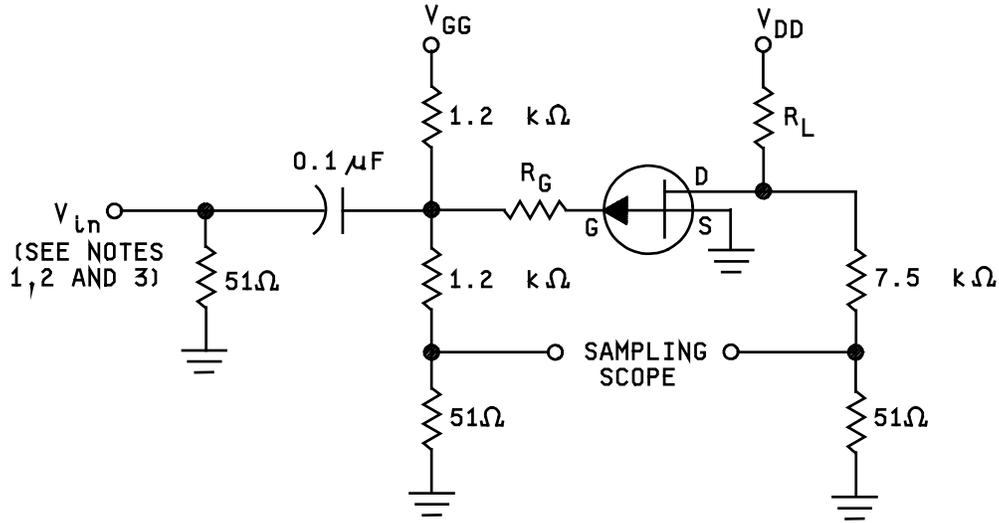
Inspection ^{1/}	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u> - Continued Fall time 2N5114, 2N5114UB 2N5115, 2N5115UB 2N5116, 2N5116UB <u>Subgroups 5 and 6</u> Not applicable	3459	See figure 3	t _f		15 30 60	ns ns ns

^{1/} For sampling plan, see [MIL-PRF-19500](#).

TABLE II. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u> Temperature cycling Hermetic seal Fine leak Gross leak Electrical measurements <u>Subgroup 2</u> ^{1/} Blocking life Electrical measurements <u>Subgroups 4 and 5</u> Not applicable	 1051 1071 1048 	 -55°C to +150°C, 500 cycles See table I , subgroup 2 1,000 hours minimum, T _A = +150°C, V _{DG} or V _{GS} = 80 percent of rated. See table I , subgroup 2 	45 devices c = 0 45 devices c = 0

^{1/} A separate sample for each test shall be pulled.



TEST CIRCUIT

Test conditions and component value					
Type	V _{DD}	V _{GG}	R _L	R _G	I _{D(ON)} (1)
	V dc	V dc	ohms	ohms	μA dc
2N5114, 2N5114UB	-10	20	430	100	-15
2N5115, 2N5115UB	-6.0	12	910	220	-7.0
2N5116, 2N5116UB	-6.0	8.0	2,000	390	-3.0

(1) Nominal value; exact value varies slightly with transistor parameters.

NOTES:

- The input waveform has the following characteristics: $t_p = 100$ ns; $t_r \leq 1$ ns; $t_f \leq 1$ ns; duty cycle ≈ 2 percent. It is supplied by a generator with $Z_{out} = 50$ ohms.
- Resistor tolerance is ± 10 percent.
- Voltage limits for the V_{in} voltage (input switching levels) are as follows:
 2N5114, 2N5114UB $V_{in} = 11$ V dc (from 0 v to -11 V dc signal level).
 2N5115, 2N5115UB $V_{in} = 7$ V dc (from 0 v to -7 V dc signal level).
 2N5116, 2N5116UB $V_{in} = 5$ V dc (from 0 v to -5 V dc signal level).

FIGURE 3. Switching time test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2013-093)

Review activities:

Army - AV, MI
Air Force - 19, 99

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