

The documentation and process conversion measures necessary to comply with this document shall be completed by 26 May 2016.

INCH-POUNDS

MIL-PRF-19500/474J
 26 February 2016
 SUPERSEDING
 MIL-PRF-19500/474H
 8 January 2015

PERFORMANCE SPECIFICATION SHEET

* UNITIZED, MULTIPLE DIODE ARRAYS, SILICON
 TYPES 1N5768, 1N5770, 1N5772, 1N5774, 1N6100, 1N6101, 1N6496,
 1N6506, 1N6507, 1N6508, 1N6509, 1N6510, AND 1N6511

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for silicon, multiple diode array.

* 1.2 Package outlines. The device packages for this specification sheet are in accordance with figures 1 through 8 for all packaged device types.

1.3 Maximum ratings. Unless otherwise specified $T_A = +25^\circ\text{C}$.

Type	$V_{BR(R)}$ 1/ 2/	I_O 1/ 3/ $T_A = +25^\circ\text{C}$	I_{FSM} 1/ $t_p = 1/120$ s	P_T $T_A = +25^\circ\text{C}$	T_J	T_{STG}
	V dc	mA dc	mA dc	mW	$^\circ\text{C}$	$^\circ\text{C}$
1N5768	60	300	500	4/ 500	-65 to +175	-65 to +200
1N5770	60	300	500	4/ 500		
1N5772	60	300	500	4/ 500		
1N5774	60	300	500	4/ 500		
1N6496	60	300	500	4/ 500		
1N6506	60	300	500	5/ 600		
1N6507	60	300	500	5/ 600		
1N6508	60	300	500	5/ 600		
1N6509	60	300	500	5/ 600		
1N6100	75	300	500	4/ 500		
1N6101	75	300	500	5/ 600		
1N6510	75	300	500	4/ 500		
1N6511	75	300	500	5/ 600		

1/ Each diode.

2/ Pulsed: $PW = 100$ ms maximum; duty cycle ≤ 20 percent.

3/ Derate at 2.0 mA/ $^\circ\text{C}$ above $+25^\circ\text{C}$.

4/ Derate at 3.33 mW/ $^\circ\text{C}$ above $+25^\circ\text{C}$.

5/ Derate at 4.0 mW/ $^\circ\text{C}$ above $+25^\circ\text{C}$.

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.4 Primary electrical characteristics, each diode.

Type	V_{F1} (1) $I_F = 100$ mA dc		V_{F2} 1/ $I_F = 500$ mA dc		I_{R1} $V_R = 40$ V dc		C_t		t_{fr} $I_F = 500$ mA dc		t_{rr} $I_F = I_R = 200$ mA dc $R_L = 100 \Omega$ $I_{rr} = 20$ mA dc	
	V dc		V dc		μ A dc		pF		ns		ns	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
1N5768		1.0		1.5		0.1		4		40		20
1N5770		1.0		1.5		0.1		8		40		20
1N5772		1.0		1.5		0.1		8		40		20
1N5774		1.0		1.5		0.1		8		40		20
1N6496		1.0		1.5		0.1		8		40		20
1N6506		1.0		1.5		0.1		4		40		20
1N6507		1.0		1.5		0.1		8		40		20
1N6508		1.0		1.5		0.1		8		40		20
1N6509		1.0		1.5		0.1		8		40		20
1N6100		1.0				(2) 25		4		(3) 15		(4) 10
1N6101		1.0				(2) 25		4		(3) 15		(4) 10
1N6510		1.0				(2) 25		4		(3) 15		(4) 10
1N6511		1.0				(2) 25		4		(3) 15		(4) 10

(1) Pulsed: $PW = 300 \mu s \pm 50 \mu s$, duty cycle ≤ 2 percent, $90 \mu s$ after leading edge of pulse.

(2) For these types, I_{R2} at $V_R = 20$ Vdc.

(3) For these types, t_{fr} at $I_F = 100$ mA dc.

(4) For these types, $I_F = I_R = 10$ mA dc, $I_{rr} = 1$ mA dc.

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500 and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN brand and quality level. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: JAN, JANTX, JANTXV, and JANS.

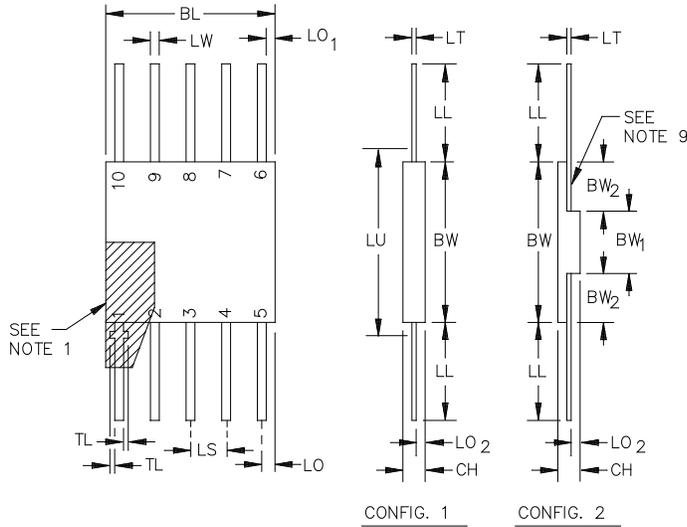
* 1.5.2 Device type. The designation system for the device types of multiple diode arrays covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The multiple diode arrays of this specification sheet are identified by the first number and letter symbols "1N".

* 1.5.2.2 Second number symbols. The second number symbols for the multiple diode arrays covered by this specification sheet are as follows: "5768", "5770", "5772", "5774", "6100", "6101", "6496", "6506", "6507", "6508", "6509", "6510", and "6511".

* 1.5.2.3 Suffix letters. Suffix letters are not applicable for this specification sheet.

* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

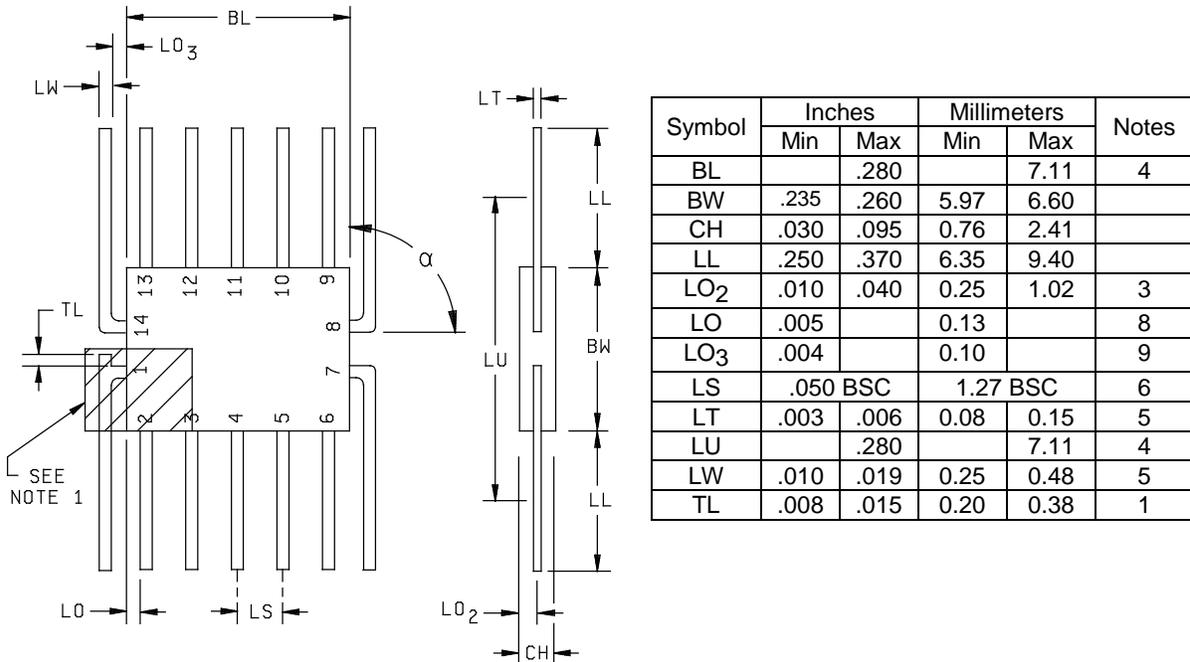


Symbol	Inches		Millimeters		Notes	Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max			Min	Max	Min	Max	
BL		.290		7.37	3	LO ₁	.005		0.13		7, 8
BW	.235	.260	5.97	6.60		LO ₂	.005	.050	0.13	1.27	2
BW ₁	.125		3.18			LS	.050 BSC		1.27 BSC		4, 6
BW ₂	.030		0.76			LT	.003	.006	0.08	0.15	5
CH	.030	.095	0.76	2.41		LU		.280		7.11	3
LL	.240	.370	6.10	9.40		LW	.010	.019	0.25	0.48	5
LO		.045		1.14	7	TL	.008	.015	0.20	0.38	1

NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark. Alternatively, a tab (dimension TL) may be used to identify pin 1. This tab may be located on either side as shown. If a pin 1 identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
2. Dimension LO₂ shall be measured at the point of exit of the lead from the body. Dimension LO₂ shall be .0085 inch (0.216 mm) minimum when lead finish A is solder.
3. These dimensions allow for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 10.
5. All leads: Dimensions are pre-solder dip.
6. Eight spaces.
7. Applies to all four corners (lead numbers 1, 5, 6, and 10).
8. Dimension LO may be .000 inch (0.00 mm) if lead numbers 1, 5, 6, and 10 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body. For all bottom-brazed or side-brazed configurations, dimension LO shall be measured from the edge of the furthest extension of the metal pad or lead.
9. Optional configuration. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Dimensions are in inches. Millimeters are given for general information only.

FIGURE 1. Physical dimensions for types 1N5768, 1N5770, and 1N5772.

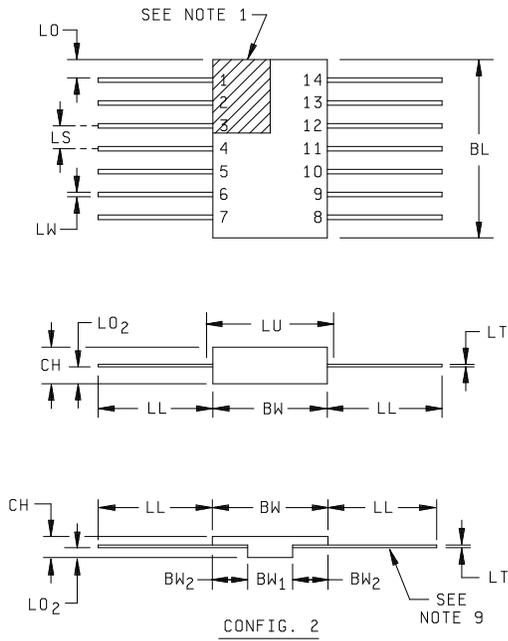


NOTES:

This package is inactive and shall be replaced with the package on [figure 3](#).

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark. Alternatively, a tab (dimensions TL) may be used to identify pin 1. This tab may be located on either side as shown. If a pin 1 identification mark is used in addition to this tab, the minimum limit of dimension TL does not apply.
2. Dimension LO₂ shall be measured at the point of exit of the lead from the body. Dimension LO₂ shall be .0085 inch (0.216 mm) minimum when lead finish A is applied.
3. These dimensions allow for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ± 0.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
5. All leads: Increase maximum limit by .003 inch (0.08 mm) measured at the center of the flat, when lead finish A is applied. Dimensions given are pre-solder dip.
6. Twelve places.
7. Applies to all four corners (lead numbers 2, 6, 9, and 13).
8. Dimensions LO may be .000 inch (0.00 mm) if lead numbers 2, 6, 9, and 13 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body.
9. Applies to lead numbers 1, 7, 8, and 14.
10. Lead configuration is optional within dimension BW except dimensions LT and LW apply.
11. Dimensions are in inches. Millimeters are given for general information only.

FIGURE 2. Physical dimensions for types 1N5774 and 1N6100.

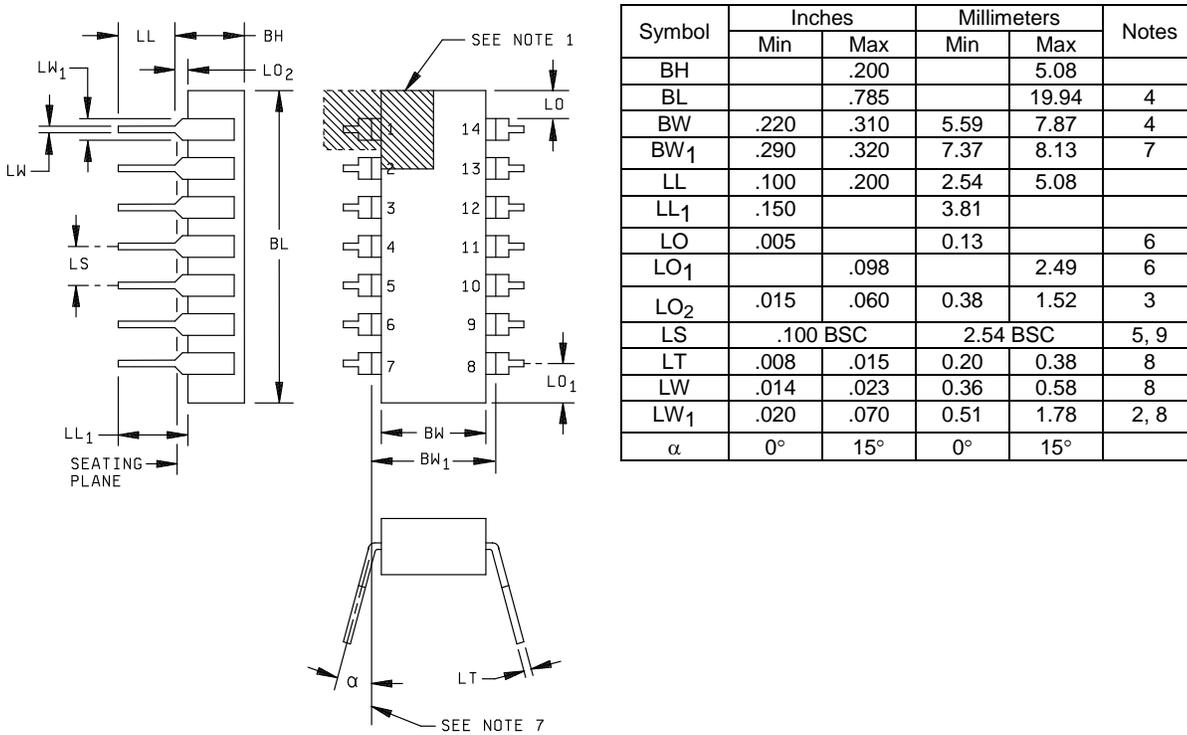


Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL		.390		9.91	3
BW	.235	.280	5.97	6.60	
BW ₁	.125		3.18		
BW ₂	.030		0.76		
CH	.045	.095	1.14	2.41	
LL	.250	.370	6.35	9.40	
LO	.005		0.13		7, 8
LO ₂	.010	.045	0.66	1.14	2
LS	.050 BSC		1.27 BSC		4, 6
LT	.003	.006	0.08	0.15	5
LU		.280		7.11	3
LW	.010	.019	0.25	0.48	5

NOTES

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. Dimension LO₂ shall be measured at the point of exit of the lead from the body. Dimension LO₂ minimum shall be reduced by .0015 inch (0.038 mm) maximum when lead finish is solder.
3. These dimensions allow for off-center lid, meniscus, and glass overrun.
4. The basic pin spacing is .050 inch (1.27 mm) between centerlines. Each pin centerline shall be located within ±.005 inch (0.13 mm) of its exact longitudinal position relative to pins 1 and 14.
5. All leads: Dimensions are pre-solder dip.
6. Twelve spaces.
7. Applies to all four corners.
8. Dimensions LO may be .000 inch (0.00 mm) if lead numbers 1, 7, 8, and 14 bend toward the cavity of the package within one lead width from the point of entry of the lead into the body.
9. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Lead configuration is optional within dimension BW except dimensions LW and LT apply.
11. Dimensions are in inches. Millimeters are given for general information only.

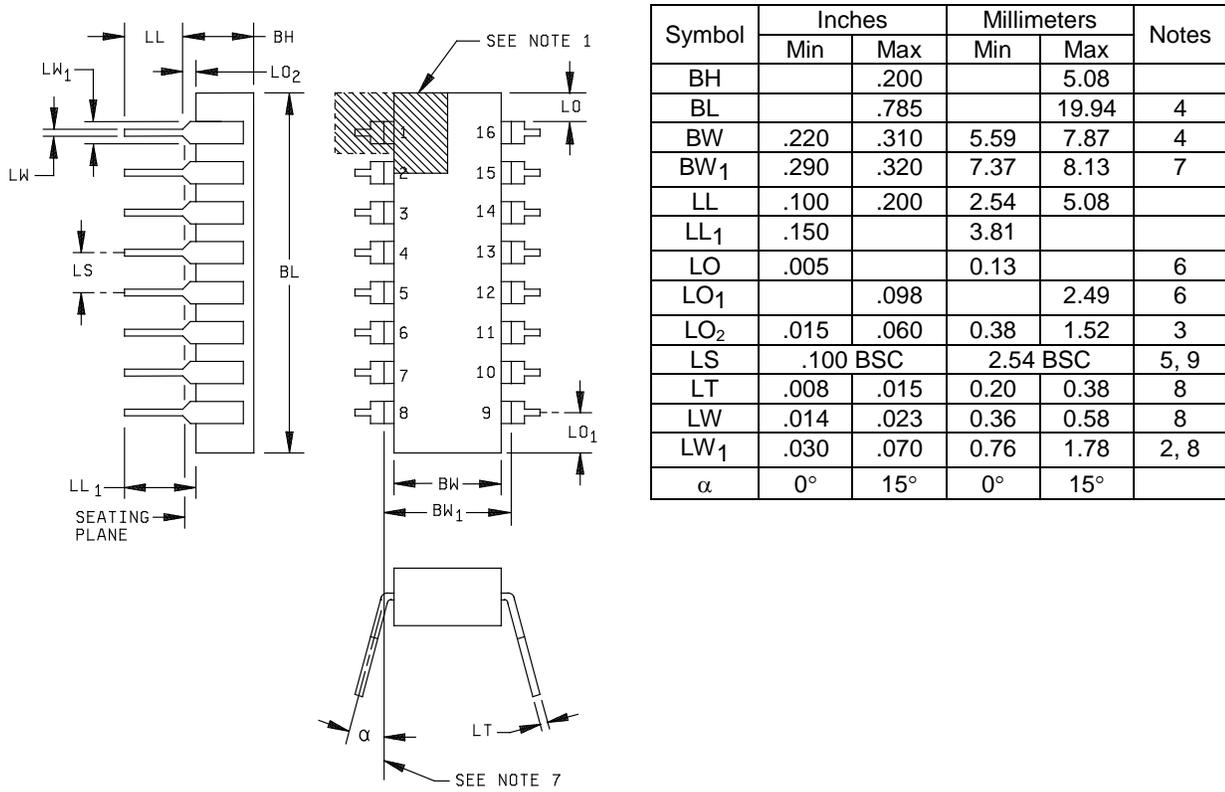
FIGURE 3. Alternate physical dimensions for types 1N5774 and 1N6100.



NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. The minimum limit for dimension LW₁ may be .023 inch (0.58 mm) for lead numbers 1, 7, 8, and 14 only.
3. Dimension LO₂ shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (0.25 mm) of its exact longitudinal position relative to pins 1 and 14.
6. Applies to all four corners (lead numbers 1, 7, 8, and 14).
7. Lead center when α is 0 degrees. BW₁ shall be measured at the centerline of the leads.
8. All leads: Dimensions are pre-solder dip. Pointed or round lead ends are allowed.
9. Twelve spaces.
10. Dimensions are in inches. Millimeters are given for general information only.

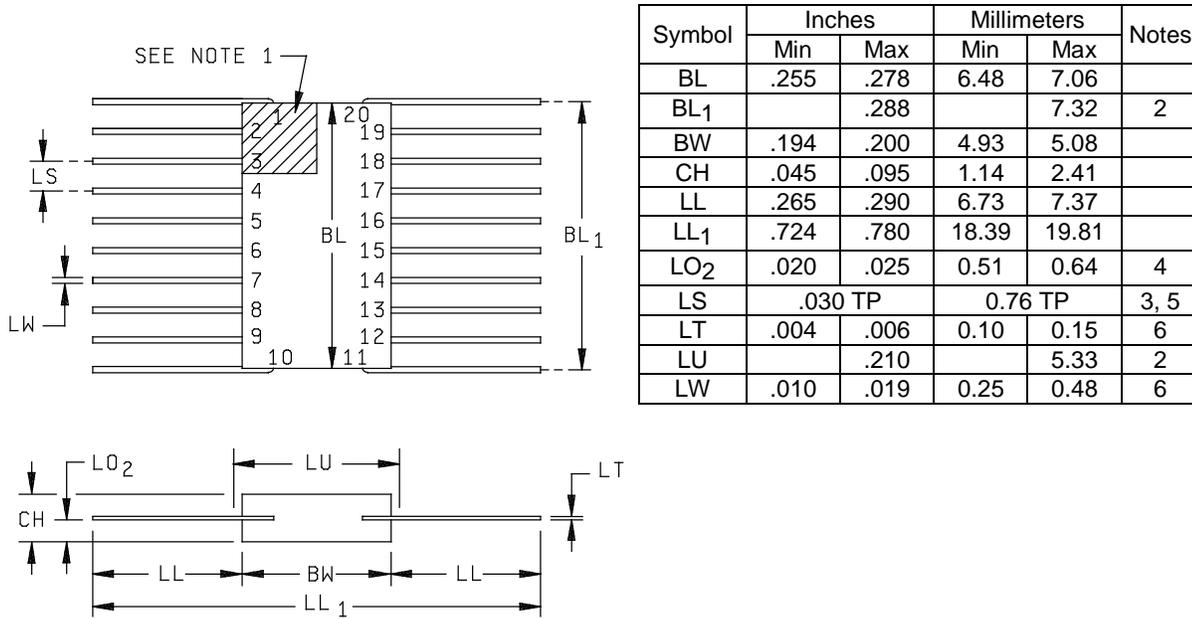
FIGURE 4. Physical dimensions for types 1N6506, 1N6507, 1N6508, 1N6509, and 1N6511.



NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. The minimum limit for dimension LW₁ may be .020 inch (0.51 mm) for lead numbers 1, 8, 9, and 16 only.
3. Dimension LO₂ shall be measured from the seating plane to the base plane.
4. This dimension allows for off-center lid, meniscus, and glass overrun.
5. The basic pin spacing is .100 inch (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 inch (0.25 mm) of its exact longitudinal position relative to pins 1 and 16.
6. Applies to all four corners (lead numbers 1, 8, 9, and 16).
7. Lead center when α is 0 degrees. BW₁ shall be measured at the centerline of the leads.
8. All leads: Dimensions are pre-solder dip. Pointed or round lead ends are allowed.
9. Fourteen spaces.
10. Dimensions are in inches. Millimeters are given for general information only.

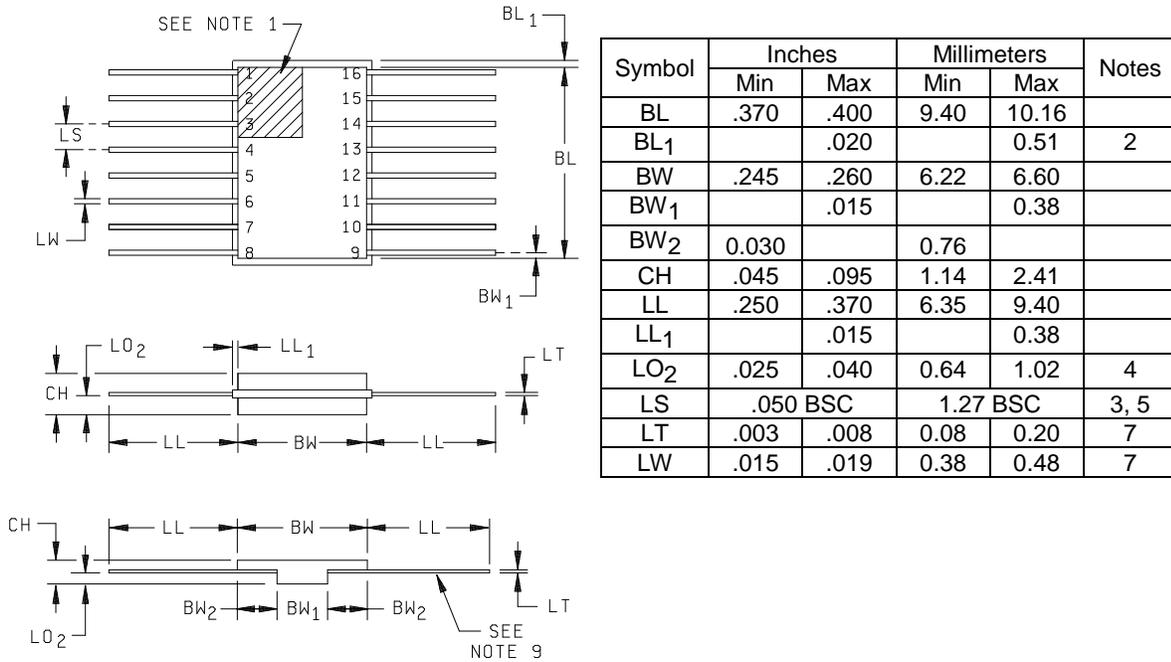
FIGURE 5. Physical dimensions for type 1N6101.



NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area limited by pin 3 and package centerline. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The true position pin spacing is located within ± 0.005 inch (0.13 mm) of its true longitudinal position relative to pins 1 and 20.
4. Dimension LO₂ shall be measured at the point of exit of the lead from the body.
5. Eighteen spaces.
6. All leads: Dimensions are pre-solder dip.
7. Dimensions are in inches. Millimeters are given for general information only.

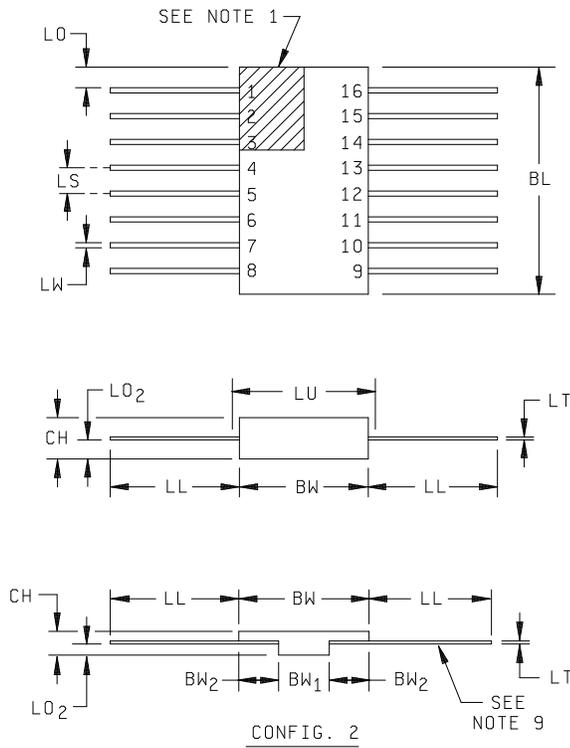
FIGURE 6. Physical dimensions for type 1N6496.



NOTES:

1. This package is inactive and shall be replaced with the package on [figure 8](#).
2. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area limited by pin 3 and package centerline. The manufacturer's identification shall not be used as a pin 1 identification mark.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. The true position pin spacing is located within ± 0.005 inch (0.13 mm) of its true longitudinal position relative to pins 1 and 16.
5. Dimension LO₂ shall be measured at the point of exit of the lead from the body.
6. Fourteen spaces.
7. All leads: Dimensions are pre-solder dip.
8. Dimensions are in inches. Millimeters are given for general information only.
9. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.

FIGURE 7. Physical dimensions for type 1N6510.



Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
BL	.370	.445	9.40	10.16	
BW	.235	.275	5.97	6.60	10
BW ₁	.125		3.18		
BW ₂	.030		0.76		
CH	.045	.095	1.52	2.41	
LL	.250	.370	6.35	9.40	
LO	.005		0.13		11
LO ₂	.005	.050	0.13	1.27	2
LS	.050 BSC		1.27 BSC		3, 5
LT	.003	.006	0.08	0.15	6
LW	.015	.022	0.38	0.48	6

NOTES:

1. Index area: A notch or a pin 1 identification mark shall be located adjacent to pin 1 and shall be within the shaded area limited by pin 3 and package centerline. The manufacturer's identification shall not be used as a pin 1 identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The true position pin spacing is located within ± 0.005 inch (0.13 mm) of its true longitudinal position relative to pins 1 and 14.
4. Dimension LO₂ shall be measured at the point of exit of the lead from the body.
5. Twelve places.
6. All leads: Dimensions are pre-solder dip.
7. Dimensions are in inches.
8. Millimeters are given for general information only.
9. If this configuration is used, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
10. Lead configuration is optional within dimension BW except dimensions LW and LT apply.
11. Applies to all four corners.

FIGURE 8. Physical dimensions for type 1N6510.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 – Test Methods for Semiconductor Devices.
MIL-STD-883 - Microcircuits

(Copies of these documents are available online at <http://quicksearch.dla.mil>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as specified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows.

- I_{Ri} - Isolation current between any two interconnect pins of adjacent parallel sets of diodes with all other pins open circuited.
- I_{RX} - Reverse current for each diode of test section.
- V_{fr} - Forward recovery voltage. Specified maximum forward voltage used to determine forward recovery time.
- V_{FX} - Forward voltage for each diode of test section.

3.4 Interface requirements and physical dimension. The interface requirements and physical dimension shall be as specified in MIL-PRF-19500 and herein. The device package style is as specified in either figures 1, 2, 3, 4, 5, 6, 7, or 8. Schematic diagrams are specified in figure 9. No organic or polymeric materials shall be used.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead material of finish is desired, it shall be specified in the acquisition document (see 6.2).

3.4.2 Pin-out. The pin-out of the device shall be as shown on figure 1, figure 2, figure 3, figure 4, figure 5, figure 6, figure 7 and figure 8.

3.5 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

* 3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#) and [table I](#).

3.7 Workmanship. Multiple diode arrays shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [table I](#) and [table II](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not require the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (JANS, JANTXV, and JANTX levels). Screening shall be in accordance with table E-IV of [MIL-PRF-19500](#) and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurements	
	JANS level	JANTX and JANTXV levels
1	Method 2010 of MIL-STD-883 , condition B	Method 2010 of MIL-STD-883 , condition B (JANTXV only)
7	Optional	Optional
9	Not applicable	Not applicable
11	I_{R1} and V_{F1}	I_{R1} and V_{F1}
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; ΔI_{R1} = 100 percent of initial reading or 10 nA dc, whichever is greater; ΔV_{F1} = ± 25 mV dc of initial reading.	Subgroup 2 of table I herein; ΔI_{R1} = 100 percent of initial reading or ± 25 nA dc, whichever is greater; ΔV_{F1} = ± 30 mV dc of initial reading.
14	Required	Required

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows (see [4.5.7](#)): T_A = +150°C. Time = 72 hours minimum. V_R = 50 V dc for 1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, and 1N6509. V_R = 60 V dc for 1N6100, 1N6101, 1N6510, and 1N6511.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance [MIL-PRF-19500](#) and [table I](#) herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIa (JANS) and table E-VIb (JAN, JANTX, JANTXV) of [MIL-PRF-19500](#) herein.

* 4.4.2.1 Group B inspection, table E-VIa (JANS) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B4	1027	$T_A = +150^\circ\text{C}$ each diode DC blocking, $V_R = 50\text{ V dc}$.

4.4.2.2 Group B inspection, table E-VIb (JANTX and JANTXV) of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1027	DC blocking; $T_A = +150^\circ\text{C}$; $V_R = 50\text{ V dc}$.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#) and herein.

* 4.4.3.1 Group C inspection, table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	1056	Test condition A.
* C2	2036	TA condition E; 3 oz. weight, three bends of 45 for flat packs, three bends of 15 for dips; omit end leads of configuration 2.
C6	1026	$T_A = +150^\circ\text{C}$; $V_R = 50\text{ V dc}$.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#), and [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Measurement of reverse current for 1N5772, 1N5774, 1N6496 1N6508, and 1N6509. For 1N5772, 1N5774, 1N6496, 1N6508, and 1N6509, the reverse current shall be measured using a circuit which bypasses the shunt resistance through the other diodes not under test, around the current meter. Care should be taken to assure that the voltage drop across the current meter is less than 10 millivolts.

4.5.2 Forward voltage. This parameter shall be measured 90 microseconds after the leading edge of the pulse.

4.5.3 Peak forward voltage. During this test, the maximum shunt capacitance across the diode shall be 19 pF and the equipment bandwidth shall be 80 MHz minimum.

4.5.4 Pin-to-pin capacitance. This parameter is the total pin-to-pin capacitance across each individual diode and may not necessarily represent actual diode capacitance since they are all connected together at either the anode or cathode and these connections represent additional capacitance.

4.5.5 Reverse current (I_{RX}) and forward voltage (V_{FX}). Each common anode section and each common cathode section shall be tested separately. Each diode in the test section shall be measured individually after the array has reached thermal equilibrium.

4.5.6 Isolation current (I_R); bridging current (I_{Rbr}). These devices shall be subjected to the isolation current/bridging current tests as specified:

- a. For types 1N5772, 1N5774, 1N6496, 1N6508, and 1N6509, the bridging current shall be measured by supplying the forcing function to every other interconnect pin and measuring the remaining interconnect pins (excluding common anode and common cathode pins), I_{Rbr} . Repeat the test, reversing the polarity of the forcing function.
- b. For types 1N6100, 1N6101, 1N6511, and 1N6510, the bridging current shall be measured by applying the forcing function to every other diode (anode and cathode simultaneously) and measuring the remaining diodes (anode and cathode simultaneously), I_{Rbr} . Repeat the test, reversing the polarity of the forcing function.
- c. For types 1N5774, 1N6496, and 1N6509, the isolation current shall be measured between the individual circuits by applying the forcing function to the anode and cathode of one circuit and measuring to the anode and cathode of other circuit, I_{Ri} . Repeat the test, reversing the polarity of the forcing function.
- d. For types 1N5768 and 1N6506, the forcing function shall be applied to every other anode and measured on the remaining anodes, I_{Rbr} . Repeat the test, reversing the polarity of the forcing function.
- e. For types 1N5770 and 1N6507, the forcing function shall be applied to every other cathode and measured on the remaining cathodes, I_{Rbr} . Repeat the test, reversing the polarity of the forcing function.

4.5.7 Free air power burn-in and life tests. The use of a current limiting or ballast resistor is permitted provided that each device under test still sees the full P_t (minimum) and that the minimum applied voltage, where applicable, is maintained throughout the burn-in period.

* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical Inspection	2071					
<u>Subgroup 2</u>						
Breakdown voltage	4021		V(BR)			
1N5768, 1N5770, 1N5772 1N5774, 1N6496, 1N6506 1N6507, 1N6508, 1N6509		I _R = 10 μ A dc; PW = 100 ms maximum duty cycle \leq 20 percent		60		V dc
1N6100, 1N6101, 1N6510 1N6511		I _R = 5 μ A dc; PW = 100 ms maximum; duty cycle \leq 20 percent		75		V dc
Reverse current	4016	DC method (see 4.5.1)				
All types		V _R = 40 V dc	I _{R1}		.1	μ A dc
1N6100, 1N6101, 1N6510 1N6511		V _R = 20 V dc	I _{R2}		25	nA dc
Forward voltage	4011	Condition B, PW = 300 μ s \pm 50 μ s; duty cycle \leq 2 percent (see 4.5.2)				
All types		I _F = 100 mA dc	V _{F1}		1.0	V dc
1N5768, 1N5770, 1N5772 1N5774, 1N6496, 1N6506 1N6507, 1N6508, 1N6509		I _F = 500 mA dc	V _{F2}		1.5	V dc
<u>Subgroup 3</u>						
High temperature operation:		T _A = +150°C				
Reverse current	4016	DC method; V _R = 40 V dc				
Low temperature operation:		T _A = -55°C	I _{R3}		50	μ A dc
Forward voltage	4011	Condition B, I _F = 10 mA dc	V _{F3}		1	V dc

See footnote at end of table.

* TABLE I. Group A inspection - Continued.

Inspection 1/ <u>Subgroup 4</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
Forward recovery voltage (peak)	4026	PW \geq 150 ns; $R_S = 50\Omega$; $t_r = 10$ ns; duty cycle \leq 2 percent (see 4.5.3)	V_{F4}			
1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, 1N6509		$I_F = 500$ mA			5	V (pk)
1N6100, 1N6101, 1N6510, 1N6511		$I_F = 100$ mA			5	V (pk)
Capacitance (pin-to-pin)	4001	$V_R = 0$ V dc; $f = 1$ MHz (see 4.5.4)	C_t			
1N5770, 1N5772, 1N5774, 1N6496, 1N6507, 1N6508, 1N6509					8	pF
1N5768, 1N6100, 1N6101, 1N6506, 1N6510, 1N6511					4	pF
Forward recovery time	4026	PW \geq 150 ns; $R_S = 50\Omega$; duty cycle \leq 2 percent, $t_r = 10$ ns; $V_{fr} = 1.1$ V dc	t_{fr}			
1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, 1N6509		$I_F = 500$ mA dc			40	ns
1N6100, 1N6101, 1N6510, 1N6511		$I_F = 100$ mA dc			15	ns
Reverse recovery time	4031	Condition B; $I_F = I_R = 200$ mA; $R_L = 100\Omega$; $I_{rr} = 20$ mA	t_{rr}			
1N5768, 1N5770, 1N5772, 1N5774, 1N6496, 1N6506, 1N6507, 1N6508, 1N6509					20	ns
1N6100, 1N6101, 1N6510, 1N6511		Condition B; $I_F = I_R = 10$ mA; $R_L = 100\Omega$; $I_{rr} = 1$ mA			10	ns
Forward voltage (match)	4011	Condition B, $I_F = 10$ mA	V_{F5}			
1N6100, 1N6101, 1N6510, 1N6511					5	mV

See footnote at end of table.

* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> Not applicable						
<u>Subgroup 6</u> Surge current	4066	Condition A, $I_{FSM} = 500$ mA(pk); 10 surges at one per minute; $t_p = 1/120$ s; choose four diodes from each array in cycles.				
Electrical measurements		See table. I, subgroup 2				
<u>Subgroup 7</u> Reverse current (except omit for the following devices.) 1N6100, 1N6101, 1N6510, 1N6511	4016	DC method; $V_R = 40$ V dc; $I_F = 25$ mA dc for each of the other diodes in the test section (see 4.5.5).	I_{RX}		10	μ A dc
Forward voltage (except omit for the following devices.) 1N6100, 1N6101, 1N6510 1N6511	4011	Condition B, $I_F = 25$ mA dc for each of the other diodes in the test section (see 4.5.5)	V_{FX}		1.0	V dc
Bridging current (all devices)	4016	DC method; $V_R = +40$ V dc and -40 V dc (see 4.5.6.a through 4.5.6.d)	I_{Rbr}		0.8	μ A dc
Isolation current 1N5774 1N6496 1N6509	4016	DC method; $V_R = +40$ V dc and -40 V dc (see 4.5.6.c)	I_{Ri}		0.8	μ A dc

1/ For sampling plan, see MIL-PRF-19500.

* TABLE II. Group E inspection (all quality levels) for qualification and requalification only.

Inspection	MIL-STD-750		Qualification inspection
	Method	Conditions	
<u>Subgroup 1</u>			n = 45, c = 0
Temperature cycling	1051	500 cycles, -65°C to +175°C	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurement		See table I , subgroup 2.	
<u>Subgroup 2</u>			n = 45, c = 0
Intermittent operating life	1037	10,000 cycles.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroups 3, 4, 5, 7, 8 and 9</u>			
Not applicable			

*

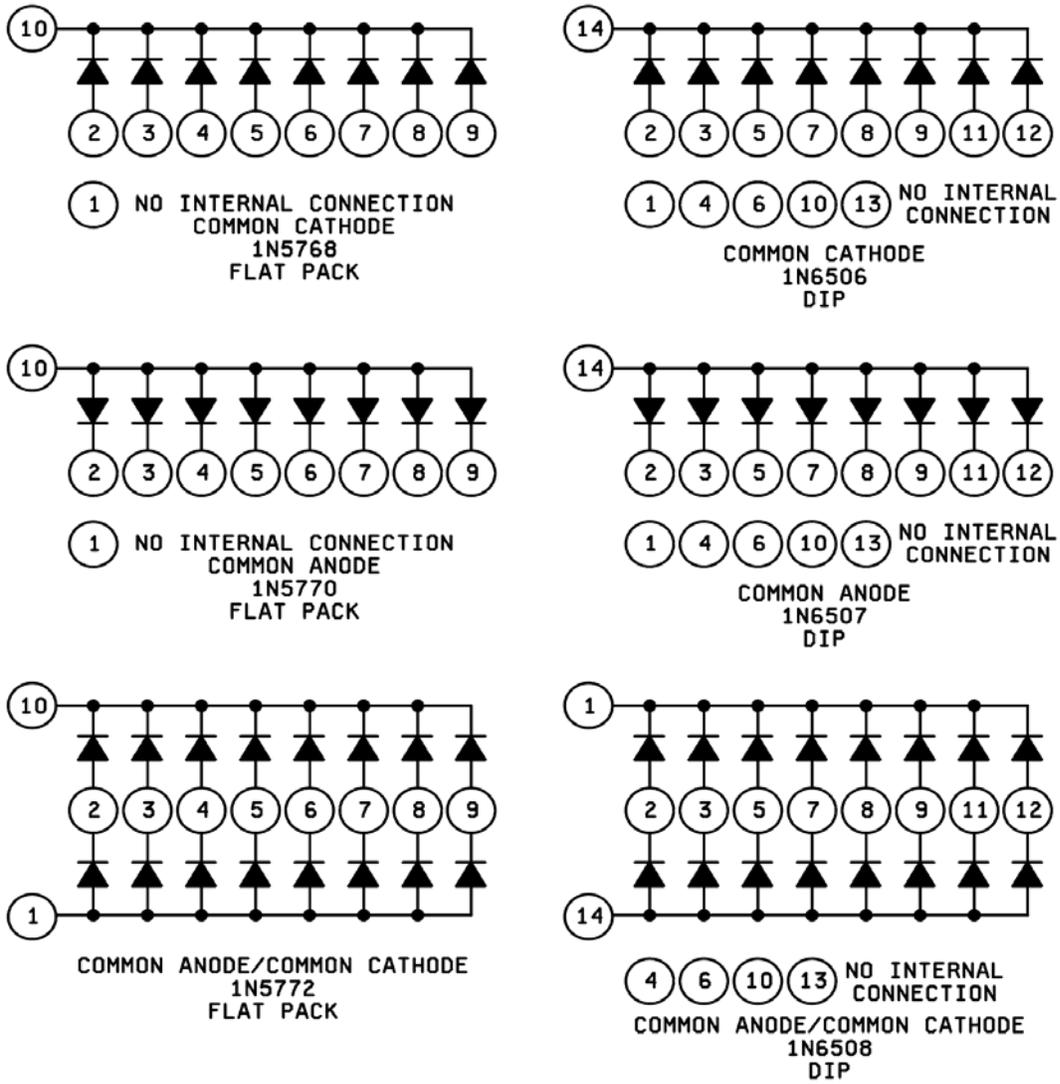


FIGURE 9. Schematics.

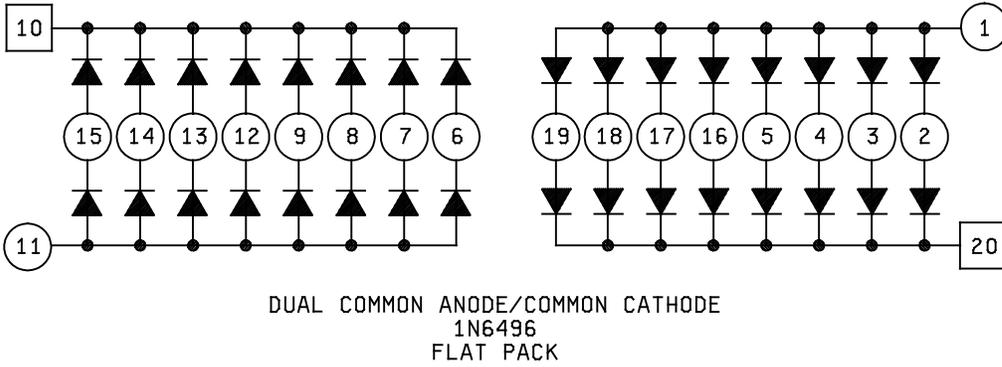
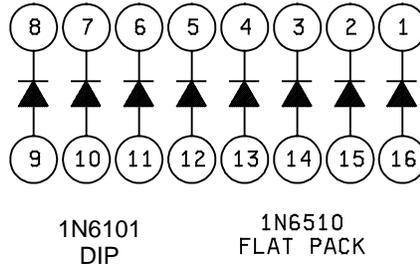
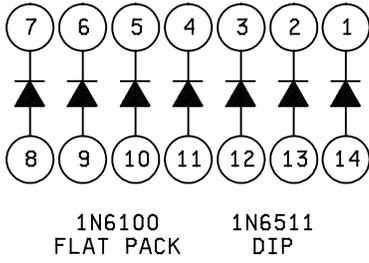
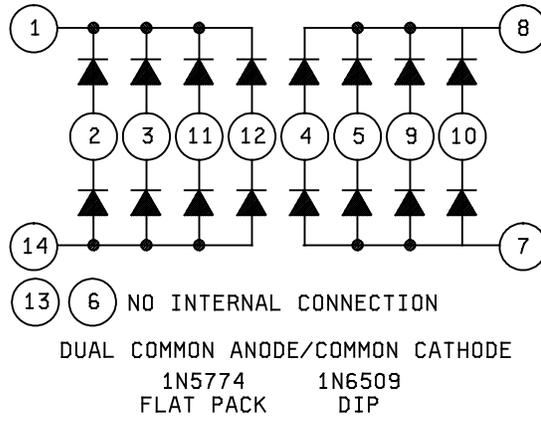


FIGURE 9. Schematics - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

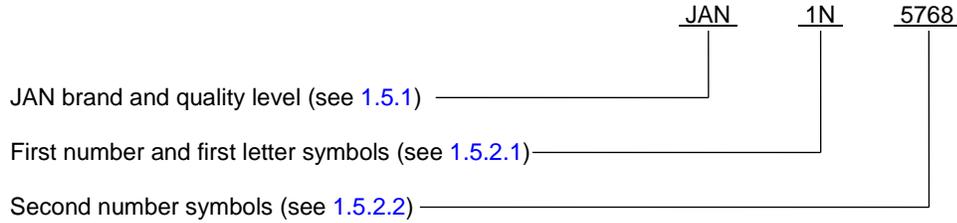
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete Part or Identifying Number (PIN), see 1.5 and 6.4.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil.

* 6.4 PIN construction example. The PINs for encapsulated devices are constructed using the following form.



6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN1N5768	JANTX1N5768	JANTXV1N5768	JANS1N5768
JAN1N5770	JANTX1N5770	JANTXV1N5770	JANS1N5770
JAN1N5772	JANTX1N5772	JANTXV1N5772	JANS1N5772
JAN1N5774	JANTX1N5774	JANTXV1N5774	JANS1N5774
JAN1N6100	JANTX1N6100	JANTXV1N6100	JANS1N6100
JAN1N6101	JANTX1N6101	JANTXV1N6101	JANS1N6101
JAN1N6496	JANTX1N6496	JANTXV1N6496	JANS1N6496
JAN1N6506	JANTX1N6506	JANTXV1N6506	JANS1N6506
JAN1N6507	JANTX1N6507	JANTXV1N6507	JANS1N6507
JAN1N6508	JANTX1N6508	JANTXV1N6508	JANS1N6508
JAN1N6509	JANTX1N6509	JANTXV1N6509	JANS1N6509
JAN1N6510	JANTX1N6510	JANTXV1N6510	JANS1N6510
JAN1N6511	JANTX1N6511	JANTXV1N6511	JANS1N6511

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2016-003)

Review activities:
 Army - AR, AV, MI, SM
 Navy - AS, MC
 Air Force - 99

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