The documentation and process conversion measures necessary to comply with this revision shall be completed by 18 March 2016.

INCH-POUND

MIL-PRF-19500/433J
18 December 2015
SUPERSEDING
MIL-PRF-19500/433H
14 August 2006

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, PNP, SILICON, HIGH-POWER, THROUGH-HOLE PACKAGE,
TYPES 2N4399 AND 2N5745, JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

* 1.1 Scope. This specification covers the performance requirements for PNP silicon, high-power transistors. Four levels of product assurance (JAN, JANTX, JANTXV, and JANS) are provided for each encapsulated device.

1.2 Physical dimensions. See figure 1, (TO-3).

1.3 Maximum ratings. T_A = +25°C, unless otherwise specified.

Type	P_T (1)	P_T (2) T_C = +100°C	$R_{\theta JC}$	$R_{\theta JA}$	V_{CBO}	V_{CEO}	V_{EBO}	I_B	I_C	T_J and T_{STG}
	W	W	°C/W	°C/W	V dc	V dc	V dc	A dc	A dc	°C
2N4399	5	115	0.875	35	-60	-60	-5	-7.5	-30	-55 to +200
2N5745	5	115	0.875	35	-80	-80	-5	-7.5	-20	-55 to +200

(1) Derate linearly 28.57 mW/°C above T_A = +25°C.
(2) Derate linearly 1.15 W/°C above T_C = +100°C.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at https://assist.dla.mil.

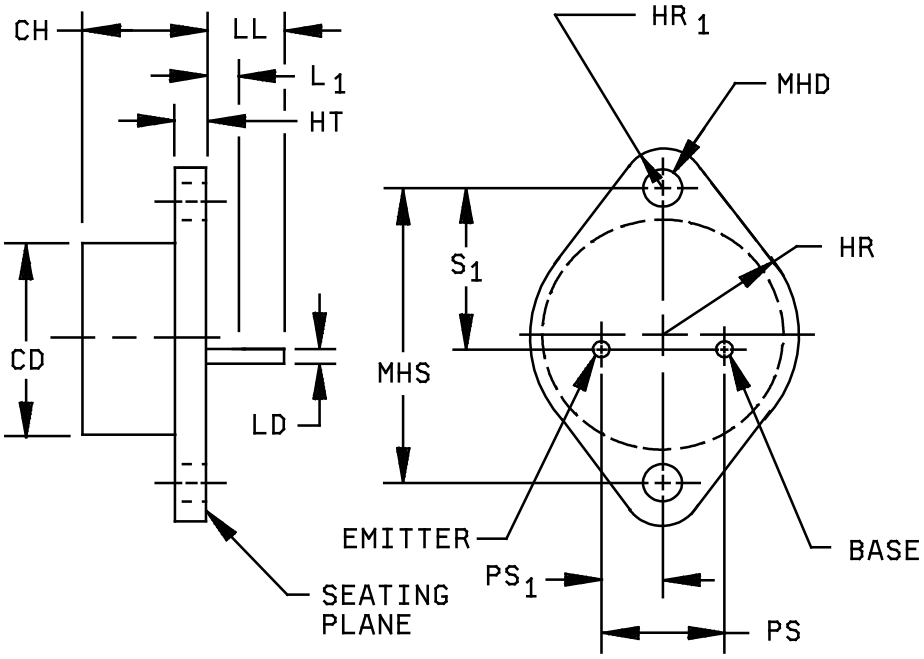


FIGURE 1. Physical dimensions (TO-3).

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.23	
CH	.270	.380	6.86	9.65	
HT	.060	.135	1.52	3.43	
HR	.495	.525	12.57	13.34	
HR_1	.131	.188	3.33	4.78	
LD	.038	.043	0.97	1.09	5
LL	.312	.500	7.92	12.70	5
L_1		.050		1.27	5
MHD	.151	.161	3.84	4.09	
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	2, 3
PS_1	.205	.225	5.21	5.72	2, 3
S_1	.655	.675	16.64	17.15	2

NOTES:
1. Dimensions are in inches. Millimeters are given for general information only.
2. These dimensions should be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.
3. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
4. Collector shall be electrically connected to the case.
5. LD applies between L1 and LL. Lead diameter shall not exceed twice LD within L_1
6. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions (TO-3) - Continued.

1.4 Primary electrical characteristics at T_C = +25°C.

Limit	h_{FE2} (1)		$\|h_{FE}\|$	$V_{CE(sat)1}$ (1)		$V_{BE(sat)1}$ (1)		C_{obo}	Switching	
	V_{CE} = -2 V dc I_C = -15 A dc	V_{CE} = -2 V dc I_C = -10 A dc	V_{CE} = -10 V dc I_C = -1 A dc f = 1 MHz	I_C = -10 A dc I_B = -1.0 A dc		I_C = -15 A dc I_B = -1.5 A dc		V_{CB} = -10 V dc I_E = 0 100 kHz ≤ f ≤ 1 MHz	t_{on}	t_{off}
	2N4399	2N5745	V dc	2N4399 V dc	2N5745 V dc	2N4399 V dc	2N5745 V dc	pF	µs	µs
Min	15	15	4							
Max	60	60	40	-0.75	-1.0	-1.8	-2.0	1,000	1.2	2.5

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: “JAN”, “JANTX”, “JANTXV” and "JANS".

* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "4399" and "5745".

* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDSIS-19500.

2. APPLICABLE DOCUMENTS

* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at http://quicksearch.dla.mil/).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figure 1.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500, and herein (see 6.2).

3.5 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.6 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table I.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of and inspection. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Screening (see 4.3).

c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.2)	Thermal impedance (see 4.3.2)
9	I_{CEX1} and h_{FE2}	I_{CEX1}
11	I_{CEX1} and h_{FE2} $\Delta I_{CEX1} \leq$ 100 percent of initial value or -5 nA dc, whichever is greater. $\Delta h_{FE2} \leq \pm$ 15 percent of initial value	I_{CEX1} and h_{FE2}; $\Delta I_{CEX1} \leq$ 100 percent of initial value or -100 nA dc, whichever is greater.
12	See 4.3.1	See 4.3.1
13	Subgroup 2 of table I herein; $\Delta I_{CEX1} \leq$ 100 percent of initial value or -50 nA dc, whichever is greater; $\Delta h_{FE2} \leq \pm$ 15 percent of initial value	Subgroup 2 of table I herein; $\Delta I_{CEX1} \leq$ 100 percent of initial value or -100 nA dc, whichever is greater; $\Delta h_{FE2} \leq \pm$ 15 percent of initial value;

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: T_J = +187.5 ± 12.5°C; V_{CE} = -30 V dc, ±10 V dc; T_A = room ambient as defined in the general requirements of MIL-STD-750.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M, I_H, t_H, t_{SW}, (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of table I, subgroup 1 and 2 inspection only (table E-VIB, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500, and as follows.

* 4.4.2.1 Quality level JANS, table E-VIA of MIL-PRF-19500.

	Subgroup	Method	Conditions
*	B4	1037	V_{CB} = -20 V dc; P_T = 5 W at T_A = room ambient as defined in the general requirements of 4.5 of MIL-STD-750; $t_{on} = t_{off}$ = 3 minutes minimum . No heat sink or forced-air cooling on devices shall be permitted.
	B5	1027	V_{CB} = -20 V dc; T_A = +125°C ± 25°C for 96 hours; P_T = 5 W at T_A = +125°C or adjusted as required by the chosen T_A to give an average lot T_J = +275°C.

* 4.4.2.2 Quality levels JAN, JANTX and JANTXV, table E-VIB of MIL-PRF-19500.

	Subgroup	Method	Conditions
*	B3	1037	V_{CB} = -20 V dc; adjust device current or power between cycles to achieve a minimum ΔT_J of +100°C; $t_{on} = t_{off}$ = 3 minutes minimum-. No heat sink or forced-air cooling on the devices shall be permitted.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows.

	Subgroup	Method	Conditions
	C2	2036	Test condition A, weight = 10 lbs, t = 15 seconds.
*	C5	3131	See 1.3, $R_{\theta JC}$ = 0.875.
	C6	1037	V_{CB} = -20 V dc; Adjust device current or power between cycles to achieve a minimum ΔT_J of +100°C; $t_{on} = t_{off}$ = 3 minutes minimum. No heat sink or forced-air cooling on device shall be permitted.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

* TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits 2/		Unit
	Method	Conditions		Min	Max	
Subgroup 1						
Visual and mechanical inspection	2071					
Subgroup 2						
Thermal impedance	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Collector to base breakdown voltage	3011	Bias condition D; I_C = -200 mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$			
2N4399				-60		V dc
2N5745				-80		V dc
Collector to emitter cutoff current	3041	Bias condition D	I_{CEO}			
2N4399		V_{CE} = -60 V dc			-100	µA dc
2N5745		V_{CE} = -80 V dc			-100	µA dc
Emitter-base cutoff current	3061	Bias condition D; V_{EB} = -5 V dc	I_{EBO}		-5.0	µA dc
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = +1.5 V dc	I_{CEX1}			
2N4399		V_{CE} = -60 V dc			-5.0	µA dc
2N5745		V_{CE} = -80 V dc			-5.0	µA dc
Base emitter saturated voltage	3066	Test condition A; I_C = -15 A dc; I_B = -1.5 A dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$			
2N4399					-1.8	V dc
2N5745					-2.0	V dc
Base emitter saturated voltage	3066	Test condition A; I_C = -10 A dc; I_B = -1.0 A dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-1.7	V dc
Collector to emitter saturated voltage	3071	Pulsed (see 4.5.1); I_C = -10 A dc; I_B = -1 A dc	$V_{CE(sat)1}$			
2N4399					-0.75	V dc
2N5745					-1.0	V dc
Collector to emitter saturated voltage	3071	I_C = -5.0 dc; I_B = -0.5 A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		-0.55	V dc
Forward-current transfer ratio	3076	V_{CE} = -2 V dc; I_C = -1.0 A dc; pulsed (see 4.5.1)	h_{FE1}	40	425	

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 2 - Continued						
Forward-current transfer ratio	3076	V_{CE} = -2 V dc; pulsed (see 4.5.1)	h_{FE2}			
2N4399		I_C = -15 A dc		15	60	
2N5745		I_C = -10 A dc		15	60	
Forward-current transfer ratio	3076	V_{CE} = -5 V dc; pulsed (see 4.5.1)	h_{FE3}			
2N4399		I_C = -30 A dc		5		
2N5745		I_C = -20 A dc		5		
Subgroup 3						
High-temperature operation:		T_A = +150°C				
Collector to emitter cutoff current	3041	Bias condition A; V_{BE} = +1.5 V dc	I_{CEX2}			
2N4399		V_{CE} = -60 V dc			-10	mA dc
2N5745		V_{CE} = -80 V dc			-10	mA dc
Low-temperature operation:		T_A = -55°C				
Forward-current transfer ratio	3076	V_{CE} = -2 V dc; pulsed (see 4.5.1)	h_{FE4}			
2N4399		I_C = -15 A dc		7		
2N5745		I_C = -10 A dc		7		
Subgroup 4						
Pulse response	3251	Test condition A, except test circuit and pulse requirement in accordance with figure 2				
Pulse on time		See figure 2	t_{on}		1.2	µs dc
Pulse off time		See figure 2	t_{off}		2.5	µs dc

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
Subgroup 4 - Continued						
Magnitude of common-emitter small-signal short-circuit forward-current transfer ratio	3306	V_{CE} = -10 V dc; I_C = -1.0 A dc; f = 1 MHz	$\|h_{fe}\|$	4	40	
Open circuit output capacitance	3236	V_{CB} = -10 V dc; I_E = 0; 100 kHz ≤ f ≤ 1 MHz	C_{obo}		1,000	pF
Small-signal short-circuit forward-current transfer ratio	3206	V_{CE} = -10 V dc; I_C = -1.0 A dc; f = 1.0 kHz	h_{fe}	40	425	
Subgroup 5						
Safe operating area (dc operation)	3051	T_C = +25°C; t = 1 s; 1 cycle, (see figure 3)				
Test 1 (Both device type) 2N4399 2N5745		 V_{CE} = -6.67 V dc; I_C = -30 A dc V_{CE} = -10 V dc; I_C = -20 A dc				
Test 2 (Both device types)		V_{CE} = -20 V dc; I_C = -10 A dc				
Test 3 (Both device types)		V_{CE} = -40 V dc; I_C = -3 A dc				
Test 4 (Both device type) 2N4399 2N5745		 V_{CE} = -50 V dc; I_C = -600 mA dc V_{CE} = -60 V dc; I_C = -600 mA dc				
Electrical measurements		See subgroup 2, herein for I_{CEX1} and h_{FE2}				

See footnote at end of table.

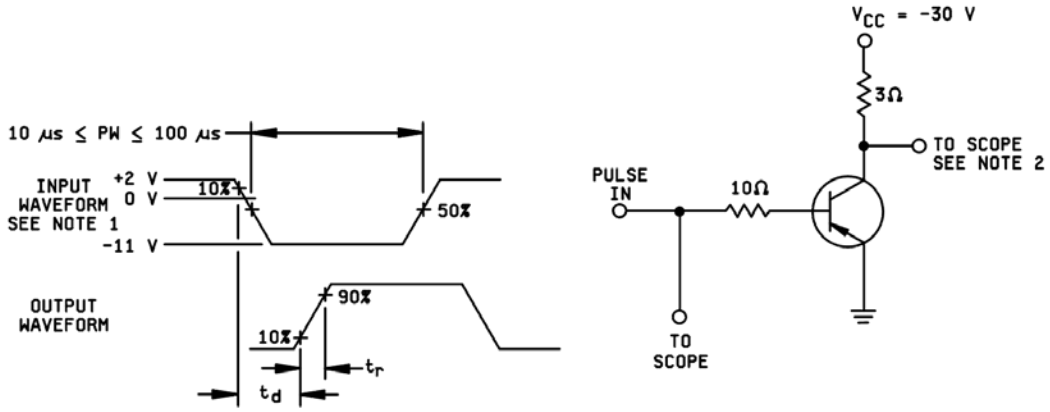
TABLE I. Group A inspection - Continued.

	Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
	Subgroup 5 - continued						
	Safe operating area (unclamped inductive load)	3053	Load condition C; (see figure 4); T_C = +25°C; duty cycle ≤ 10 percent; R_s = .01Ω; $t_r = t_f \leq 500$ ns.				
	Test 1 (Both device types)		t_p = 5 ms (vary to obtain I_C); V_{BB2} = 0; R_{BB1} = 10Ω; L = 2 mH; V_{BB1} = -10 V dc; R_{BB2} = infinity; I_C = -10 A dc; V_{CC} = -15 V dc.				
	Safe operating area (unclamped inductive load) - continued	3053	Load condition C; (see figure 4); T_C = +25°C; duty cycle ≤ 10 percent; R_s = .01Ω; $t_r = t_f \leq 500$ ns.				
	Test 2 (Both device types)		t_p = 5 ms (vary to obtain I_C); V_{BB2} = 0; V_{BB1} = -10 V dc; R_{BB1} = 100Ω; L = 40 mH; R_{BB2} = infinity; I_C = -1 A dc; V_{CC} = -15 V dc.				
*	Safe operating area, clamped (switching destructive)	3053	Load condition C; V_{CC} = -55 V dc; T_A = +25°C; L = 20 mH; (see figures 5 and 6)				
	2N4399		Clamped voltage = -60 V dc; I_C = -30 A dc				
	2N5745		Clamped voltage = -80 V dc; I_C = -20 A dc				
	Subgroups 6 and 7						
	Not applicable						

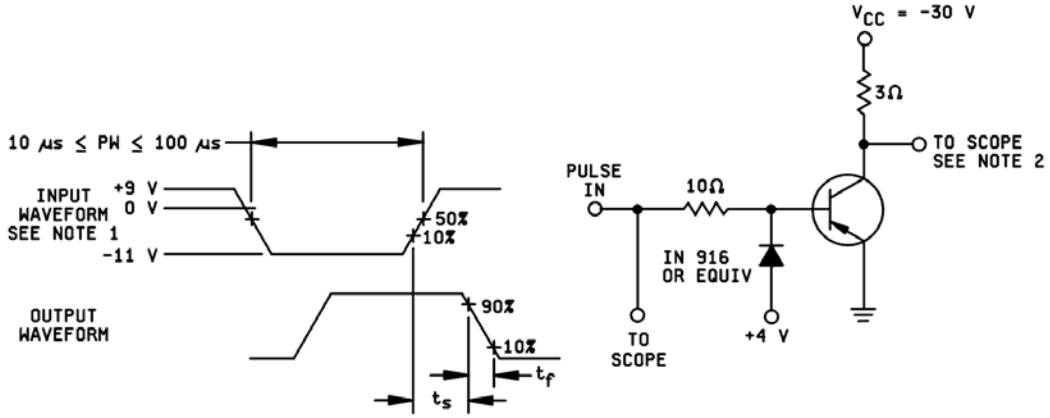
1/ For sampling plan see MIL-PRF 19500.

* TABLE II. Group E inspection (all quality levels) - for qualification and re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
Subgroup 1			45 devices c = 0
Temperature cycling	1051	Condition G, 500 cycles	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table I, subgroup 2.	
Subgroup 2			45 devices c = 0
Blocking life	1048	Test temperature = +125°C; T = 1,000 hrs, V_{CB} = 80 percent rated voltage (see 1.3).	
Electrical measurements		See table I, subgroup 2.	
Subgroup 4			N/A
Thermal impedance curves		See MIL-PRF-19500.	
Subgroup 8			45 devices c = 0
Reverse stability	1033	Condition B	



TURN-ON (t_{on}) TIME TEST CIRCUIT A



TURN-OFF (t_{off}) TIME TEST CIRCUIT B

NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics: $t_r \leq 20$ µs, $t_f \leq 1$µs, 10µs ≤ PW ≤ 100µs, $Z_{OUT} = 50\Omega$, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics: $t_r \leq 2$ µs, $Z_{IN} \geq 100$ kΩ, $C_{IN} \leq 12$ pF.
3. Test circuit A for t_d and t_r; test circuit B for t_s and t_f.
4. $t_{on} = t_d + t_r$, $t_{off} = t_s + t_f$

FIGURE 2. Pulse response test circuit.

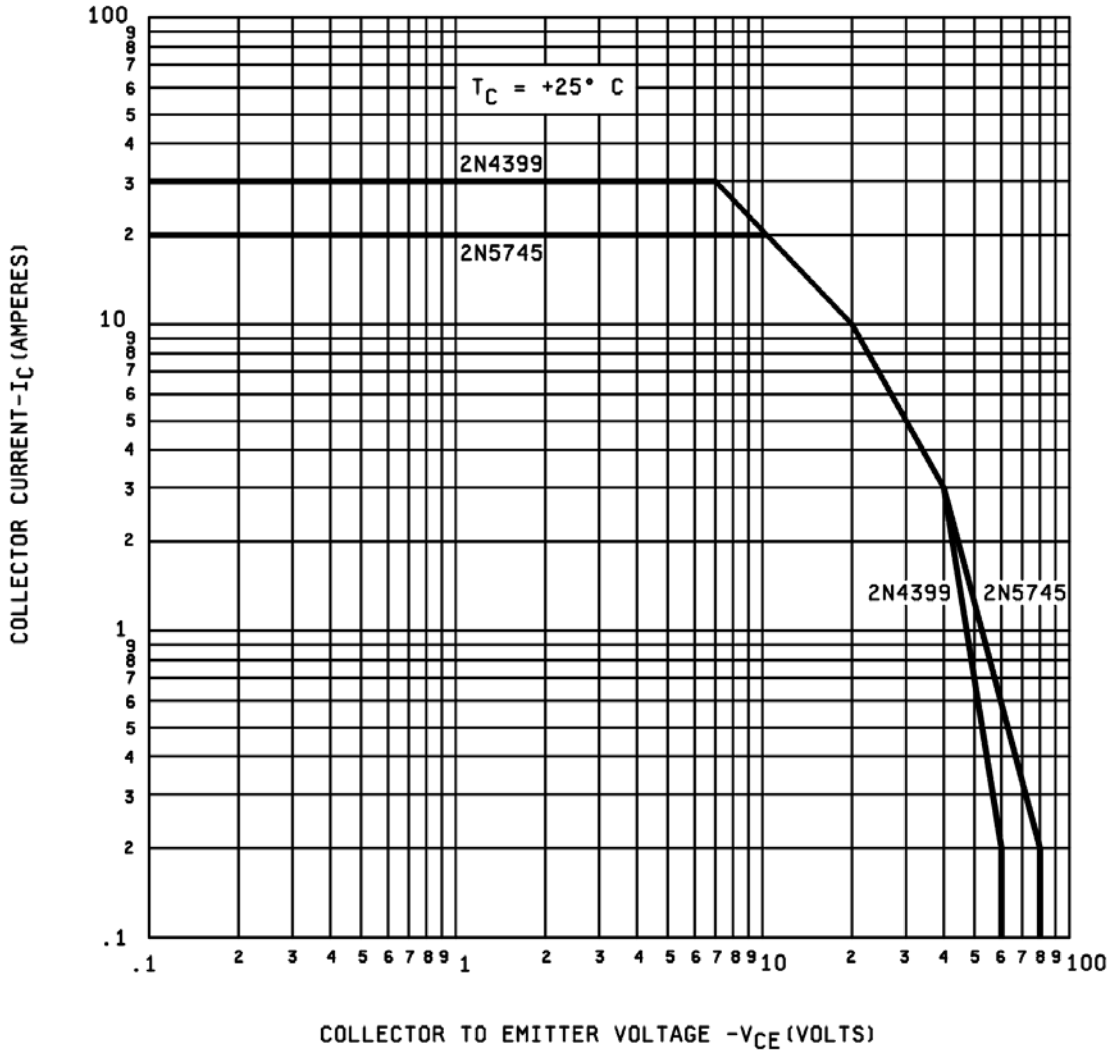


FIGURE 3. Maximum safe operating area graph (continuous dc).

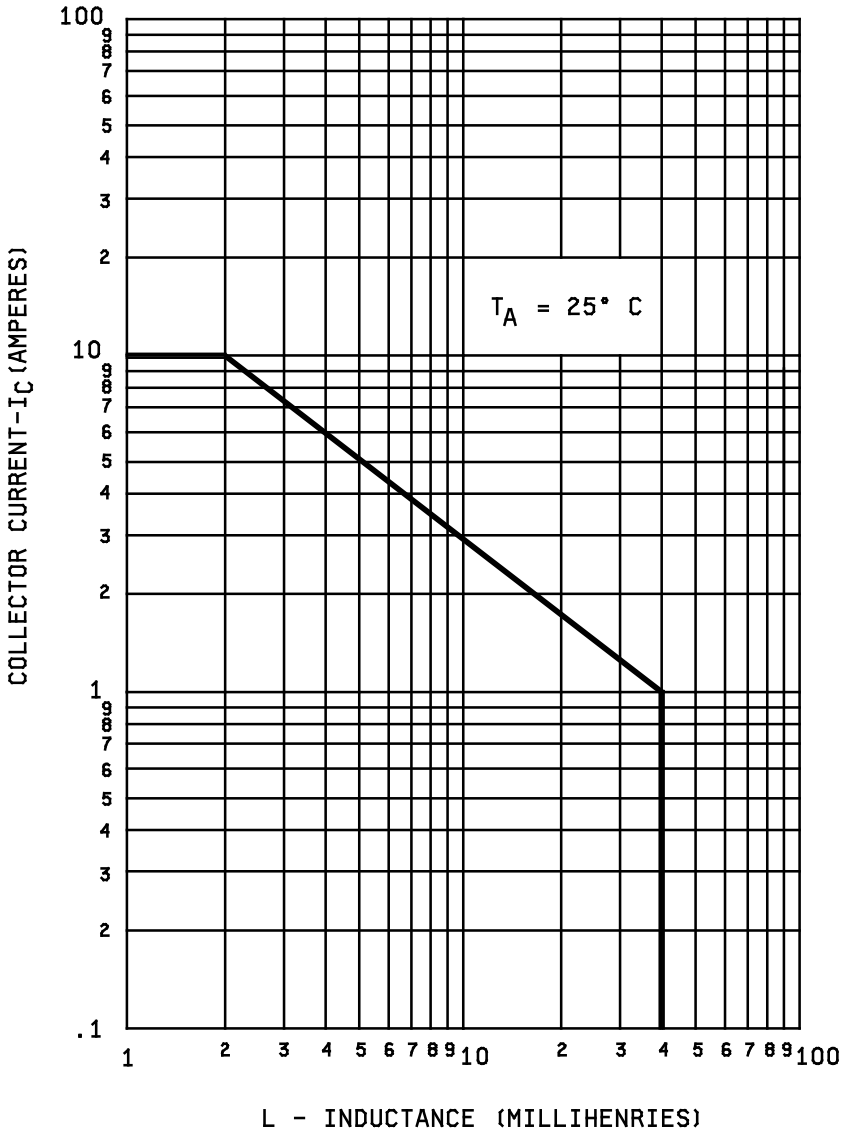
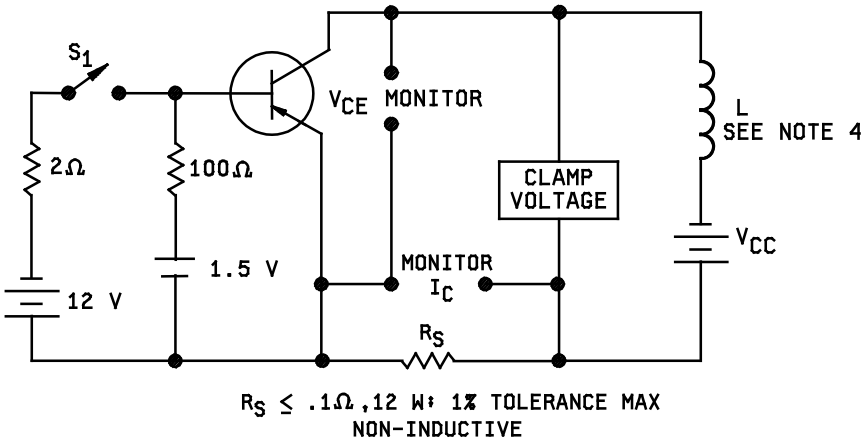


FIGURE 4. Safe operating area for switching between saturation and cutoff (unclamped inductive load).



NOTES:
1. With switch S1 closed, set the specified test conditions.
2. Open S1. Device fails if clamp voltage not reached.
3. Perform specified end-points tests.
4. L = 2.0 mH (2 each 1 mH, 50 A, .001Ω, Sanford Miller CK-50, or equivalent).

FIGURE 5. Clamped inductive sweep test circuit.

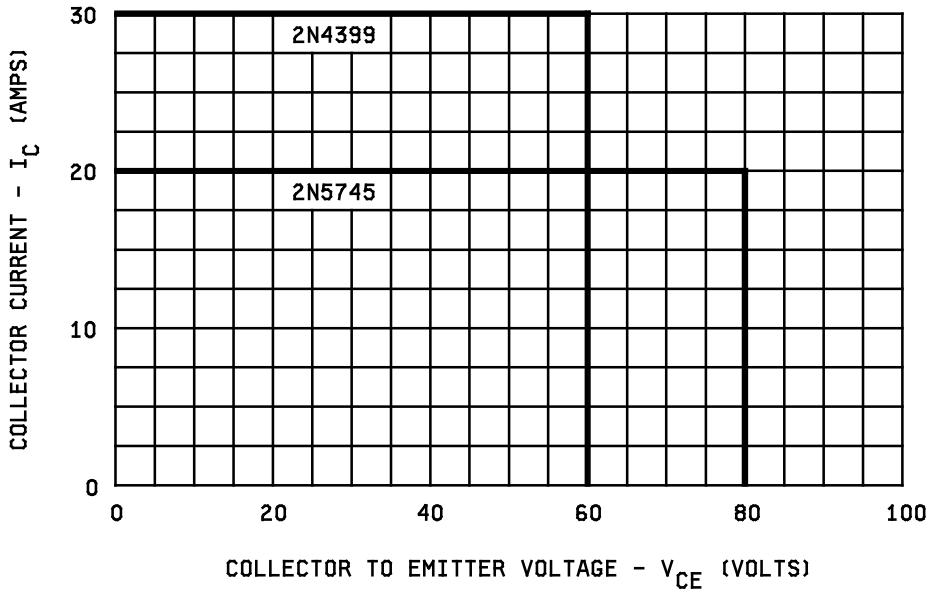


FIGURE 6. Safe operating area for switching between saturation and cutoff (clamped inductive load).

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use The notes specified in MIL-PRF-19500 are applicable to this specification.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1).

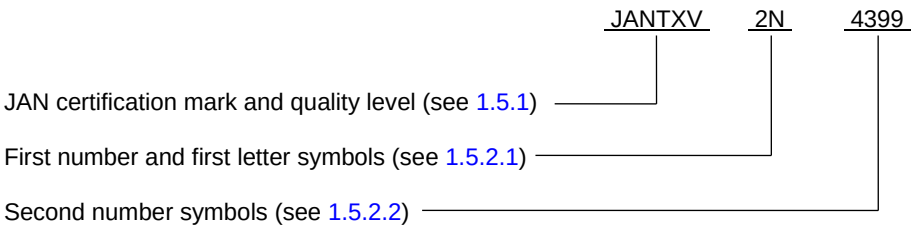
c. Lead finish (see 3.4.1).

* d. The complete PIN, see 1.5 and 6.5.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at https://assist.dla.mil.

* 6.4 PIN construction example.

* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



* 6.5 List of PINs.

* 6.5.1 List of PINs for encapsulated devices. The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N4399	JANTX2N4399	JANTXV2N4399	JANS2N4399
JAN2N5745	JANTX2N5745	JANTXV2N5745	JANS2N5745

* 6.6 Request for new types and configurations. Requests for new device types or configurations for inclusions in this specification sheet should be submitted to: DLA Land and Maritime, ATTN: VAC, Post Office Box 3990, Columbus, OH 43218-3990 or by electronic mail at Semiconductor@.dla.mil or by facsimile (614) 693-1642 or DSN 850-6939.

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Review activities:
Army - MI, SM
Navy - AS, MC
Air Force - 19

Preparing activity:
DLA - CC

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* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at https://assist.dla.mil.