

The documentation and process conversion measures necessary to comply with this document shall be completed by 3 September 2012.

INCH-POUND

MIL-PRF-19500/421H  
 3 June 2012  
 SUPERSEDING  
 MIL-PRF-19500/421G  
 w/AMENDMENT 1  
 12 October 2009

PERFORMANCE SPECIFICATION SHEET

SEMICONDUCTOR DEVICE, DUAL TRANSISTOR, UNITIZED, NPN/PNP,  
 COMPLEMENTARY, SILICON, TYPES 2N3838, 2N4854, AND 2N4854U,  
 JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments  
 and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of  
 this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for unitized, dual transistors which contain a pair of electrically isolated complementary NPN and PNP silicon triode transistors in one package. Three levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Polarity designation. Voltages and currents of limits and test conditions shown herein apply to the NPN transistor. For the PNP transistor, the values are the same, but the polarity designations are the opposite.

1.3 Physical dimensions. See figures 1 (6 lead flatpak), 2 (similar to TO-78), and 3 (surface mount).

\* 1.4 Maximum ratings.

Types	P <sub>T</sub> at T <sub>A</sub> = +25°C		R <sub>θJA</sub>		P <sub>T</sub> at T <sub>C</sub> = +25°C (1)		R <sub>θJsp</sub>		T <sub>J</sub> and T <sub>STG</sub>
	One transistor	Total device	One transistor	Total device	One transistor	Total device	One transistor	Total device	
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>°C/W</u>	<u>°C</u>
2N3838	(2) 0.25	(2) 0.35	350	290	(3) 0.7	(3) 1.4	250	125	-65 to +200
2N4854	(4) 0.30	(4) 0.60	350	290	(5) 1.0	(5) 2.0	175	87	
2N4854U	0.30	0.60	350	290	1.0	2.0	(6) 110	(6) 90	

Types	V <sub>1C-2C</sub>	Lead to case voltage	I <sub>C</sub>	T <sub>J</sub>	V <sub>CB0</sub>	V <sub>EBO</sub>	V <sub>CEO</sub>
	<u>V dc</u>	<u>V dc</u>	<u>mA dc</u>	<u>°C</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>
2N3838	±120	±120	600	200	60	5	40
2N4854, 2N4854U	±120	±120	600	200	60	5	40

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.daps.dla.mil>.

1.4 Maximum ratings. – Continued.

- (1)  $T_C$  rating does not apply to surface mount devices (2N4854U).
- (2) For  $T_A > +25^\circ\text{C}$ , derate linearly 1.43 mW/ $^\circ\text{C}$  one transistor, 2.00 mW/ $^\circ\text{C}$  both transistors.
- (3) For  $T_C > +25^\circ\text{C}$ , derate linearly 4.0 mW/ $^\circ\text{C}$  one transistor, 8.0 mW/ $^\circ\text{C}$  both transistors.
- (4) For  $T_A > +25^\circ\text{C}$ , derate linearly 1.71 mW/ $^\circ\text{C}$  one transistor, 3.43 mW/ $^\circ\text{C}$  both transistors.
- (5) For  $T_C > +25^\circ\text{C}$ , derate linearly 5.71 mW/ $^\circ\text{C}$  one transistor, 11.43 mW/ $^\circ\text{C}$  both transistors.
- (6) For U package the thermal resistance is  $R_{\theta\text{SP}}$ .

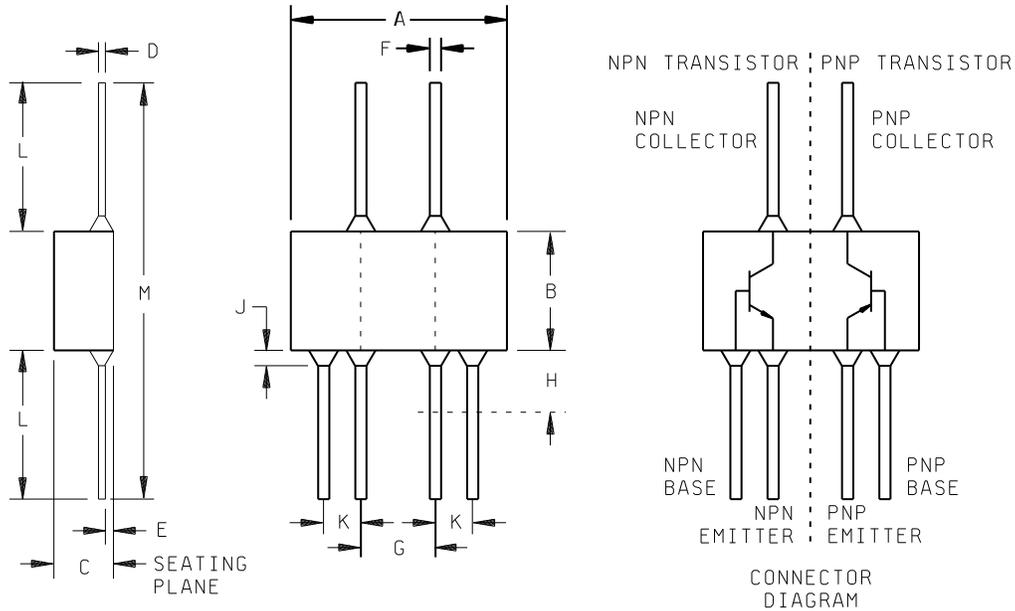
1.5 Primary electrical matching characteristics of each individual section. Characteristics apply to all case outlines.

	$h_{FE5}$ (1) $V_{CE} = 10\text{ V dc}$ $I_C = 150\text{ mA dc}$	$h_{FE4}$ (1) $V_{CE} = 10\text{ V dc}$ $I_C = 10\text{ mA dc}$	$h_{FE2}$ $V_{CE} = 10\text{ V dc}$ $I_C = 100\ \mu\text{A dc}$	$V_{CE(\text{sat})}$ (1) $I_B = 15\text{ mA dc}$ $I_C = 150\text{ mA dc}$	$V_{BE(\text{sat})}$ (1) $I_B = 15\text{ mA dc}$ $I_C = 150\text{ mA dc}$
Min	100	75	35	<u>V dc</u>	<u>V dc</u>
Max	300			0.4	0.80 1.25

	$ h_{fe} $ $V_{CE} = 10\text{ V dc}$ $I_C = 20\text{ mA dc}$ $f = 100\text{ MHz}$	$C_{\text{obo}}$ $V_{CB} = 10\text{ V dc}$ $I_E = 0$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	Non-latching $V_{CE}$ (2)	$t_{(\text{on})}$ See <a href="#">figure 4</a>	$t_{(\text{off})}$ See <a href="#">figure 5</a>	$t_{\text{on}} + t_{\text{off}}$ See <a href="#">figure 6</a>
Min	2	<u>pF</u>	<u>V dc</u>	<u>ns</u>	<u>ns</u>	<u>ns</u>
Max	10	8	40	45	300	18

- (1) Pulsed (see [4.5.1](#)).
- (2) See [4.5.2](#).

MIL-PRF-19500/421H



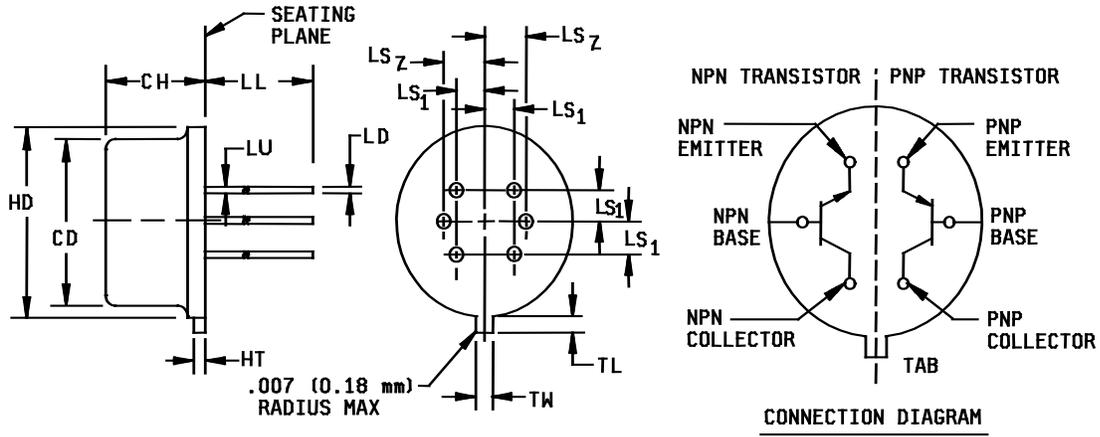
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.240	.290	6.10	7.37	
B	.115	.160	2.92	4.06	
C	.030	.080	0.76	2.03	
D	.003	.006	0.08	0.15	4
E	.005	.035	0.13	0.89	
F	.010	.019	0.25	0.48	4, 6

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
G	.100 TP		2.54 TP		6, 7
H		.050		1.27	
J		.015		0.38	5
K	.050 TP		1.27 TP		6, 7
L	.070	.250	1.78	6.35	3, 4
M	.260	.650	6.60	16.51	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Maximum limit of this dimension does not apply to device supplied in a carrier.
4. All six leads.
5. Lead dimensions are uncontrolled in this zone.
6. Dimensions "F", "G", and "K" to be measured in zone "H".
7. Leads within .005 inch (0.13 mm) total of true position (TP) at "H" with maximum material condition.
8. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

FIGURE 1. Physical dimensions of transistor type 2N3838 (all quality levels).



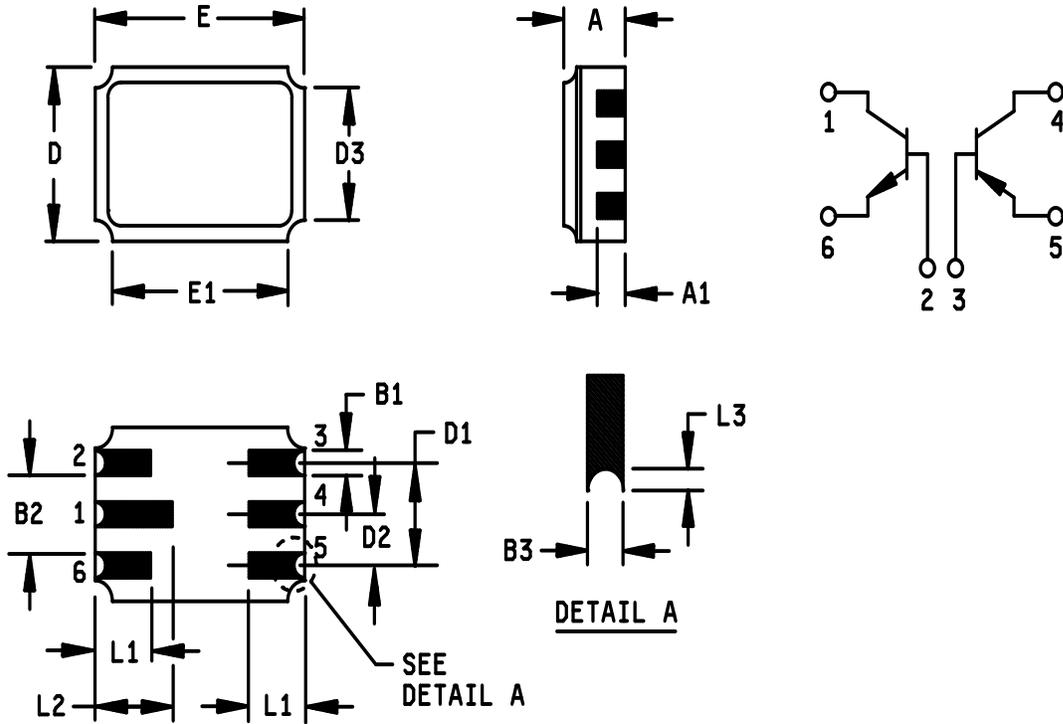
Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.140	.260	3.56	6.60	
HD	.335	.370	8.51	9.40	
HT	.009	.125	0.23	3.18	
LD	.016	.021	0.41	0.53	3, 7
LL	.500	1.750	12.70	44.45	7

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
LS1	.0707 Nom.		1.796 Nom.		5
LS2	.1000 Nom.		2.540 Nom.		5
LU	.016	.019	0.41	0.48	4, 7
TL	.029	.045	0.74	1.14	6
TW	.028	.034	0.71	0.86	

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Measured in the zone beyond .250 inch (6.35 mm) from the seating plane.
4. Measured in the zone .050 inch (1.27 mm) and .250 inch (6.35 mm) from the seating plane.
5. When measured in a gauging plane .054 +.001, -.000 inch (1.37 +0.03, -0.00 mm) below the seating plane of the transistor, maximum diameter leads shall be within .007 inch (0.18 mm) of their true location relative to a maximum width tab. Smaller diameter leads shall fall within the outline of the maximum diameter lead tolerance.
6. Measured from the maximum diameter of the actual device.
7. All six leads.
8. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

FIGURE 2. Physical dimensions of transistor type 2N4854 (all quality levels, similar to TO-78).



Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
A	.058	.100	1.47	2.54
A <sub>1</sub>	.026	.039	0.66	0.99
B <sub>1</sub>	.022	.028	0.56	0.71
B <sub>2</sub>	.072 Ref.		1.83 Ref.	
B <sub>3</sub>	.006	.022	0.15	0.56
D	.165	.175	4.19	4.45
D <sub>1</sub>	.095	.105	2.41	2.67

Ltr	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
D <sub>2</sub>	.045	.055	1.14	1.40
D <sub>3</sub>		.175		4.45
E	.240	.250	6.10	6.35
E <sub>1</sub>		.250		6.35
L <sub>1</sub>	.060	.070	1.52	1.78
L <sub>2</sub>	.082	.098	2.08	2.49
L <sub>3</sub>	.003	.007	0.08	0.18

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The coplanarity deviation of all terminal contact points, as defined by the device seating plane, shall not exceed .006 inch (0.15 mm) for solder dipped leadless chip carriers.

FIGURE 3. Physical dimensions of transistor type 2N4854U.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch> or <https://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500 and as follows:

$V_{1C-2C}$ .....Voltage difference between the collector of transistor one and that of transistor two.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500, and figures 1 (flat pack), 2 (similar to TO-78) and 3 (surface mount) herein.

3.4.1 Lead finish. Lead finish shall be solderable as defined in MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.4, 1.5, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be the subgroups specified in tables I and II herein.

MIL-PRF-19500/421H

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement
	JANTX and JANTXV levels
(1) 3c	Thermal impedance (see 4.3.2)
9	Not applicable
10	48 hours minimum
11	$I_{CB02}$ and $h_{FE5}$
12	Burn-in (see 4.3.1) 80 hours minimum
13	Subgroup 2 of table I herein; $\Delta I_{CB02}$ = 100 percent of initial value or 25 nA dc; whichever is greater for the 2N3838. $\Delta I_{CB02}$ = 100 percent of initial value or 5 nA dc; whichever is greater for the 2N4854, 2N4854U. $\Delta h_{FE5}$ = 15 percent of initial value.
14	Required

(1) Shall be performed anytime after temperature cycling, screen 3a.

MIL-PRF-19500/421H

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:  $V_{CB} = 10 - 30$  V dc  $T_A =$  room ambient as defined in the general requirements of MIL-STD-750, (see 4.5).

- 2N3838:  $P_T = 175$  mW each transistor (350 mw total device).
- 2N4854:  $P_T = 300$  mW each transistor (600 mW total device).
- 2N4854U:  $P_T = 300$  mW each transistor (600 mW total device).

NOTE: No heat sink or forced air-cooling on the devices shall be permitted.

4.3.2 Thermal impedance ( $Z_{\theta JX}$  measurements). The  $Z_{\theta JX}$  measurements shall be performed in accordance with method 3131 of MIL-STD-750.

- a.  $I_H$  forward heating current ..... 200 mA.minimum.
- b.  $I_M$  measurement current..... 5 mA.
- c.  $t_H$  heating time..... 25 -30 ms.
- d.  $t_{MD}$  measurement delay time..... 60  $\mu$ s maximum.
- e.  $V_{CE}$  collector to emitter ..... 10 V.

The maximum limit for  $Z_{\theta JX}$  under these conditions are  $Z_{\theta JX}$  (maximum) = 45°C/W.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein. If alternate screening is being performed in accordance with MIL-PRF-19500, a sample of screened devices shall be submitted to and pass the requirements of group A1 and A2 inspection only (table E-VIb, group B, subgroup 1 is not required to be performed again if group B has already been satisfied in accordance with 4.4.2).

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in 4.4.2.1 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.1 and shall be in accordance with table I, subgroup 2 herein.

4.4.2.1 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of MIL-PRF-19500 shall apply. In addition, all catastrophic failures during conformance inspection shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot and /or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failure mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1039	Steady-state life: Test condition B, 1,000 hours minimum, $V_{CB} = 10$ dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated $P_T$ as defined in 1.4. $n = 45$ devices, $c = 0$ .
2	1039	HTRB: Test condition A, 48 hours minimum. $n = 45$ devices, $c = 0$ .
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$ . $n = 22$ , $c = 0$ .

4.4.2.2 Group B sample selection. Samples selected for group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. See MIL-PRF-19500.
- b. Shall be chosen from an inspection lot that has been submitted to and passed [table I](#), subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the test and conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and [4.4.3.1](#) (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) requirements shall be in accordance with [table I](#), subgroup 2 herein.

4.4.3.1 Group C inspection, table E-VII of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition E, not applicable to U.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ , see <a href="#">1.4</a> .
C6	1026	Not applicable.

4.4.3.2 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes group A tests for conformance inspection. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in [table II](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurements shall be as specified in section 4 of MIL-STD-750.

4.5.2 Testing of units. All specified electrical tests, including end-point tests, shall be performed equally on both sections of the transistor types covered herein, except where the electrical characteristic being evaluated applies to the transistor as a device entity.

MIL-PRF-19500/421H

\* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071					
Solderability <u>3/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/</u>	1051	Test condition C, 25 cycles n = 22 devices, c = 0				
Hermetic seal Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements	2037	<a href="#">Table I</a> , subgroup 2				
* Bond strength <u>3/</u>		Precondition T <sub>A</sub> = +300°C at t = 2 hrs, n = 11 wires, c = 0				
<u>Subgroup 2</u>						
Thermal impedance	3131	See <a href="#">4.3.2</a>	Z <sub>θJX</sub>			°C/W
Collector to base cutoff current	3036	Bias condition D; V <sub>CB</sub> = 60 V dc	I <sub>CBO1</sub>		10	μA dc
Breakdown voltage, collector to emitter	3011	Bias condition D; I <sub>C</sub> = 10 mA dc; pulsed (see <a href="#">4.5.1</a> )	V <sub>(BR)CEO</sub>	40		V dc
Emitter to base cutoff current	3061	Bias condition D; V <sub>EB</sub> = 5 V dc	I <sub>EBO1</sub>		10	μA dc
Collector to base cutoff current	3036	Bias condition D; V <sub>CB</sub> = 50 V dc	I <sub>CBO2</sub>			
2N3838					50	nA dc
2N4854					10	nA dc
2N4854U					10	nA dc
Emitter to base cutoff current	3061	Bias condition D; V <sub>EB</sub> = 3 V dc	I <sub>EBO2</sub>		10	nA dc
Forward-current transfer ratio	3076	V <sub>CE</sub> = 1 V dc; I <sub>C</sub> = 150 mA dc; pulsed (see <a href="#">4.5.1</a> )	h <sub>FE1</sub>	50		
Forward-current transfer ratio	3076	V <sub>CE</sub> = 10 V dc; I <sub>C</sub> = 100 μA dc	h <sub>FE2</sub>	35		
Forward-current transfer ratio	3076	V <sub>CE</sub> = 10 V dc; I <sub>C</sub> = 1.0 mA dc	h <sub>FE3</sub>	50		

See footnotes at end of table.

MIL-PRF-19500/421H

\* TABLE I. Group A inspection - Continued.

Inspection 1/  	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2 - Continued.</u>						
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc};$ pulsed (see 4.5.1)	$h_{FE4}$	75		
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 150 \text{ mA dc}$ pulsed (see 4.5.1)	$h_{FE5}$	100	300	
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 300 \text{ mA dc};$ pulsed (see 4.5.1)	$h_{FE6}$	35		
Base emitter saturation voltage	3066	Test condition A; $I_B = 15 \text{ mA dc};$ $I_C = 150 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{BE(sat)}$	0.80	1.25	V dc
Collector to emitter saturation voltage	3071	$I_B = 15 \text{ mA dc}; I_C = 150 \text{ mA dc};$ pulsed (see 4.5.1)	$V_{CE(sat)}$		0.40	V dc
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
* Collector to base cutoff current	3036	Bias condition D; $V_{CB} = 50 \text{ V dc}$	$I_{CBO3}$		10	$\mu\text{A dc}$
Low temperature operation:	3076	$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}; I_C = 10 \text{ mA dc}$	$h_{FE7}$	12		
<u>Subgroup 4</u>						
Small-signal short-circuit forward current transfer ratio	3206	$V_{CE} = 10 \text{ V dc}; I_C = 1 \text{ mA dc};$ $f = 1 \text{ kHz}$	$h_{fe}$	60	300	
Small-signal common emitter input impedance	3201	$V_{CE} = 10 \text{ V dc}; I_C = 1 \text{ mA dc};$ $f = 1 \text{ kHz}$	$h_{ie}$	1.5	9	$\text{k}\Omega$
Small-signal common emitter output admittance	3216	$V_{CE} = 10 \text{ V dc}; I_C = 1 \text{ mA dc};$ $f = 1 \text{ kHz}$	$h_{oe}$		50	$\mu\text{hmo}$
Magnitude of small-signal short-circuit forward current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}; I_C = 20 \text{ mA dc};$ $f = 100 \text{ MHz}$	$ h_{fe} $	2	10	
Open circuit output capacitance	3236	$V_{CB} = 10 \text{ V dc}; I_E = 0;$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	$C_{obo}$		8	pF

See footnotes at end of table.

MIL-PRF-19500/421H

\* TABLE I. Group A inspection - Continued.

	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4 - Continued.</u>						
Noise figure	3246	$V_{CE} = 10 \text{ V dc}; I_C = 100 \mu\text{A dc};$ $f = 1 \text{ kHz}; R_G = 1 \text{ k}\Omega$	NF		8	dB
Turn-on time		See <a href="#">figure 7</a>	$t_{on}$		45	ns
Turn-off time		See <a href="#">figure 8</a>	$t_{off}$		300	ns
Pulse response		See <a href="#">figure 9</a>	$t_{on} + t_{off}$		18	ns
Collector emitter nonlatching voltage		See <a href="#">figure 10</a>	$V_{CE}$	40		V dc
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup 1, double the sample size of the failed test or sequence of tests. A failure in [table I](#), subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for laser marked devices.

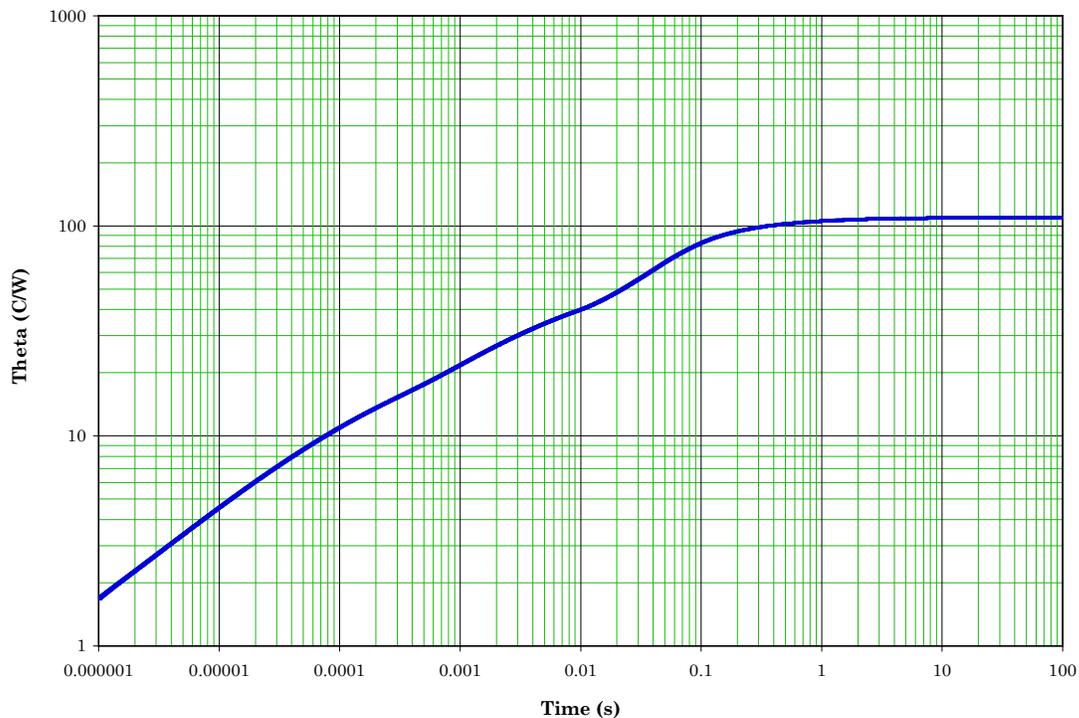
MIL-PRF-19500/421H

\* TABLE II. Group E inspection (all quality levels) - for qualification and re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V <sub>CB</sub> = 10 V dc, 6,000 cycles.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2 herein.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance, thermal resistance curves	3131	See table E-IX of MIL-PRF-19500, group E, subgroup 4.	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			11 devices c = 0
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition A for devices ≥ 400 V Condition B for devices < 400 V	

### Maximum Thermal Impedance

023F Half-Dual Chip LCC6 (U) Theta-JSP (Infinite Mount) Tsp=25C

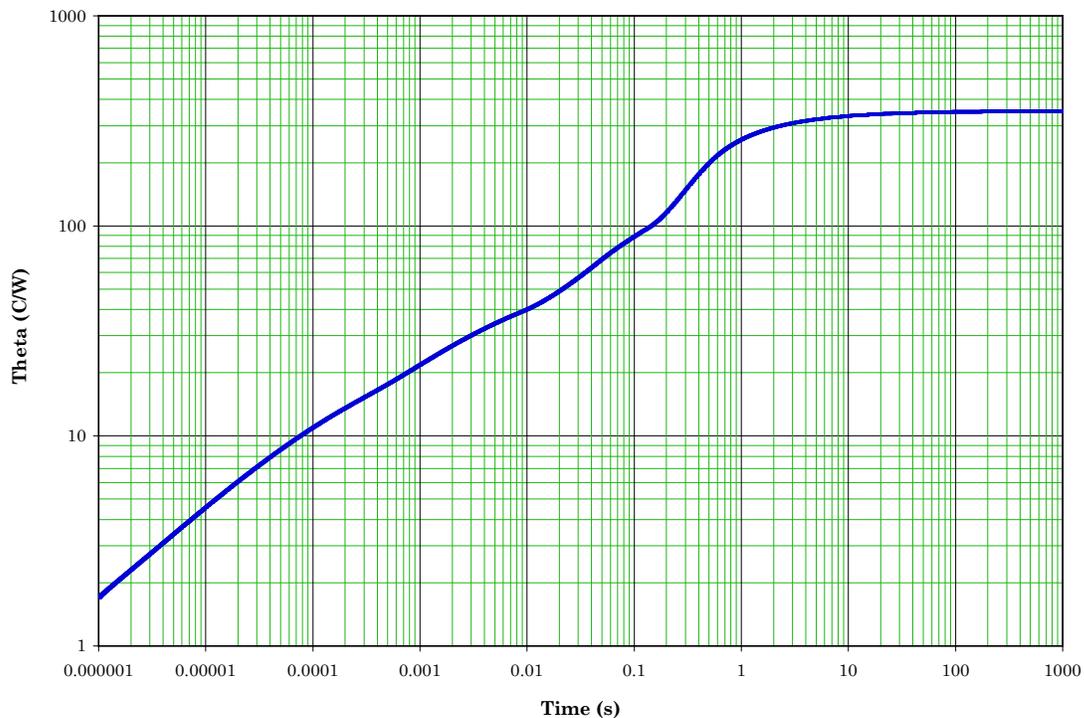


Thermal resistance = 110°C/W one side, 90°C/W both sides operating in “parallel”.  
Tsp = 25°C (Solder Pads = Infinite Sink).

\* FIGURE 4. Thermal impedance graph ( $R_{\theta JSP}$ ) for 2N4854U (U).

### Maximum Thermal Impedance

023F Dual Chip LCC6 (U) Theta-JA (FR4 PCB Mount) Ta=25C

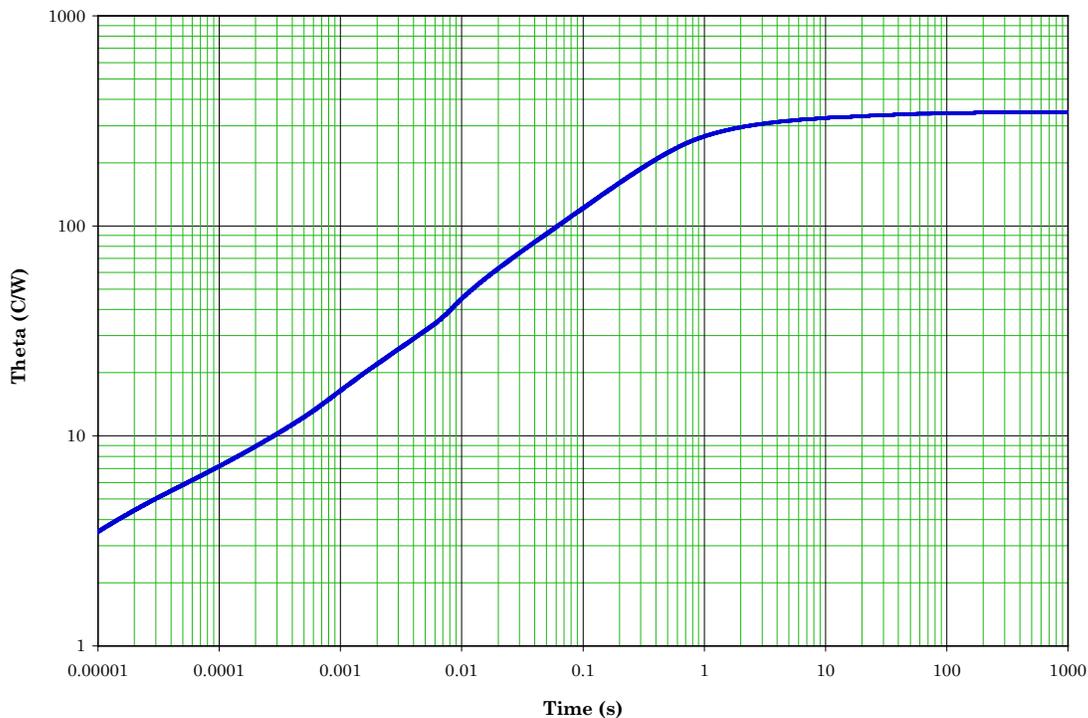


Thermal resistance = 350°C/W one side, 290°C/W both sides operating in “parallel”.  
Ta = 25°C (PCB FR4 Mounted).

\* FIGURE 5. Thermal impedance graph ( $R_{\theta JPCB}$ ) for 2N4854U (U).

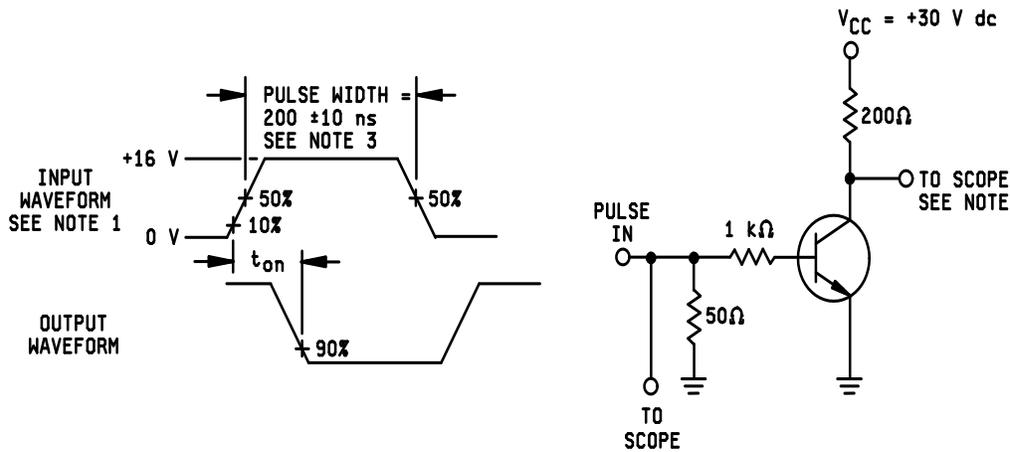
### Maximum Thermal Impedance

TO-78 with 023F Chip Thermal Impedance per Side with Other Side Equally Biased



Thermal impedance TO-78 package dual 023F chips,  
 Thermal resistance = 350°C/W one side, 290°C/W both sides operating in “parallel”.  
 $T_A = 25^\circ\text{C}$  (air cooled).

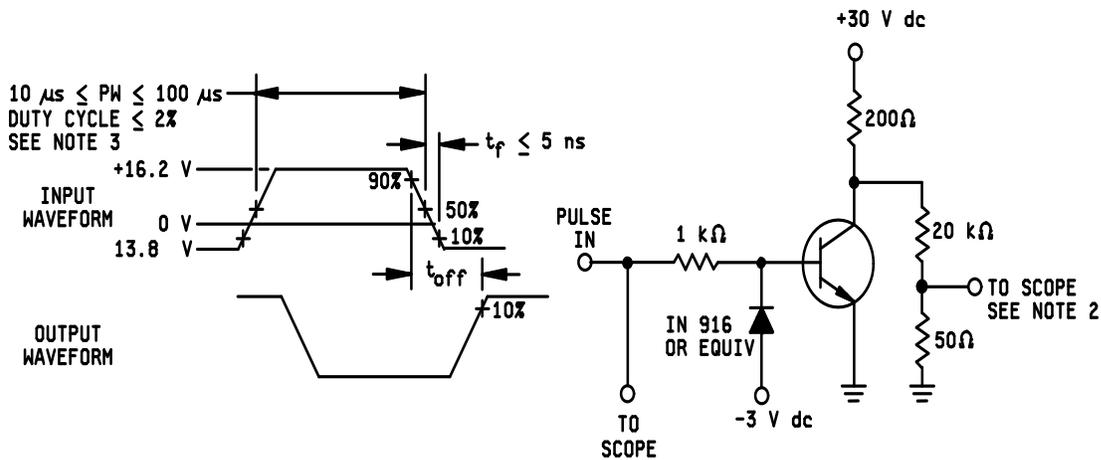
\* FIGURE 6. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N4854 (all quality levels, similar to TO-78).



NOTES:

1. The rise time ( $t_r$ ) of the applied pulse shall be  $\leq 2.0$  ns, duty cycle  $\leq 2$  percent, and the generator source impedance shall be  $50 \Omega$ .
2. Sampling oscilloscope:  $Z_{IN} \geq 100$  k $\Omega$ ,  $C_{IN} \leq 12$  pF, rise time  $\leq 0.2$  ns.
3. The signs, polarity symbols, and waveforms shown are for the NPN transistor; the signs and polarity symbols are reversed for the PNP triode (see 1.2 herein).

\* FIGURE 7. Saturated turn-on switching time test circuit.

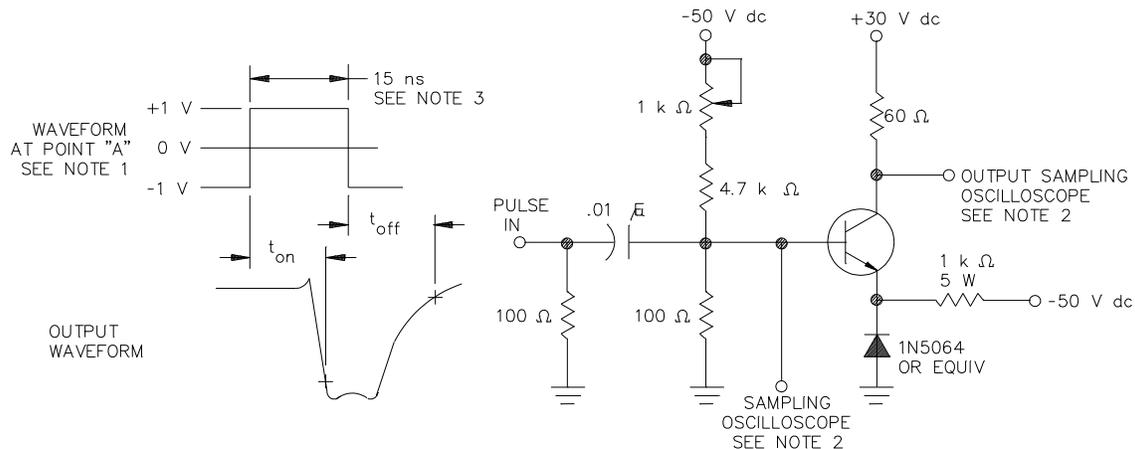


NOTES:

1. The rise time ( $t_r$ ) of the applied pulse shall be  $\leq 2.0$  ns, duty cycle  $\leq 2$  percent, and the generator source impedance shall be  $50 \Omega$ .
2. Sampling oscilloscope:  $Z_{IN} \geq 100$  k $\Omega$ ,  $C_{IN} \leq 12$  pF, rise time  $\leq 0.2$  ns.
3. The signs, polarity symbols, and waveforms shown are for the NPN transistor; the signs and polarity symbols are reversed for the PNP triode (see 1.2 herein).

\* FIGURE 8. Saturated turn-off switching time test circuit.

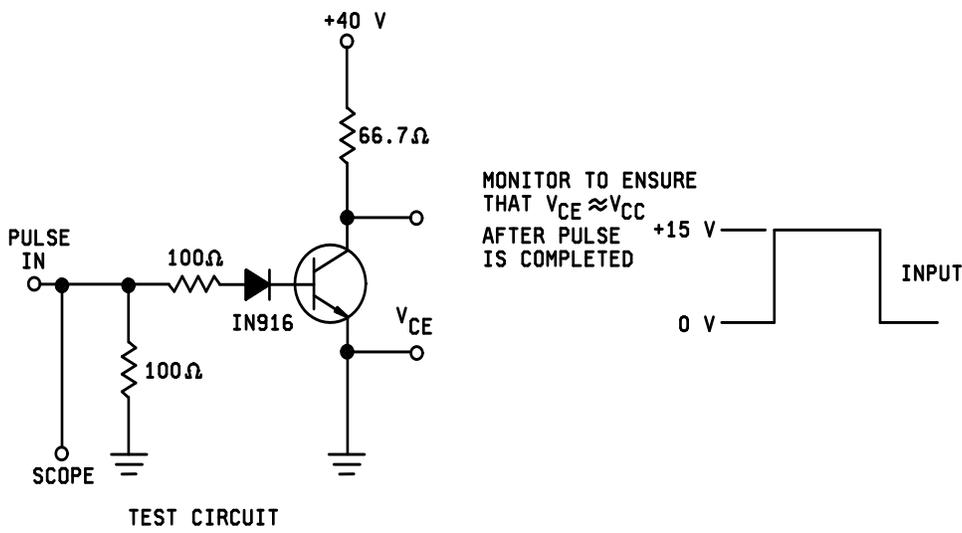
MIL-PRF-19500/421H



NOTES:

1. The rise time ( $t_r$ ) of the applied pulse shall be  $\leq 2.0$  ns, duty cycle  $\leq 2$  percent, and the generator source impedance shall be  $50 \Omega$ .
2. Sampling oscilloscope:  $Z_{IN} \geq 100 \text{ k}\Omega$ ,  $C_{IN} \leq 12 \text{ pF}$ , rise time  $\leq 0.2$  ns.
3. The signs, polarity symbols, and waveforms shown are for the NPN transistor; the signs and polarity symbols are reversed for the PNP triode (see 1.2 herein).

\* FIGURE 9. Nonsaturated switching time test circuit.



NOTE: The input waveform has the following characteristics:  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 2$  percent.

FIGURE 10. Collector emitter nonlatching voltage test circuit.

## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

\* 6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

MIL-PRF-19500/421H

Custodian:

Army - CR  
Navy - EC  
Air Force - 85  
DLA - CC

Preparing activity:

DLA - CC  
  
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Review activities:

Army - AR, MI  
Navy - MC  
Air Force - 99

\* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.daps.dla.mil>.