

The documentation and process conversion measures necessary to comply with this revision shall be completed by 10 March 2015.

INCH-POUND

MIL-PRF-19500/402G
 10 December 2014
 SUPERSEDING
 MIL-PRF-19500/402F
 12 August 2009

PERFORMANCE SPECIFICATION SHEET

* TRANSISTOR, NPN, SILICON, POWER,
 DEVICE TYPE 2N3739, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

- * 1.1 Scope. This specification covers the performance requirements for NPN, silicon, power transistors for use in particular power-switching applications. Three levels of product assurance (JAN, JANTX, and JANTXV) are provided for each device type as specified in [MIL-PRF-19500](#).
- * 1.2 Package outlines. The device package for this specification sheet is similar to TO-66 in accordance with [figure 1](#) for all packaged device types.
- * 1.3 Maximum ratings. Unless otherwise specified, $T_A = +25^\circ\text{C}$.

Types	P_T (1)	P_T (1)	$R_{\theta JC}$	V_{CBO}	V_{CEO}	V_{EBO}	I_B	I_C	T_{STG} and T_J
	$T_C = +25^\circ\text{C}$	$T_C = +100^\circ\text{C}$							
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>$^\circ\text{C}$</u>
2N3739	20	13	7.5	325	300	6.0	0.5	1.0	-55 to +200

(1) For temperature-power derating curves, see [figure 2](#).

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.

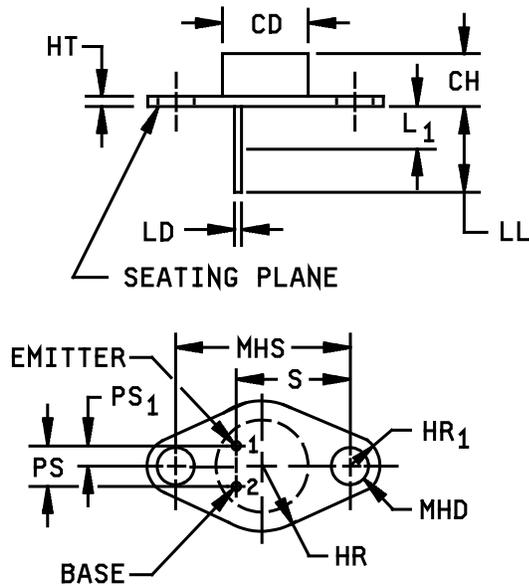
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1.4 Primary electrical characteristics at $T_A = +25^\circ\text{C}$.

Limit	h_{FE1} (1)	h_{FE3} (1)	V_{BE}	$V_{CE(SAT)2}$	C_{obo}	$ h_{fe} $	Switching	
	$V_{CE} = 10\text{ V dc}$ $I_C = 10\text{ mA dc}$	$V_{CE} = 10\text{ V dc}$ $I_C = 100\text{ mA dc}$	$V_{CE} = 10\text{ V dc}$ $I_C = 100\text{ mA dc}$	$I_C = 250\text{ mA dc}$ $I_B = 25\text{ mA dc}$	$V_{CB} = 100\text{ V dc}$ $I_E = 0\text{ mA dc}$ $100\text{ kHz} \leq f \leq 1\text{ MHz}$	$V_{CE} = 10\text{ V dc}$ $I_C = 100\text{ mA dc}$ $f = 10\text{ MHz}$	t_{on}	t_{off}
			<u>V dc</u>	<u>V dc</u>	<u>pF</u>		<u>μs</u>	<u>μs</u>
Min	30	40	1	2.5	20	1	1.5	3.5
Max		200				6		

(1) Pulsed (see 4.5.1).

- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- * 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", and "JANTXV".
- * 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
 - * 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
 - * 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "3739".
- * 1.5.3 Suffix symbols. Suffix symbols are not applicable for this specification sheet.
- * 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.620		15.75	
CH	.250	.340	6.35	8.64	
HR		.350		8.89	
HR1	.115	.145	2.92	3.68	
HT	.050	.075	1.27	1.91	
LD	.028	.034	0.71	0.86	4, 6
LL	.360	.500	9.14	12.70	
L1		.050		1.27	6
MHD	.142	.152	3.61	3.86	4
MHS	.958	.962	24.33	24.43	
PS	.190	.210	4.83	5.33	3
PS1	.093	.107	2.36	2.72	3
S	.570	.590	14.48	14.99	
Term 1	Emitter				
Term 2	Base				

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. These dimensions should be measured at points .050 inch (1.27 mm) +.005 inch (0.13 mm) -.000 inch (0.00 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.
4. Two places.
5. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
6. Lead diameter shall not exceed twice LD within L1.
7. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.
8. Pin 1 is the emitter, pin 2 is the base. The collector shall be electrically connected to the case.

FIGURE 1. Physical dimensions (similar to TO-66).

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#)- Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- * (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

* 3.4.2 Pin-out. The pin-out of the device types shall be as shown on [figure 1](#). Terminal 1 is the emitter, terminal 2 is base. The collector shall be electrically connected to the case.

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein shall be performed by the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANTX and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement
	JANTX and JANTXV levels only
(1) 3c	Thermal impedance (see 4.3.2)
9	Not applicable
11	h_{FE2} and I_{CBO1}
12	See 4.3.1
13	Subgroup 2 of table I herein, ΔI_{CBO1} = 100 percent of initial value or 1 μ A dc, whichever is greater Δh_{FE2} = ± 20 percent of initial value

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Power burn-in conditions. Power burn-in conditions are as follows: 2N3739 - V_{CB} = 10 - 30 V dc, T_J = +162.5°C \pm 12.5°C

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein. Group A inspection shall be performed on each subplot.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500 and table I herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIB (JAN, JANTX, and JANTXV), of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1037	For solder die attach: $V_{CB} \geq 10$ V dc, $T_A \leq +35^\circ\text{C}$.
	1026	For eutectic die attach: $V_{CB} = 10$ V dc, $T_A \leq +35^\circ\text{C}$ adjust P_T to achieve $T_J = +150^\circ\text{C}$ min.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in appendix E, table E-VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A, weight = 10 lbs, T = 15 seconds.
C5	3131	Thermal resistance, see 4.3.2, $R_{\theta JC(\text{max})} = 7.5^\circ\text{C/W}$.
C6	1037	For solder die attach: $V_{CB} \geq 10$ V dc. $T_A \leq +35^\circ\text{C}$.
	1026	For eutectic die attach: $V_{CB} = 10$ V dc, $T_A \leq +35^\circ\text{C}$ adjust P_T to achieve $T_J = +150^\circ\text{C}$ min.

* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

* 4.5.1 Pulse response measurements. Conditions for pulse response measurement shall be as specified in section 4 of MIL-STD-750.

* 4.5.2 Coil selection for safe operating area (SOAR) tests. In selecting coils for use in the clamped and unclamped inductive SOAR tests, prime consideration should be given to the recommended commercially available coil. However, due to the extreme critical nature of the coil in these circuits and the wide tolerance of some commercially available coils (+100%, -50%), it shall be the semiconductor manufacturer's responsibility, to prove upon request, compliance or equivalency of any coil used (commercial or in-plant designed) to be within ($\pm 20\%$) of the specified inductance at the rated current and dc resistance.

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TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3131	See 4.3.2	$Z_{\theta JX}$			°C/W
Breakdown voltage, collector to emitter	3011	Bias condition D, $I_C = 5.0$ mA dc	$V_{(BR)CEO}$	300		V dc
Collector to base cutoff current	3036	Bias condition D, $V_{CB} = 325$ V dc	I_{CBO1}		10	μA dc
Collector to emitter cutoff current	3041	Bias condition A, $V_{CE} = 300$ V dc, $V_{BE} = 1.5$ V dc	I_{CEX}		20	μA dc
Emitter to base cutoff current	3061	Bias condition D, $V_{EB} = 6.0$ V dc	I_{EBO}		0.1	mA dc
Base to emitter, non-saturated voltage	3066	Test condition B, $V_{CE} = 10$ V dc, $I_C = 100$ mA dc; pulsed (see 4.5.1)	V_{BE}		1	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 100$ mA dc; $I_B = 10$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		0.75	V dc
Collector to emitter voltage (saturated)	3071	$I_C = 250$ mA dc; $I_B = 25$ mA dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		2.5	V dc
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 10$ mA dc; pulsed (see 4.5.1)	h_{FE1}	30		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 50$ mA dc; pulsed (see 4.5.1)	h_{FE2}	30		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 100$ mA dc; pulsed (see 4.5.1)	h_{FE3}	40	200	
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 250$ mA dc; pulsed (see 4.5.1)	h_{FE4}	25		
Forward-current transfer ratio	3076	$V_{CE} = 10$ V dc; $I_C = 500$ mA dc; pulsed (see 4.5.1)	h_{FE5}	10		

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High-temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current	3036	Bias condition D, $V_{CB} = 325\text{ V dc}$	I_{CBO2}		150	$\mu\text{A dc}$
Low-temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 10\text{ V dc}$; $I_C = 100\text{ mA dc}$; pulsed (see 4.5.1)	h_{FE6}	15		
<u>Subgroup 4</u>						
Pulse response:						
Turn-on time		$V_{CC} = 150\text{ V dc}$; $I_C = 500\text{ mA dc}$; $I_B = 50\text{ mA dc}$ (see figure 3)	t_{on}		1.5	μs
Turn-off time		$V_{CC} = 150\text{ V dc}$; $I_C = 500\text{ mA dc}$; $I_{B1} = I_{B2} = 50\text{ mA dc}$ (see figure 3)	t_{off}		3.5	μs
Magnitude of common emitter, small-signal short-circuit forward-current transfer ratio	3306	$V_{CE} = 10\text{ V dc}$; $I_C = 100\text{ mA dc}$; $f = 10\text{ MHz}$	$ h_{FE} $	1.0	6	
Small-signal short-circuit forward-current transfer ratio	3206	$V_{CE} = 20\text{ V dc}$; $I_C = 100\text{ mA dc}$; $f = 1\text{ kHz}$	h_{fe}	35	300	
Open circuit output capacitance	3236	$V_{CB} = 100\text{ V dc}$; $I_E = 0\text{ mA dc}$; $100\text{ kHz} \leq f \leq 1\text{ MHz}$	C_{obo}		20	pF
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}$; $t = 1\text{ s}$; 1 cycle; (see figure 4)				
<u>Test 1</u>		$V_{CE} = 80\text{ V dc}$; $I_C = 250\text{ mA dc}$				
<u>Test 2</u>		$V_{CE} = 290\text{ V dc}$; $I_C = 6\text{ mA dc}$				

See footnotes at end of table.

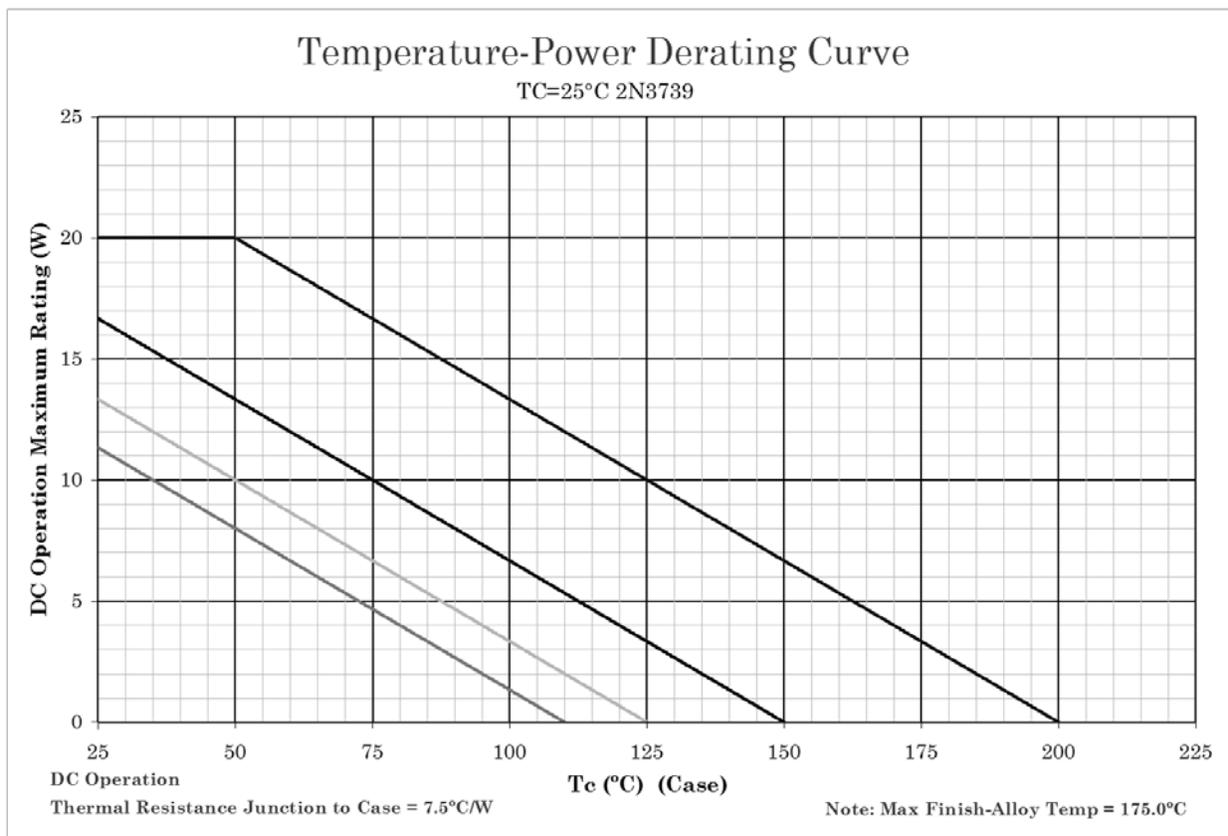
TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u> - Continued						
Safe operating area (switching)	3053	Load condition C (unclamped inductive load) (see figure 5) $T_A = +25^\circ\text{C}$; duty cycle ≤ 10 percent; $R_s = 1\Omega$; $t_r = t_f \leq 500$ ns				
<u>Test 1</u>		t_p approx 8 ms (vary to obtain I_C); $R_{BB1} = 100\Omega$; $V_{BB1} \geq 10$ V dc; $R_{BB2} = \infty$; $V_{BB2} = 0$ V dc; $V_{CC} \geq 100$ V dc; $I_C = 500$ mA dc; the coil used shall provide a minimum inductance of 3.5 mH at 500 mA with max. dc resistance of 0.5 ohm (for reference only: Acme T58220, or equivalent)				
<u>Test 2</u>		t_p approx 8 ms (vary to obtain I_C); $R_{BB1} = 100\Omega$; $V_{BB1} \geq 10$ V dc; $R_{BB2} = \infty$; $V_{BB2} = 0$ V dc; $V_{CC} \geq 100$ V dc; $I_C = 100$ mA dc; the coil used shall provide a minimum inductance of 25 mH at 100 mA with max. dc resistance of 1.0 ohm (for reference only: Triad C-48u, centertapped, or equivalent.)				
Safe operating area (switching)		$T_A = +25^\circ\text{C}$; duty cycle ≤ 10 percent; t_p approx 8 ms (vary to obtain I_C); $V_{CC} \geq 100$ V dc; $I_C = 1$ A dc; $R_s = 1\Omega$; clamp voltage = 300 V dc (see figure 6)				
Electrical measurements		See table I , subgroup 2				

1/ For sampling plan, see [MIL-PRF-19500](#).
2/ This test required for the following end-point measurements only:
 Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
 Group C, subgroup 2 and 6.
 Group E, subgroup 1.

* TABLE II. Group E inspection (all quality levels) - for qualification and re-qualification only.

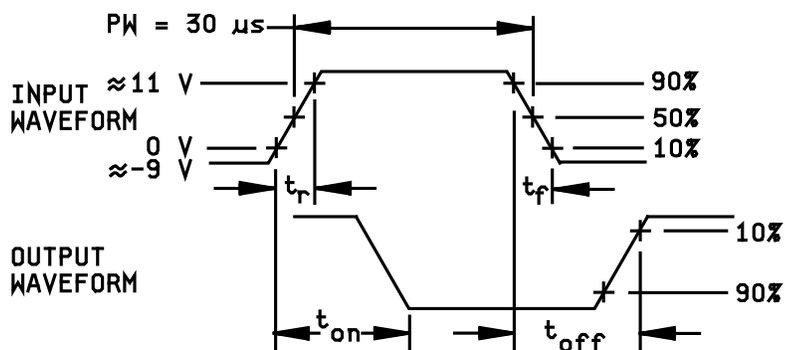
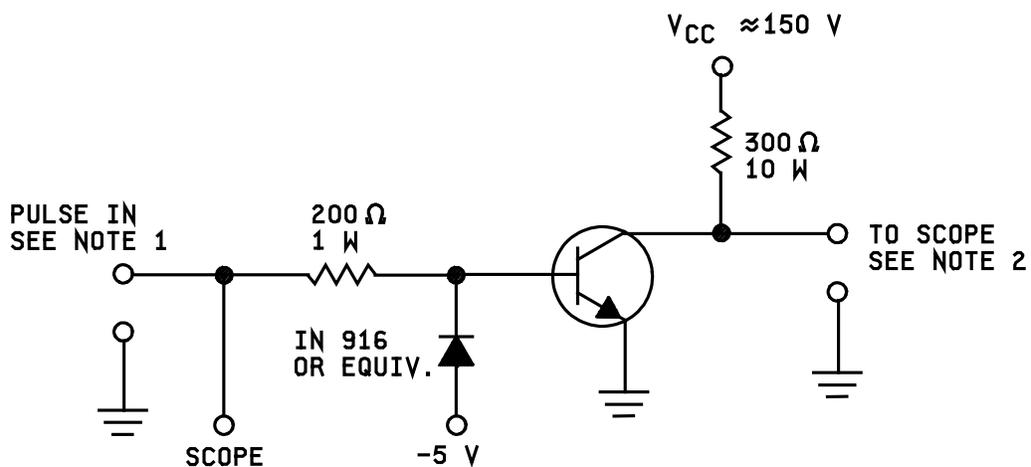
Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	500 cycles.	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 2</u>			45 devices c = 0
High temperature reverse bias	1039	Condition A, 1,000 hrs.	
Electrical measurements		See table I , subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500 .	
<u>Subgroup 5</u>			3 devices c = 0
Barometric pressure	1001	Condition B, $V_{CBO} = 325$ V dc.	
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	



NOTES:

1. Maximum theoretical derate design curve. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$ where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$ and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-power derating graph.



NOTES:

1. The rise time (t_r) and fall time (t_f) of the applied pulse shall be each ≤ 20 ns; duty cycle ≤ 1 percent; generator source impedance shall be 50 ohms.
2. Output sampling oscilloscope: $Z_{in} \geq 100$ k Ω ; $C_{in} \leq 50$ pF; rise time ≤ 2.0 ns.

FIGURE 3. Pulse response test circuit.

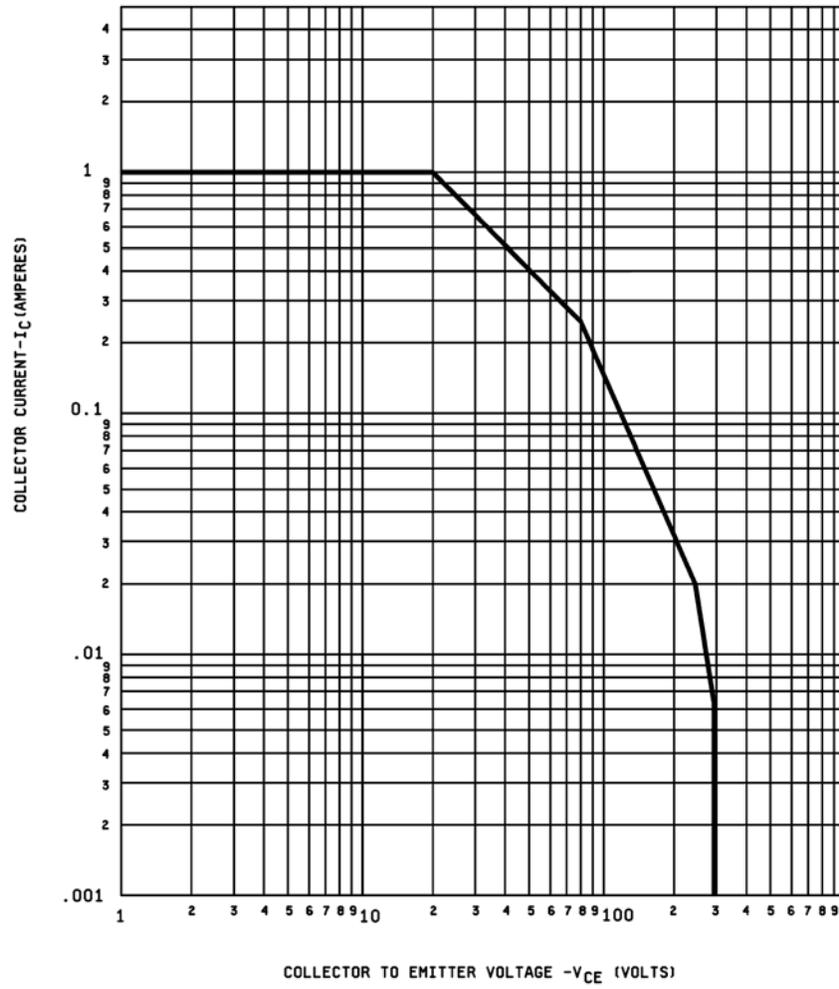


FIGURE 4. Maximum safe operating area graph (continuous dc).

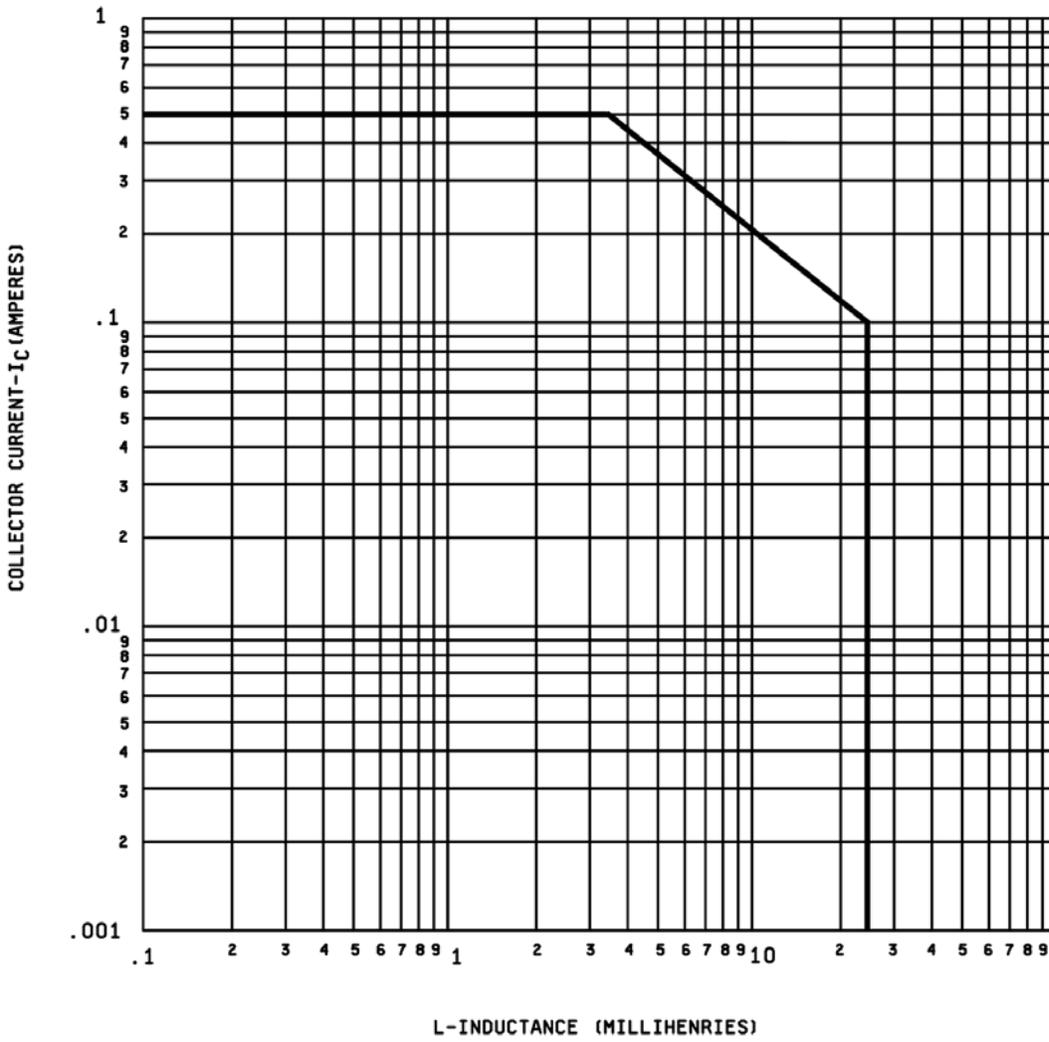
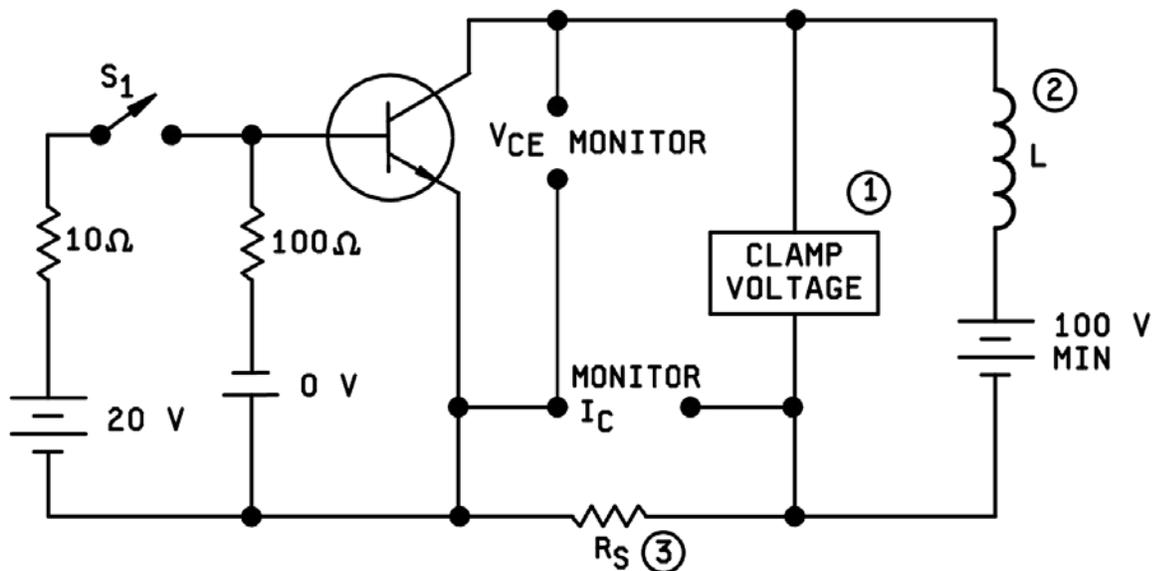


FIGURE 5. Safe operating area for switching between saturation and cutoff (unclamped inductive load).



NOTES:

1. Either a clamping circuit or clamping diode may be used.
- * 2. The coil used shall provide a minimum inductance of 25 mH at 1 A with a maximum dc resistance of 1 ohm. For reference only: Triad C-48u (center-tapped), or equivalent (see 4.5.2).
3. $R_S \leq 1$ ohm, 12 W, 1% tolerance max., (noninductive).

Procedure:

1. With switch S_1 closed, set the specified test conditions.
2. Open S_1 . Device fails if clamp voltage not reached and maintained until the current returns to zero.
3. Perform specified endpoint tests.

* FIGURE 6. Clamped inductive sweep test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

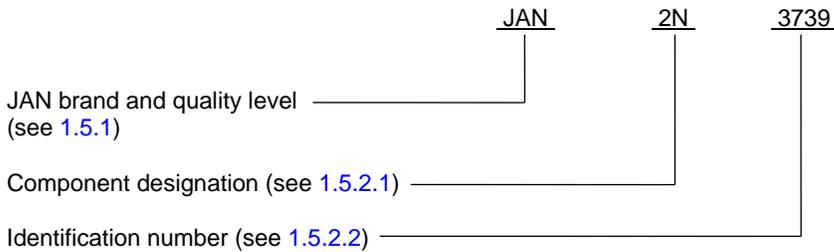
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- * d. The complete Part or Identifying Number (PIN), see 1.5 and 6.4.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

* 6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



* 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level
JAN2N3739	JANTX2N3739	JANTXV2N3739

6.6 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC

(Project 5961-2014-109)

Review activities:

Army - AR, AV, MI, SM
 Navy - AS, SH
 Air Force - 19

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.