

The documentation and process conversion measures necessary to comply with this revision shall be completed by 2 September 2015.

INCH-POUND

MIL-PRF-19500/385J  
2 June 2015  
SUPERSEDING  
MIL-PRF-19500/385H  
10 March 2009

PERFORMANCE SPECIFICATION SHEET

\* TRANSISTOR, JUNCTION FIELD EFFECT, N-CHANNEL,  
SILICON, DEVICE TYPES 2N4856 THROUGH 2N4861,  
JAN, JANTX, JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

\* 1.1 Scope. This specification covers the performance requirements for N-channel, depletion mode, silicon J-FET (Junction Field Effect transistor). Four levels of product assurance are provided for each device (JAN, JANTX, JANTXV, and JANS).

\* 1.2 Package outlines. The device package outlines are as follows: TO-18 (no suffix) in accordance with [figure 1](#) and surface mount (UB suffix) in accordance with [figure 2](#) for all encapsulated device types.

1.3 Maximum ratings.  $T_A = +25^\circ\text{C}$ , unless otherwise specified. (1)

P <sub>T</sub> (2) T <sub>A</sub> = +25°C	P <sub>T</sub> (3) T <sub>C</sub> = +25°C	V <sub>DS</sub> , V <sub>DG</sub>		V <sub>GS</sub>		I <sub>G</sub>	R <sub>θJA</sub>	R <sub>θJC</sub>	T <sub>J</sub> and T <sub>STG</sub>
		2N4856 2N4857 2N4858	2N4859 2N4860 2N4861	2N4856 2N4857 2N4858	2N4859 2N4860 2N4861				
<u>W</u> 0.36  0.40, all UB (4)	<u>W</u> 1.8	<u>V dc</u> 40	<u>V dc</u> 30	<u>V dc</u> -40	<u>V dc</u> -30	<u>mA dc</u> 50	<u>°C/W</u> 486  325	<u>°C/mW</u> 0.097	<u>°C</u> -65 to +200

- (1) These characteristics applicable to all package styles, unless otherwise noted.
- (2) Derate linearly 2.06 mW/°C for  $T_A > +25^\circ\text{C}$ .
- (3) Derate linearly 10.3 mW/°C for  $T_C > +25^\circ\text{C}$ .
- (4) Derate linearly 3.08 mW/°C above  $T_C = +70^\circ\text{C}$ .

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



1.4 Primary electrical characteristics.  $T_A = +25^\circ\text{C}$ , unless otherwise specified. (1)

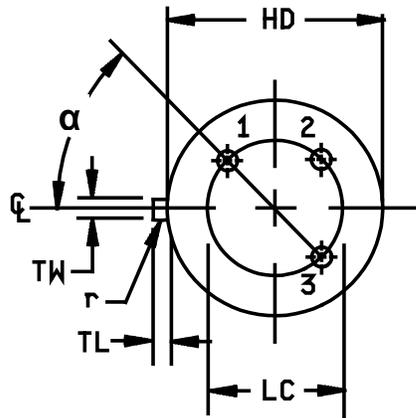
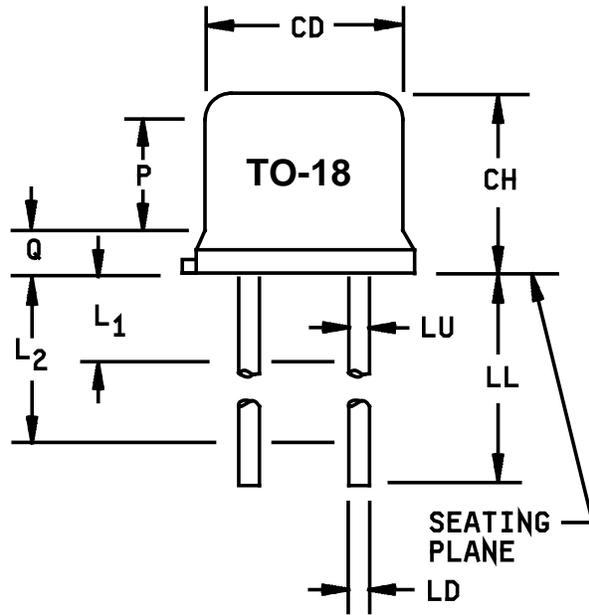
	$I_{DSS}$ (2) $V_{DS} = 15\text{ V dc}$ $V_{GS} = 0$			$V_{DS(on)}$			$V_{GS(off)}$ $V_{DS} = 15\text{ V dc}$ $I_D = 0.5\text{ nA dc}$		
				$V_{GS} = 0$ $I_D = 20\text{ mA dc}$	$V_{GS} = 0$ $I_D = 10\text{ mA dc}$	$V_{GS} = 0$ $I_D = 5\text{ mA dc}$			
	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861
	<u>mA dc</u>	<u>mA dc</u>	<u>mA dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>
Min	50	20	8				-4	-2	-0.8
Max	175	100	80	0.75	0.50	0.50	-10	-6	-4

	$r_{ds(on)}$		
	$V_{GS} = 0; I_D = 1.0\text{ mA dc}$ $I_d = 100\text{ }\mu\text{A ac(rms), } f = 1\text{ kHz}$		
	2N4856 2N4859	2N4857 2N4860	2N4858 2N4861
	<u><math>\Omega</math></u>	<u><math>\Omega</math></u>	<u><math>\Omega</math></u>
Min			
Max	25	40	60

- (1) These characteristics applicable to all package styles.
- (2) Pulsed (see 4.5.1).

- \* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.
- \* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV" and "JANS".
- \* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
- \* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
- \* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "4856", "4857", "4858", "4859", "4860", and "4861".
- \* 1.5.2.3 Suffix letters. No suffix is used on devices that are packaged in the TO-18 package of figure 1. The suffix letters "UB" are used on devices that are packaged in the surface mount package of figure 2.
- \* 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on QPDISIS-19500.

Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	5
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	4, 5
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L <sub>1</sub>		.050		1.27	7,8
L <sub>2</sub>	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	
r		.010		0.25	3, 10
$\alpha$	45° TP		45° TP		6

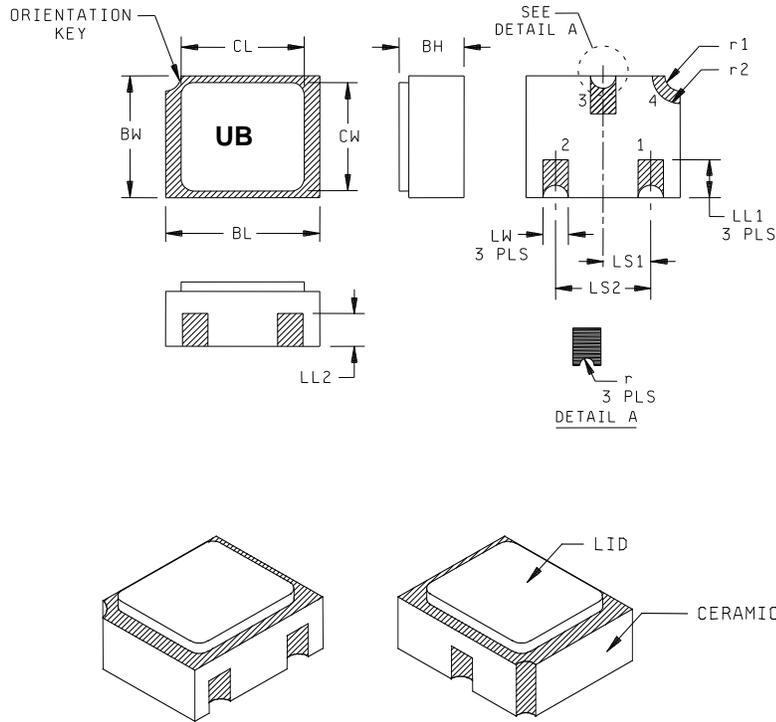


NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TL shall be held for a minimum length of .011 (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
8. All three leads.
9. The gate shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.
12. Lead 1 = source, lead 2 = drain, lead 3 = gate.

FIGURE 1. Physical dimensions TO-18.

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Ltr.	Dimensions				Note	Ltr.	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.040	0.89	1.02	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL		.128		3.25		r		.008		0.20	
CW		.108		2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.96		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas.
4. Lid material: Kovar.
5. Pad 1 = Drain, Pad 2 = Source, Pad 3 = Gate, Pad 4 = Shielding connected to the lid.
6. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.

\*

FIGURE 2. Physical dimensions for surface mount.

## 2. APPLICABLE DOCUMENTS

- \* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

- \* (Copies of these documents are available online at <http://quicksearch.dla.mil/>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and on figures 1 and 2.

3.4.1 Lead finish. Unless otherwise specified, lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. Metal oxide semiconductor (MOS) devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate must be terminated to source,  $R \leq$  or 100 k $\Omega$ , whenever bias voltage is applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500 except for the UB suffix package. Marking on the UB package shall consist of an abbreviated part number, the date code, and the manufacturer's symbol or logo. The prefixes JAN, JANTX, JANTXV, and JANS can be abbreviated as J, JX, JV, and JS respectively.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4 VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and tables I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table III tests, the tests specified in table III herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement	
	JANS level	JANTX and JANTXV levels
9	Not applicable	Not applicable
10	Not applicable	Not applicable
11	$I_{D(off)1}$ , $r_{ds(on)}$ , $I_{GSS1}$ , and $I_{DSS}$	$I_{D(off)1}$ , $r_{ds(on)}$ , $I_{GSS1}$ , and $I_{DSS}$
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; $\Delta I_{DSS} = \pm 15$ percent; $\Delta r_{ds(on)} = \pm 20$ percent; $\Delta I_{D(off)1} = 0.1$ nA or $\pm 100$ percent of initial value. $\Delta I_{GSS1} = \pm 0.1$ nA or $\pm 100$ percent of initial value, whichever is greater.	Subgroup 2 of table I herein; $\Delta I_{DSS} = \pm 15$ percent; $\Delta r_{ds(on)} = \pm 20$ percent; $\Delta I_{D(off)1} = 0.1$ nA or $\pm 100$ percent of initial value. $\Delta I_{GSS1} = \pm 0.1$ nA or $\pm 100$ percent of initial value, whichever is greater.

4.3.1 Power burn-in. Power burn-in conditions are in accordance with method 1039 of MIL-STD-750, test condition A and as follows:  $T_A \geq +150^\circ\text{C}$ ;  $V_{GS} = 80$  percent of rated,  $V_{DS} = 0$ . NOTE: No heatsink or forced air cooling on the devices shall be permitted.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500, and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in tables VIA (JANS) and VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 and as follows. Delta measurements shall be in accordance with table II herein.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

Subgroup	Method	Condition
B4	1037	$P_T = 360$ mW at $T_A = +30^\circ\text{C}$ , $\pm 5^\circ\text{C}$ ; 2,000 cycles.
B5	1027	96 hours; $V_{DS} = 15$ V dc; $I_D = 24$ mA at $T_A = +100^\circ\text{C}$ ; or adjust as required by the chosen $T_A$ to give an average lot $T_J = +275^\circ\text{C}$ .

4.4.2.2 Group B inspection, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1027	$V_{GS} = -32$ V dc for 2N4856, 2N4857, 2N4858, at $T_A = +175^\circ\text{C} \pm 5^\circ\text{C}$ ; $V_{DS} = 0$ V. $V_{GS} = -24$ V dc for 2N4859, 2N4860, 2N4861, at $T_A = +175^\circ\text{C} \pm 5^\circ\text{C}$ ; $V_{DS} = 0$ V.

- \* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and as follows. Delta measurements shall be in accordance with [table II](#) herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E, (not applicable to UB suffix device).
C6	1026	$V_{GS} = -32$ V dc for 2N4856, 2N4857, 2N4858, at $T_A = +175^\circ\text{C} \pm 5^\circ\text{C}$ ; $V_{DS} = 0$ V. $V_{GS} = -24$ V dc for 2N4859, 2N4860, 2N4861, at $T_A = +175^\circ\text{C} \pm 5^\circ\text{C}$ ; $V_{DS} = 0$ V.

- \* 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table III](#) herein. Delta measurements shall be in accordance with [table II](#) herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

TABLE I. Group A inspection

Inspection <u>1/ 2/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Gate to source breakdown voltage 2N4856, 2N4857, 2N4858 2N4859, 2N4860, 2N4861	3401	Bias condition C; $I_G = -1.0 \mu\text{A dc}$ ; $V_{DS} = 0$	$V_{(BR)GSS}$	-40 -30		V dc V dc
Gate reverse current 2N4856, 2N4857, 2N4858 2N4859, 2N4860, 2N4861	3411	Bias condition C; $V_{DS} = 0$ $V_{GS} = -20 \text{ V dc}$ $V_{GS} = -15 \text{ V dc}$	$I_{GSS1}$		-0.25 -0.25	nA dc nA dc
Drain current cutoff	3413	Bias condition A, $V_{DS} = 15 \text{ V dc}$ , $V_{GS} = -10 \text{ V dc}$	$I_{D(off)1}$		0.25	nA dc
Drain current zero-gate voltage 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3413	Bias condition C, $V_{DS} = 15 \text{ V dc}$ , $V_{GS} = 0$ , pulsed (see 4.5.1)	$I_{DSS}$	50 20 8	175 100 80	mA dc mA dc mA dc
Drain to source on-state voltage 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3405	Bias condition B, $V_{GS} = 0$ $I_D = 20 \text{ mA dc}$ $I_D = 10 \text{ mA dc}$ $I_D = 5 \text{ mA dc}$	$V_{DS(on)}$		0.75 0.50 0.50	V dc V dc V dc
Gate to source off-state voltage 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3403	$V_{DS} = 15 \text{ V dc}$ , $I_D = 0.5 \text{ nA dc}$	$V_{GS(off)}$	-4 -2 -0.8	-10 -6 -4	V dc V dc V dc
Static drain to source on-state resistance 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3421	$V_{GS} = 0$ ; $I_D = 1.0 \text{ mA dc}$ ;	$r_{ds(on)}$		25 40 60	$\Omega$ $\Omega$ $\Omega$

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u> <u>2/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u>						
High temperature operation:						
Gate reverse current 2N4856, 2N4857, 2N4858 2N4859, 2N4860, 2N4861	3411	Bias condition C; $V_{DS} = 0$ V $V_{GS} = -20$ V dc $V_{GS} = -15$ V dc	$I_{GSS2}$		-0.5	$\mu$ A dc
					-0.5	$\mu$ A dc
Drain current	3413	Bias condition A, $V_{DS} = 15$ V dc; $V_{GS} = -10$ V dc	$I_{D(off)2}$		0.5	$\mu$ A dc
<u>Subgroup 4</u>						
Small-signal common-source short-circuit input capacitance	3431	$V_{DS} = 0$ , $V_{GS} = -10$ V; $f = 1$ MHz; $C_1 = .1$ $\mu$ F, $C_2 = 20.1$ $\mu$ F $L_1 = L_2 = \geq 500$ $\mu$ H	$C_{iss}$		18	pF
Small-signal common-source short-circuit reverse transfer capacitance	3433	$V_{DS} = 0$ , $V_{GS} = -10$ V; $f = 1$ MHz; $C_1 = .1$ $\mu$ F, $L_1 = L_2 = \geq 500$ $\mu$ H	$C_{riss}$		8	pF
Turn-on delay time 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3459	See <a href="#">figure 3</a>	$t_{d(on)}$		6	ns
					6	ns
					10	ns
Rise time 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3459	See <a href="#">figure 3</a>	$t_r$		3	ns
					4	ns
					10	ns
Turn-off delay time 2N4856, 2N4859 2N4857, 2N4860 2N4858, 2N4861	3459	See <a href="#">figure 3</a>	$t_{d(off)}$		25	ns
					50	ns
					100	ns
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan, see [MIL-PRF-19500](#).2/ These characteristics applicable to all package styles, unless otherwise noted.

TABLE II. Groups B, C, and E delta measurements 1/ 2/ 3/ 4/

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1.	Static drain to source on-state resistance	3421	$V_{GS} = 0$ ; $I_{DS} = 1.0$ mA dc;	$\Delta r_{DS(on)}$	$\pm 25$ percent change from previously measured value.	
2.	Drain current	3413	Bias condition C; $V_{DS} = 15$ V dc, $V_{GS} = 0$ ; pulsed (see 4.5.1)	$\Delta I_{DSS1}$	$\pm 15$ percent change from previously measured value.	

1/ Devices which exceed the group A limits for this test shall be rejected.

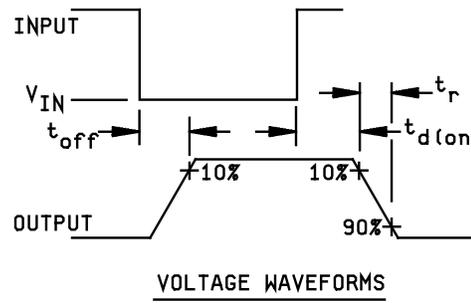
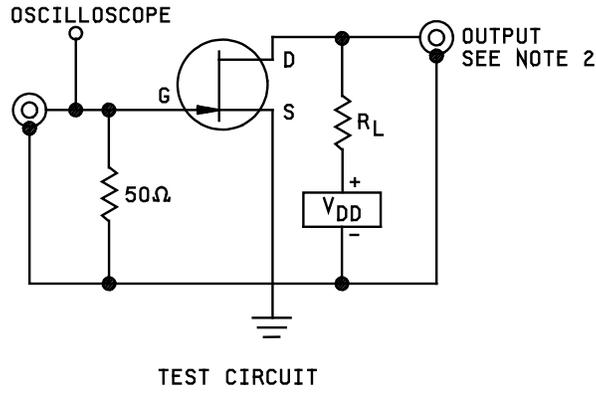
2/ The delta measurements for table E-VIA (JANS) of MIL-PRF-19500 are as follows: Subgroup 5, see table II herein, steps 1 and 2.

3/ The delta measurements for table E-VII of MIL-PRF-19500 are as follows: Subgroup 6, table II herein, steps 1 and 2 (for JANS only).

4/ The delta measurements for table E-IX of MIL-PRF-19500 are as follows: Subgroups 1 and 2, table II herein, steps 1 and 2.

\* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	500 cycles.	
* Hermetic seal	1071		
Fine leak			
Gross leak			
End-point electrical measurements		See <a href="#">table I</a> , subgroup 2 and <a href="#">table II</a> herein.	
<u>Subgroup 2</u>			45 devices c = 0
Blocking life	1048	Test temperature = +125°C, $V_{GS}$ or $V_{DG}$ = 80 percent of rated, T = 1,000 hours.	
End-point electrical measurements		See <a href="#">table I</a> , subgroup 2 and <a href="#">table II</a> herein	
<u>Subgroup 4 and 5</u>			
Not applicable			



TEST CONDITIONS AND COMPONENT VALUE						
Type	V <sub>DD</sub>	V <sub>GS(on)</sub>	V <sub>GS(off)</sub>	R <sub>L</sub>	V <sub>IN</sub>	I <sub>D(on)</sub> (1)
	V dc	V dc	V dc	Ω	V dc	mA dc
2N4856, 2N4859	10	0	-10	464	-10	20
2N4857, 2N4860	10	0	-6	953	-6	10
2N4858, 2N4861	10	0	-4	1,910	-4	5

(1) Nominal value; exact value varies slightly with transistor parameters.

NOTES:

1. The input waveform has the following characteristics:  $t_p = 200$  ns;  $t_r \leq 1$  ns; duty cycle  $\approx 2$  percent. It is supplied by a generator with  $Z_{out} = 50$  Ω.
2. Waveforms are monitored on an oscilloscope with the following characteristics:  $t_r \leq 0.75$  ns;  $R_{IN} \geq 1$  MΩ;  $C_{IN} \leq 2.5$  pF.
3. These characteristics applicable to all package styles, unless otherwise noted.

FIGURE 3. Switching time test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

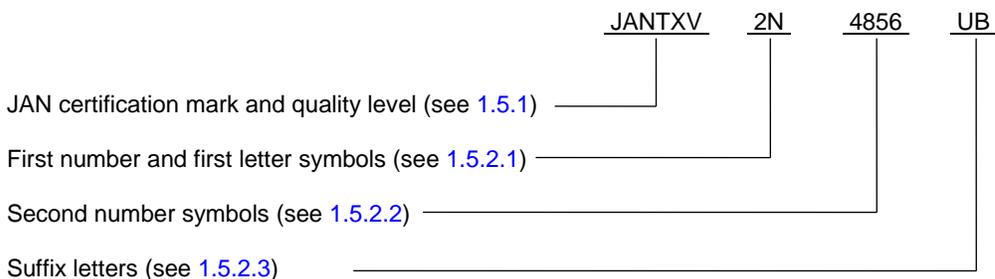
6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- \* d. The complete Part or Identifying Number (PIN), see 1.5 and 6.5.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 PIN construction example.

\* 6.4.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



\* 6.5 List of PINs.

- \* 6.5.1
- List of PINs for encapsulated devices.
- The following is a list of possible PINs for encapsulated devices available on this specification sheet.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N4856	JANTX2N4856	JANTXV2N4856	JANS2N4856
JAN2N4856UB	JANTX2N4856UB	JANTXV2N4856UB	JANS2N4856UB
JAN2N4857	JANTX2N4857	JANTXV2N4857	JANS2N4857
JAN2N4857UB	JANTX2N4857UB	JANTXV2N4857UB	JANS2N4857UB
JAN2N4858	JANTX2N4858	JANTXV2N4858	JANS2N4858
JAN2N4858UB	JANTX2N4858UB	JANTXV2N4858UB	JANS2N4858UB
JAN2N4859	JANTX2N4859	JANTXV2N4859	JANS2N4859
JAN2N4859UB	JANTX2N4859UB	JANTXV2N4859UB	JANS2N4859UB
JAN2N4860	JANTX2N4860	JANTXV2N4860	JANS2N4860
JAN2N4860UB	JANTX2N4860UB	JANTXV2N4860UB	JANS2N4860UB
JAN2N4861	JANTX2N4861	JANTXV2N4861	JANS2N4861
JAN2N4861UB	JANTX2N4861UB	JANTXV2N4861UB	JANS2N4861UB

- \* 6.6
- Changes from previous issue.
- The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:  
 Army - CR  
 Navy - EC  
 Air Force - 85  
 DLA - CC

Preparing activity:  
 DLA - CC  
 (Project 5961-2015-047)

Review activities:  
 Army - MI  
 Air Force - 71, 99

- \* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at
- <https://assist.dla.mil>
- .