

The documentation and process conversion measures necessary to comply with this document shall be completed by 19 September 2015.

INCH-POUND

MIL-PRF-19500/379K
19 June 2015
SUPERSEDING
MIL-PRF-19500/379J
2 July 2012

PERFORMANCE SPECIFICATION SHEET

TRANSISTOR, PNP, SILICON, HIGH-POWER,
ENCAPSULATED (THROUGH HOLE), DEVICE TYPES 2N3791 AND 2N3792, QUALITY LEVELS: JAN, JANTX,
JANTXV, AND JANS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

1.1 Scope. This specification covers the performance requirements for power PNP silicon 2N3791 and 2N3792 transistors. Four levels of product assurance are provided for each encapsulated device type as specified in [MIL-PRF-19500](#).

1.2 Package outline. See [figure 1](#), (similar to TO-3).

1.3 Maximum ratings. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

	P_T (1) $T_A = +25^\circ\text{C}$	P_T (2) $T_C = +100^\circ\text{C}$	V_{CB0}	V_{CEO}	V_{EBO}	I_B	I_C	T_J and T_{STG}	$R_{\theta JC}$
	<u>W</u>	<u>W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>°C</u>	<u>°C/W</u>
2N3791	5.0	85.7	-60	-60	-7.0	-4.0	-10	-65 to +200	1.1
2N3792	5.0	85.7	-80	-80	-7.0	-4.0	-10	-65 to +200	1.1

(1) Derate linearly 28.57 mW/°C above $T_A = +25^\circ\text{C}$.

(2) See [figure 2](#) for temperature-power derating curves.

1.4 Primary electrical characteristics. Unless otherwise specified, $T_C = +25^\circ\text{C}$.

	h_{FE2} (1)	h_{FE4} (1)	$V_{BE(SAT)1}$ (1)	$V_{CE(SAT)1}$ (1)	C_{obo}	$ h_{fe} $
	$V_{CE} = -2.0$ V dc $I_C = -3.0$ A dc	$V_{CE} = -4.0$ V dc $I_C = -10$ A dc	$I_C = -5.0$ A dc $I_B = -0.5$ A dc	$I_C = -5.0$ A dc $I_B = -0.5$ A dc	$V_{CB} = -10$ V dc $I_E = 0$ $f = 1$ MHz	$V_{CE} = -10$ V dc $I_C = -0.5$ A dc $f = 1$ MHz
Min	30	5.0	<u>V dc</u>	<u>V dc</u>	<u>pF</u>	4.0
Max	120		-1.5	-1.0	500	20

(1) Pulse (see [4.5.1](#)).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil/>.



- * 1.5 Part or Identifying Number (PIN). The PIN is in accordance with [MIL-PRF-19500](#), and as specified herein. See 6.5 for PIN construction example and 6.6 for a list of available PINs.
- * 1.5.1 JAN brand and quality level designators.
- * 1.5.1.1 Encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: the base quality level "JAN" that uses no modifiers, "JANTX", "JANTXV", and "JANS".
- * 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.
- * 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".
- * 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "3791" and "3792".
- * 1.5.3 Lead finish. The lead finishes applicable to this specification sheet are listed on [QML-19500](#).

2. APPLICABLE DOCUMENTS

- * 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

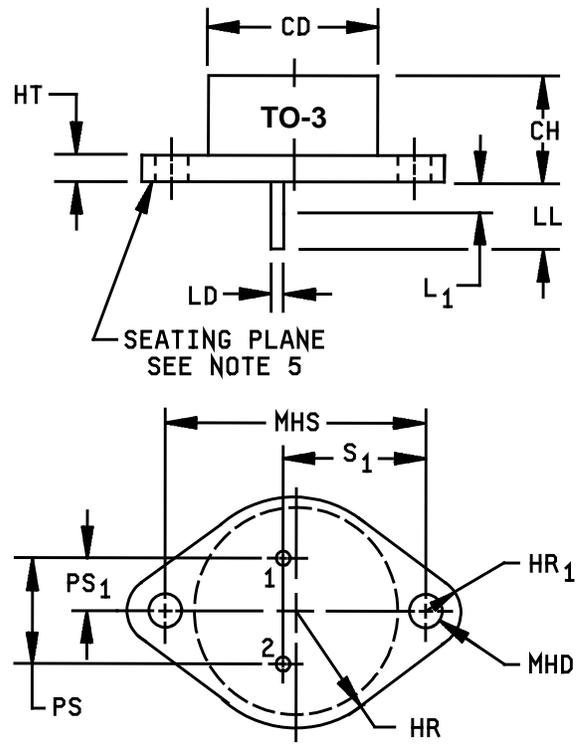
DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

*(Copies of these documents are available online at <http://quicksearch.dla.mil>)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD		.875		22.22	
CH	.270	.350	6.86	8.89	
HR	.495	.525	12.57	13.34	
HR ₁	.131	.188	3.33	4.78	
HT	.060	.135	1.52	3.43	
LD	.038	.043	0.97	1.09	7
LL	.312	.500	7.92	12.70	
L ₁		.050		1.27	7
MHD	.151	.165	3.84	4.19	
MHS	1.177	1.197	29.90	30.40	
PS	.420	.440	10.67	11.18	4,5
PS ₁	.205	.225	5.21	5.72	4,5
s ₁	.655	.675	16.64	17.15	4



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Terminal 2, base; terminal 1, emitter; case, collector.
4. These dimensions should be measured at points .050 inch (1.27 mm) to .055 inch (1.40 mm) below seating plane. When gauge is not used, measurement will be made at the seating plane.
5. The seating plane of the header shall be flat within .001 inch (0.03 mm) concave to .004 inch (0.10 mm) convex inside a .930 inch (23.62 mm) diameter circle on the center of the header and flat within .001 inch (0.03 mm) concave to .006 inch (0.15 mm) convex overall.
6. Collector shall be electrically connected to the case.
7. LD applies between L₁ and LL. Lead diameter shall not exceed twice LD within L₁.
8. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 1. Physical dimensions (similar to TO-3).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are authorized by the qualifying activity for listing on the applicable qualified products list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#).

* 3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in [MIL-PRF-19500](#) and herein. The device package style shall be as follows: TO-3, in accordance with [figure 1](#).

* 3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#) herein.

3.6 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.7 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [tables I and II](#)).

* 4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening.

* 4.3.1 Screening of encapsulated devices (quality levels JANTX, JANTXV, and JANS only). Screening of encapsulated devices shall be in accordance with table E-IV of [MIL-PRF-19500](#) and as specified herein. The following measurements shall be made in accordance with [table I](#) herein. Devices that exceed the limits of [table I](#) herein shall not be acceptable.

Screen	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750 . (see 4.3.1.2)	Thermal impedance, method 3131 of MIL-STD-750 . (see 4.3.1.2)
9	I _{CES1} and h _{FE2}	I _{CES1}
11	I _{CES1} and h _{FE2} ΔI _{CES1} = 100 percent of initial value or 5 μA dc, whichever is greater. Δh _{FE2} = ±15 percent of initial value.	I _{CES1} and h _{FE2} ; ΔI _{CES1} = 100 percent of initial value or 10 μA dc, whichever is greater.
12	See 4.3.1	See 4.3.1
13	ΔI _{CES1} = 100 percent of initial value or 1 μA dc, whichever is greater; Δh _{FE2} = ±15 percent of initial value; subgroups 2 and 3 of table I herein.	ΔI _{CES1} = 100 percent of initial value or 5 μA dc, whichever is greater; Δh _{FE2} = ±15 percent of initial value; subgroup 2 of table I herein.

(1) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1.1 Power burn-in conditions. Power burn-in conditions are as follows: T_J = +187.5°C ±12.5°C; V_{CB} = -35 ±5 V dc; T_A = room ambient as defined in the general requirements of [MIL-STD-750](#).

4.3.1.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of [MIL-STD-750](#) using the guidelines in that method for determining I_M, I_H, t_H, t_{MD} (and V_C where appropriate). The thermal impedance limit used in screen 3c of [4.3](#) herein and [table I](#) shall comply with the thermal impedance graph in [figure 3](#) (less than or equal to the curve value at the same t_H time) and shall be less than the process determined statistical maximum limit as outlined in method 3131.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#).

* 4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#) and [table I](#) herein.

* 4.4.2 Group B inspection.

* 4.4.2.1 Quality level JANS, table E-VIA of [MIL-PRF-19500](#).

Subgroup	Method	Conditions
* B3	2037	Test condition D; all internal wires for each device shall be pulled separately.
B4	1037	V _{CB} = -30 V dc; P _T = 5 W at T _A = +25°C ±3°C, t _{on} = t _{off} = 3 minutes minimum. No heat sink nor forced air on the device shall be permitted.
B5	1027	V _{CB} = -30 V dc; T _A = +125°C ±25°C for 96 hours; P _T = adjusted as required by the chosen T _A to give an average lot T _J = +275°C.
B6	3131	See 4.5.2 .

- * 4.4.2.2 Quality level JAN, JANTX and JANTXV, table E-VIb of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
B3	1027	$T_J = +187.5^\circ\text{C} \pm 12.5^\circ\text{C}$; $V_{CB} = -35 \text{ V dc} \pm 5 \text{ V dc}$; $T_A \leq +100^\circ\text{C}$.
B5	3131	See 4.5.2.
B6	1032	$T_A = +200^\circ\text{C}$.

- * 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows. Delta requirements shall be in accordance with the applicable steps of table II herein.

<u>Subgroup</u>	<u>Method</u>	<u>Conditions</u>
C2	2036	Test condition A; weight = 10 pounds, $t = 15 \text{ s}$.
C6	1026	$T_J = +187.5^\circ\text{C} \pm 12.5^\circ\text{C}$; $V_{CB} = -35 \text{ V dc}$; $T_A \leq +100^\circ\text{C}$.

- * 4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table III herein. Delta requirements shall be in accordance with the applicable steps of table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in MIL-STD-750.

4.5.2 Thermal resistance. Thermal resistance measurements shall be conducted in accordance with test method 3131 of MIL-STD-750. The following details shall apply:

- a. Collector current magnitude during power application shall be -1.0 A dc minimum.
- b. Collector to emitter voltage magnitude shall be -10 V dc minimum.
- c. Reference temperature measuring point shall be the case.
- d. Reference point temperature shall be $+25^\circ\text{C} \leq T_R \leq +75^\circ\text{C}$ and recorded before the test is started.
- e. Mounting arrangement shall be with heat sink to header.
- f. Maximum limit of $R_{\theta JC} = 1.1$.

TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical examination	2071					
<u>Subgroup 2</u>						
Thermal impedance <u>2/</u>	3131	See 4.3.1.2	$Z_{\theta JX}$			$^{\circ}\text{C/W}$
Collector-emitter breakdown voltage 2N3791 2N3792	3011	Bias conditions D, $I_C = -10$ mA dc; pulsed (see 4.5.1)	$V_{(BR)CEO}$	-60 -80		V dc V dc
Emitter-base cutoff current	3061	Bias condition D; $V_{EB} = -7$ V dc	I_{EBO}		-5.0	mA dc
Collector-base cutoff current 2N3791 2N3792	3036	Bias conditions D $V_{CB} = -60$ V dc $V_{CB} = -80$ V dc	I_{CBO}		-20 -20	μA dc μA dc
Collector-emitter cutoff current 2N3791 2N3792	3041	Bias condition A; $V_{BE} = -1.5$ V dc $V_{CE} = -60$ V dc $V_{CE} = -80$ V dc	I_{CEX}		-20 -20	μA dc μA dc
Collector-emitter cutoff current 2N3791 2N3792	3041	Bias condition C $V_{CE} = -50$ V dc $V_{CE} = -70$ V dc	I_{CES1}		-20 -20	μA dc μA dc
Base-emitter saturated voltage	3066	Test condition A; $I_C = -5$ A dc; $I_B = -0.5$ A dc; pulsed (see 4.5.1)	$V_{BE(sat)1}$		-1.5	V dc
Base-emitter saturated voltage	3066	Test condition A; $I_C = -10$ A dc; $I_B = -2$ A dc; pulsed (see 4.5.1)	$V_{BE(sat)2}$		-3.0	V dc
Collector-emitter saturated voltage	3071	$I_C = -5$ A dc; $I_B = -0.5$ A dc; pulsed (see 4.5.1)	$V_{CE(sat)1}$		-1.0	V dc
Collector-emitter saturated voltage	3071	$I_C = -10$ A dc; $I_B = -2$ A dc; pulsed (see 4.5.1)	$V_{CE(sat)2}$		-2.5	V dc
Forward-current transfer ratio	3076	$V_{CE} = -2.0$ V dc; $I_C = -1.0$ A dc; pulsed (see 4.5.1)	h_{FE1}	50	150	

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Forward-current transfer ratio	3076	$V_{CE} = -2.0$ V dc; $I_C = -3.0$ A dc; pulsed (see 4.5.1)	h_{FE2}	30	120	
Forward-current transfer ratio	3076	$V_{CE} = -2.0$ V dc; $I_C = -5$ A dc; pulsed (see 4.5.1)	h_{FE3}	10		
Forward-current transfer ratio	3076	$V_{CE} = -4.0$ V dc; $I_C = -10$ A dc; pulsed (see 4.5.1)	h_{FE4}	5		
<u>Subgroup 3</u>						
High temperature operation:		$T_A = +150^\circ\text{C}$				
Collector to emitter cutoff current 2N3791 2N3792	3041	Bias conditions C $V_{CE} = -50$ V dc $V_{CE} = -70$ V dc	I_{CES2}		-3.4 -3.4	mA dc mA dc
Low temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = -2.0$ V dc; $I_C = -3.0$ A dc; pulsed (see 4.5.1)	h_{FE5}	12		
<u>Subgroup 4</u>						
Switching parameters:		See figure 4				
Pulse delay time			t_d		0.2	μs
Pulse rise time			t_r		1.3	μs
Pulse storage time			t_s		1.4	μs
Pulse fall time			t_f		1.0	μs
Small-signal short-circuit forward-current transfer	3206	$V_{CE} = -10$ V dc; $I_C = -0.5$ A dc; $f = 1$ kHz	h_{fe}	30	300	
Magnitude of small-signal short-circuit, forward-current transfer ratio	3306	$V_{CE} = -10$ V dc; $I_C = -0.5$ A dc; $f = 1$ MHz	$ h_{fe} $	4.0	20	
Open circuit output capacitance	3236	$V_{CB} = -10$ V dc; $I_E = 0$; $f = 1$ MHz	C_{obo}		500	pF

See footnote at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area (continuous dc)	3051	$T_C = +25^\circ\text{C}$; $t \geq 1$ s; 1 cycle; (see figure 5)				
<u>Test 1</u>		$V_{CE} = -15$ V dc; $I_C = -10$ A dc				
<u>Test 2</u>		$V_{CE} = -40$ V dc; $I_C = -3.75$ A dc				
<u>Test 3</u>						
2N3791		$V_{CE} = -55$ V dc; $I_C = -0.9$ A dc				
2N3792		$V_{CE} = -65$ V dc; $I_C = -0.9$ A dc				
Safe operating area (clamped inductive)	3053	Condition C $T_A = +25^\circ\text{C}$; $I_C = -10$ A dc; $V_{CC} = -15$ V dc; (see figure 6 and 7)				
2N3791		Clamp voltage = -60 V dc				
2N3792		Clamp voltage = -80 V dc				
<u>Subgroups 6 and 7</u>						
Not applicable						

1/ For sampling plan, see [MIL-PRF-19500](#).

2/ This test required for the following end-point measurements only:
 Group B, subgroups 2 and 3 (JAN, JANTX, and JANTXV).
 Group B, subgroups 3, 4, and 5 (JANS).
 Group C, subgroup 2 and 6.
 Group E, subgroup 1.

TABLE II. Groups B, C, and E delta measurements. 1/ 2/ 3/ 4/

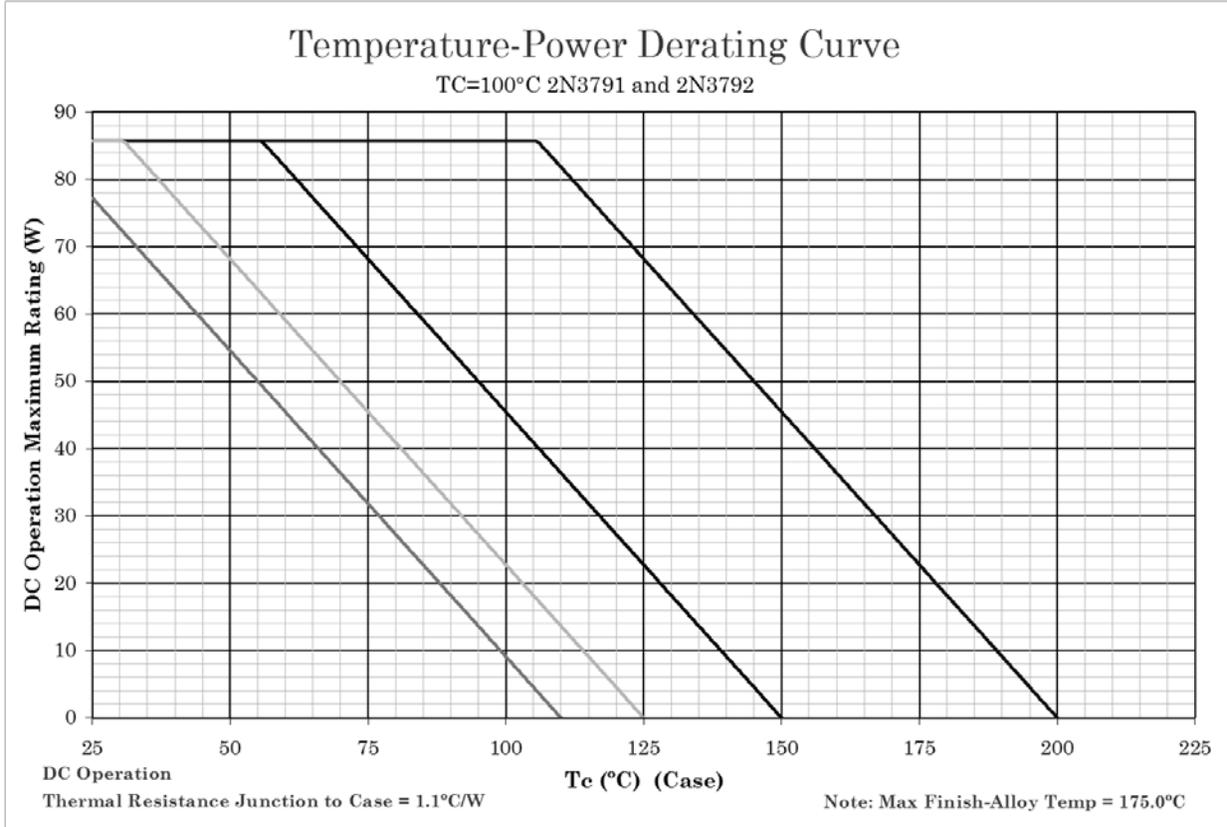
Step	Inspection	MIL-STD-750		Symbol	Limits		Unit
		Method	Conditions		Min	Max	
1.	Collector-emitter cutoff current 2N3791 2N3792	3041	Bias condition C $V_{CE} = -50$ V dc $V_{CE} = -70$ V dc	ΔI_{CES1} 5/	100 percent of initial value or 1 μ A dc; whichever is greater.		
2.	Forward-current transfer ratio	3076	$V_{CE} = -2.0$ V dc; $I_C = -3.0$ A dc; pulsed (see 4.5.1)	Δh_{FE2} 5/	± 25 percent change from initial value		
3.	Collector-emitter (voltage saturated)	3071	$I_C = -5$ A dc; $I_B = -0.5$ A dc; pulsed (see 4.5.1)	$\Delta V_{CE(sat)1}$ 5/	± 50 mV dc change from previously measured value		

- 1/ The delta measurements for appendix E, table E-VIA (JANS) of MIL-PRF-19500 are as follows:
a. Subgroup 4, see table II herein, step 3.
b. Subgroup 5, see table II herein, steps 1, 2, and 3.
- 2/ The delta measurements for appendix E, table E-VIB (JAN, JANTX, and JANTXV) of MIL-PRF-19500 are as follows:
a. Subgroup 3, see table II herein, steps 1, 2, and 3.
b. Subgroup 6, see table II herein, steps 1 and 2.
- 3/ The delta measurements for appendix E, table E-VII of MIL-PRF-19500 are subgroup 6, see table II herein, steps 1, 2, and 3 (JANS); 1 and 2 (JAN, JANTX, and JANTXV).
- 4/ The delta measurements for appendix E; table E-IX of MIL-PRF-19500 are subgroups 1 and 2, see table II herein, all steps.
- 5/ Devices which exceed the group A limits for this test shall not be shippable but are not considered failures for the test.

MIL-PRF-19500/379K

TABLE III. Group E inspection (all quality levels) - for qualification and re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			
Temperature cycle	1051	Condition G, 500 cycles.	45 devices c = 0
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I , subgroup 2 and table II , all steps.	
<u>Subgroup 2</u>			
Blocking life	1048	+125°C; V _{CB} = 80 percent rated (see 1.3); 1,000 hours.	45 devices c = 0
Electrical measurements		See table I , subgroup 2 and table II , all steps.	
<u>Subgroup 4</u>			
Thermal impedance curves		See MIL-PRF-19500 .	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 8</u>			
Reverse stability	1033	Condition A.	45 devices c = 0

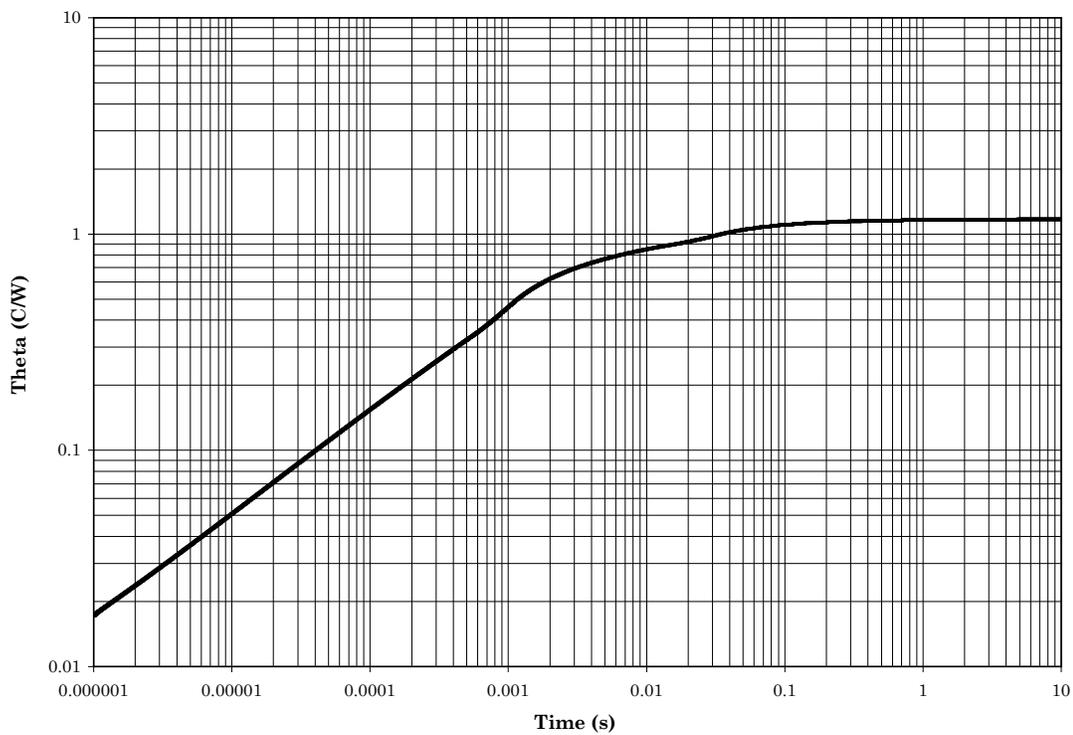


NOTES:

1. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power/current for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq +200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq +150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq +125^\circ\text{C}$, and $+110^\circ\text{C}$ to show power rating where most users want to limit T_J in their application.

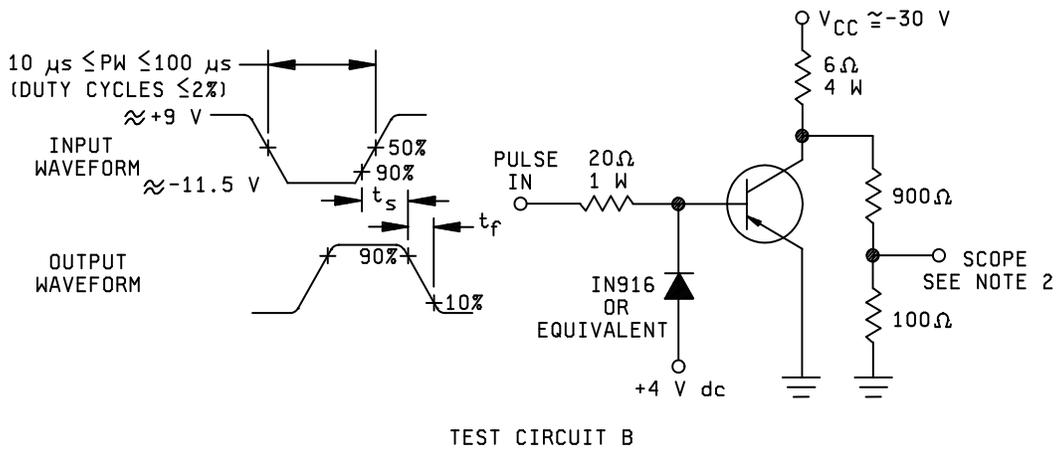
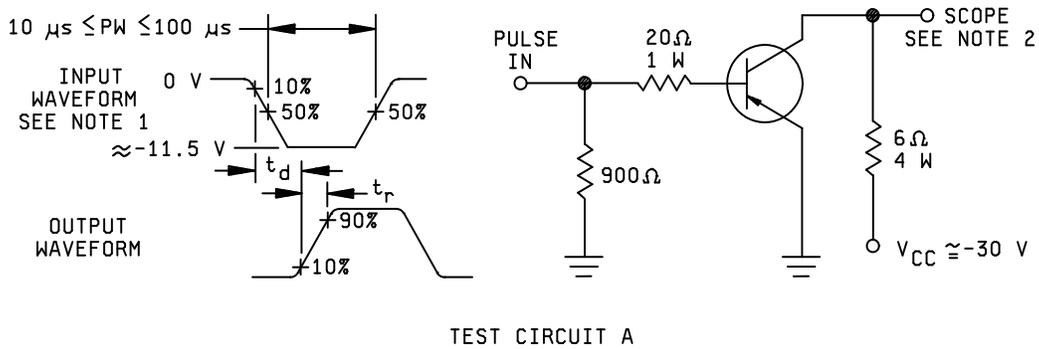
FIGURE 2. Temperature-power derating graphs, TO-3.

Maximum Thermal Impedance



$T_C = +25^{\circ}\text{C}$. $R_{\theta\text{JC}} = 1.1^{\circ}\text{C/W}$.

FIGURE 3. Transient thermal impedance graph.



NOTES:

1. The input waveform is supplied by a pulse generator with the following characteristics:
 $t_r \leq 2.0 \text{ ns}$, $t_f \leq 1 \text{ } \mu\text{s}$, $10 \text{ } \mu\text{s} \leq \text{PW} \leq 100 \text{ } \mu\text{s}$, $Z_{\text{OUT}} = 50 \Omega$, duty cycle ≤ 2 percent.
2. Output waveforms are monitored on an oscilloscope with the following characteristics:
 $t_r \leq 5 \text{ ns}$, $Z_{\text{in}} \geq 100 \text{ kW}$, $C_{\text{in}} \leq 12 \text{ pF}$.
3. Test circuit A for t_d and t_r ; test circuit B for t_s and t_f .

FIGURE 4. Pulse response test circuits.

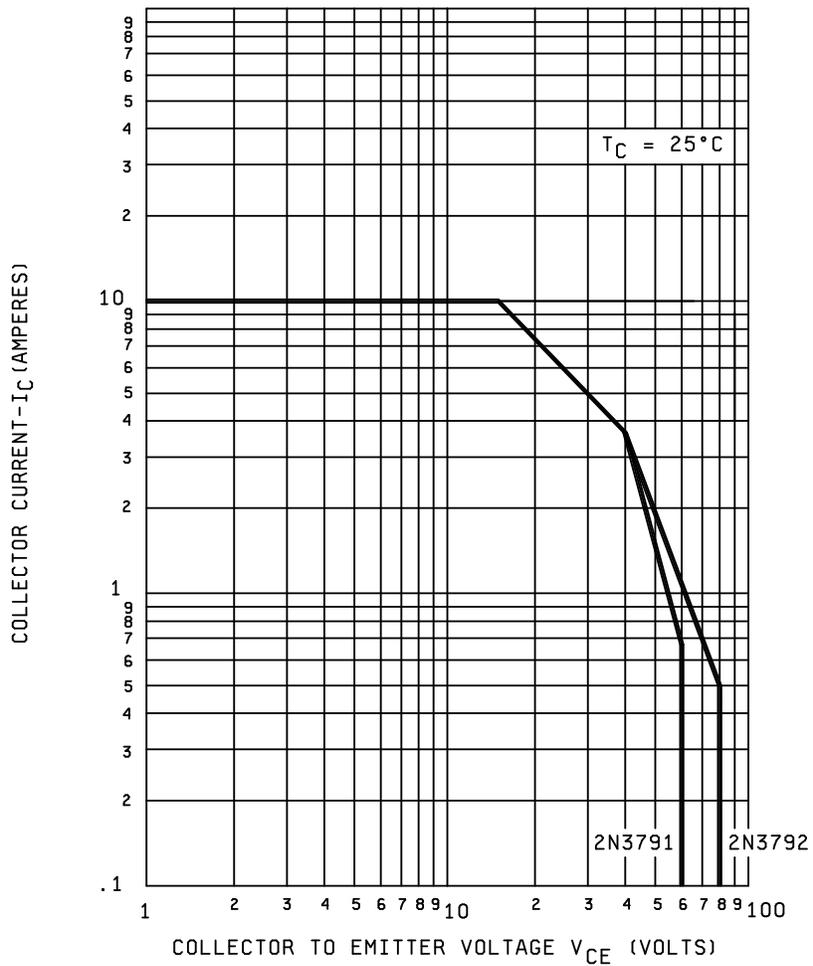


FIGURE 5. Maximum safe operating graph (dc).

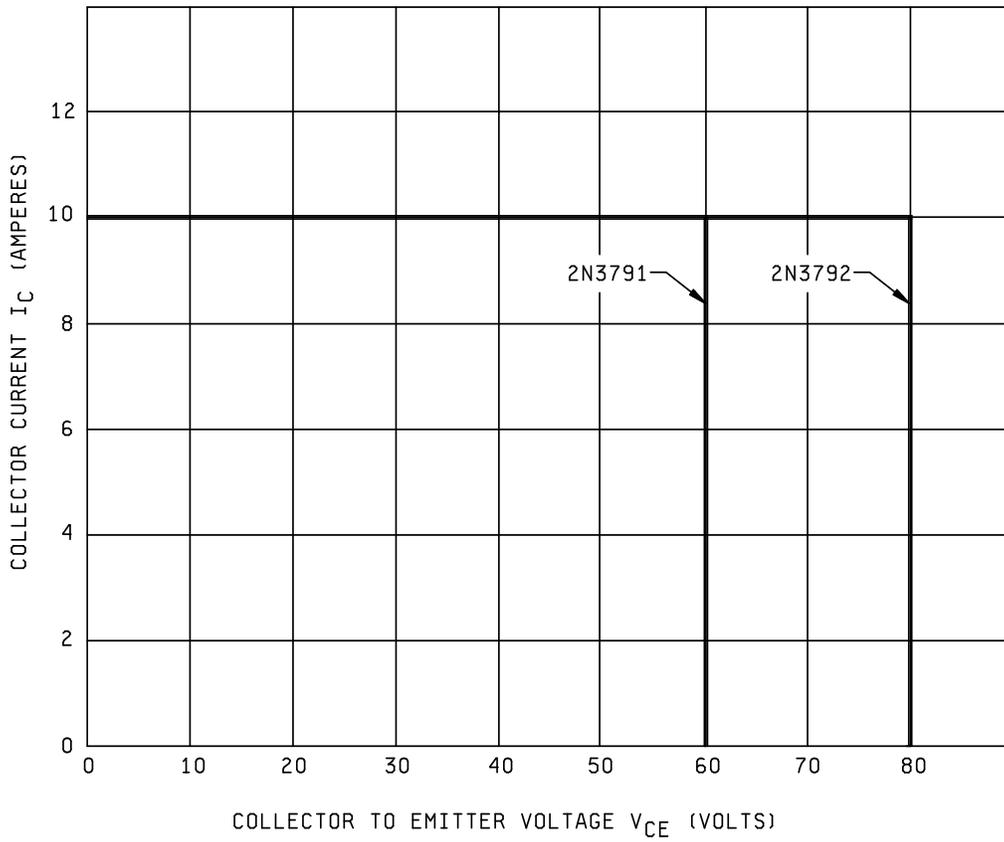
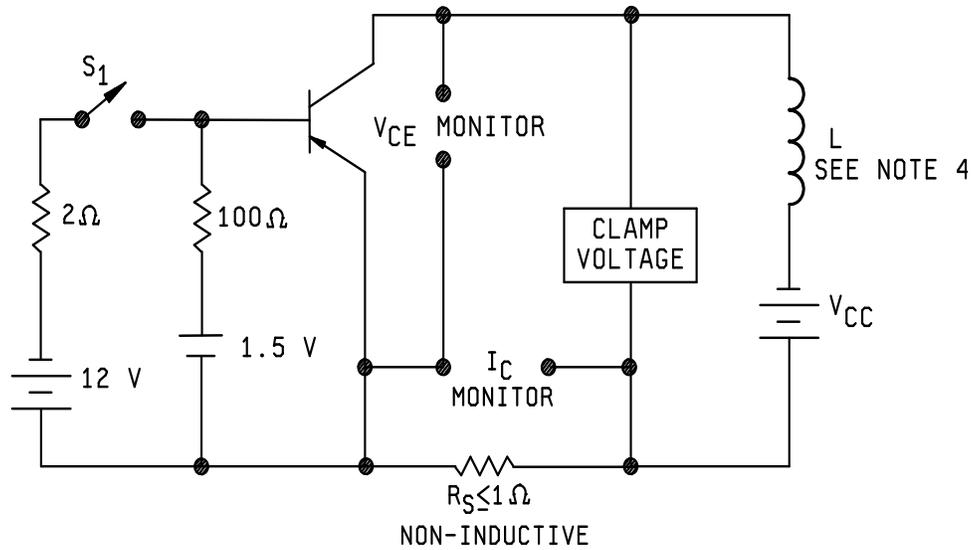


FIGURE 6. Safe operating area for switching between saturation and cutoff (clamped inductive load).



Procedure:

1. With switch S_1 closed, set the specified test conditions.
2. Open S_1 . Device fails if clamp voltage not reached.
3. Perform specified end point tests.
4. $L = 4 \text{ mH}$, $.05\text{W}$, 20 A .
 $Q | 100$ at 1 kHz .
 (Stanford Miller CK-20 or equivalent.)

FIGURE 7. Clamped inductive sweep test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in [MIL-PRF-19500](#) are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

* 6.2 Acquisition requirements. Acquisition documents should specify the following:

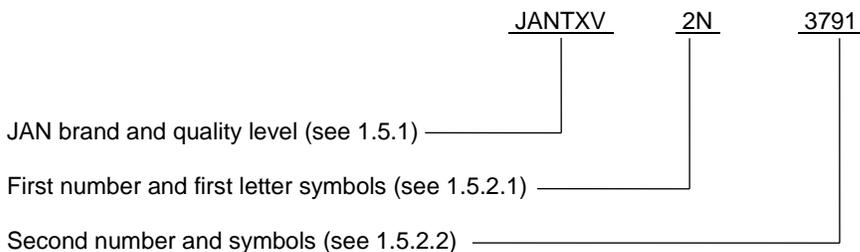
- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. The complete PIN (see 1.2 and 6.5)

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

6.4 Interchangeability information. [MIL-PRF-19500/621](#) is a TO-254 package version of MIL-PRF-19500/379, which is a TO-3 package version. The military 2N7369 contains the same die as the military 2N3792. The [MIL-PRF-19500/621](#) is preferred over the MIL-PRF-19500/379 whenever interchangeability is not a problem. For new design use 2N7369. The 2N3792 is inactive for new design. Transistor types 2N3789 and 2N3790 were deleted by MIL-PRF-19500/379A(ER). The following show the replacement types:

<u>Deleted transistors</u>	<u>Replaced by</u>
2N3789	2N3791
2N3790	2N3792

* 6.5 PIN construction examples.



6.6 List of PINs.

PINs for devices of the base quality level	PINs for devices of the "TX" quality level	PINs for devices of the "TXV" quality level	PINs for devices of the "S" quality level
JAN2N3791	JANTX2N3791	JANTXV2N3791	JANS2N3791
JAN2N3792	JANTX2N3792	JANTXV2N3792	JANS2N3792

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 85
 NASA - NA
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5961-2015-063)

Review activities:
 Army - AR, AV, MI, SM
 Navy - AS, MC
 Air Force - 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.