

The documentation and process conversion measures necessary to comply with this document shall be completed by 19 November 2016.

INCH-POUND

MIL-PRF-19500/313K  
 19 August 2016  
 SUPERSEDING  
 MIL-PRF-19500/313J  
 24 February 2011

PERFORMANCE SPECIFICATION SHEET

\* TRANSISTOR, NPN, SILICON, LOW POWER, TYPES 2N2432, JAN, JANTX, JANTXV, JANS, JANHC, AND JANKC

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-19500](#).

1. SCOPE

\* 1.1 Scope. This specification covers the performance requirements for low power, high speed chopper, NPN silicon transistors. Four levels of product assurance (JAN, JANTX, JANTXV and JANS) are provided for each device type as specified in [MIL-PRF-19500](#). Two levels of product assurance (JANHC and JANKC) are provided for die.

\* 1.2 Package outlines. The device packages for the encapsulated device types are as follows: (TO-18) in accordance with [figure 1](#), (JANHC/JANKC die) in accordance with [figure 2](#), and (UB package) in accordance with [figure 3](#).

1.3 Maximum ratings, unless otherwise specified, T<sub>C</sub> = +25°C.

Type	V <sub>CB0</sub> V <sub>dc</sub>	V <sub>CE0</sub> V <sub>dc</sub>	V <sub>EC0</sub> V <sub>dc</sub>	I <sub>C</sub> mA <sub>dc</sub>	T <sub>J</sub> and T <sub>STG</sub> °C
2N2432, 2N2432UB	30	30	15	100	-65 to
2N2432A, 2N2432AUB	45	45	18	100	+200

Type	P <sub>T</sub> T <sub>A</sub> = +83°C (1)	P <sub>T</sub> T <sub>C</sub> = +150°C (1)	P <sub>T</sub> T <sub>SP</sub> = +165°C	R <sub>θJA</sub> (2)	R <sub>θJC</sub> (2)	R <sub>θJSP</sub> (2)
	mW	mW	mW	°C/W	°C/W	°C/W
2N2432	360	360	N/A	325	150	N/A
2N2432A	360	360	N/A	325	150	N/A
2N2432UB	N/A	N/A	360	N/A	N/A	95
2N2432AUB	N/A	N/A	360	N/A	N/A	95

- (1) For derating, see [figure 4](#) and [figure 5](#).
- (2) For thermal impedance curves, see [figure 6](#), [figure 7](#), and [figure 8](#).

\* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [Semiconductor@dla.mil](mailto:Semiconductor@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.



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1.4 Primary electrical characteristics at  $T_A = +25^\circ\text{C}$ .

Limits	hFE1	hFE2	hFE(inv)1		VCE(sat)	rec(on)	
	VCE = 5 V dc IC = 10 $\mu\text{A}$ dc	VCE = 5 V dc IC = 1 mA dc	VCE = 5 V dc IE = 200 $\mu\text{A}$ dc			IE = 100 $\mu\text{A}$ ac (rms) IB = 1 mA dc, IE = 0, f = 1 kHz	
			2N2432	2N2432A	IC = 10 mA dc IB = 500 $\mu\text{A}$ dc	2N2432 2N2432UB	2N2432A 2N2432AUB
Min	30	80	2	3	V dc	Ohms	Ohms
Max		400			.15	20	15

\* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.5 for PIN construction example, 6.6 for a list of available PINs.

\* 1.5.1 JAN certification mark and quality level.

\* 1.5.1.1 Quality level designators for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JAN", "JANTX", "JANTXV", and "JANS".

\* 1.5.1.2 Quality level designators for unencapsulated devices (die). The quality level designators for unencapsulated devices (die) that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANH" and "JANKC".

\* 1.5.2 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

\* 1.5.2.1 First number and first letter symbols. The transistors of this specification sheet use the first number and letter symbols "2N".

\* 1.5.2.2 Second number symbols. The second number symbols for the transistors covered by this specification sheet are as follows: "2432".

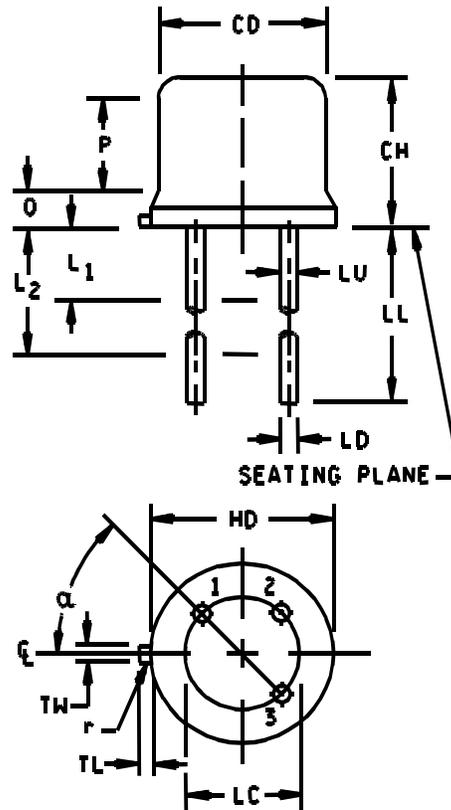
\* 1.5.3 Suffix symbols. The following suffix symbols are incorporated in the PIN as applicable.

	A blank first suffix symbol indicates a standard voltage, axial encapsulated device (see figure 1).
A	An "A" first suffix symbol Indicates higher V <sub>CB0</sub> , V <sub>CEO</sub> , and V <sub>ECO</sub> voltage.
UB	Indicates a surface mount (2N2432UB) (see figure 2)

\* 1.5.4 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.

\* 1.5.5 Die identifiers for unencapsulated device (manufacturers and critical interface identifiers). The manufacturer die identifier that is applicable for this specification sheet is "B" (see figure 2, 6.5, and 6.6).

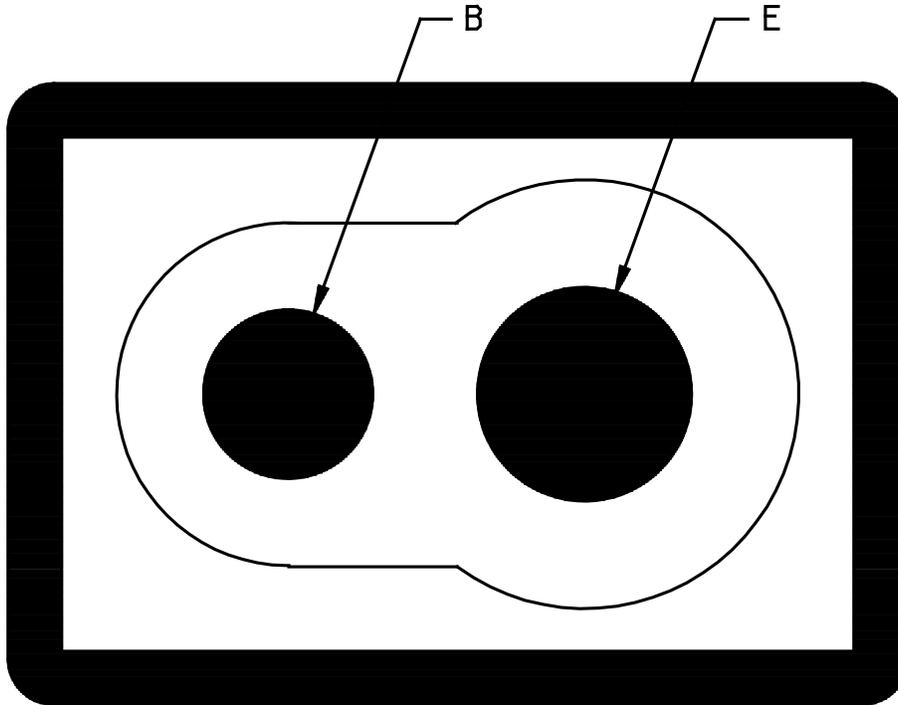
Symbol	Dimensions				Note
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.178	.195	4.52	4.95	
CH	.170	.210	4.32	5.33	
HD	.209	.230	5.31	5.84	
LC	.100 TP		2.54 TP		6
LD	.016	.021	0.41	0.53	7,8
LL	.500	.750	12.70	19.05	7,8
LU	.016	.019	0.41	0.48	7,8
L1		.050		1.27	7,8
L2	.250		6.35		7,8
P	.100		2.54		
Q		.030		0.76	5
TL	.028	.048	0.71	1.22	3,4
TW	.036	.046	0.91	1.17	3
r		.010		0.25	10
$\alpha$	45° TP		45° TP		6



NOTES:

1. Dimension are in inches.
2. Millimeters are given for general information only.
3. Beyond r (radius) maximum, TW shall be held for a minimum length of .011 inch (0.28 mm).
4. Dimension TL measured from maximum HD.
5. Body contour optional within zone defined by HD, CD, and Q.
6. Leads at gauge plane .054 +.001 -.000 inch (1.37 +0.03 -0.00 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
7. Dimension LU applies between L<sub>1</sub> and L<sub>2</sub>. Dimension LD applies between L<sub>2</sub> and LL minimum. Diameter is uncontrolled in L<sub>1</sub> and beyond LL minimum.
8. All three leads.
9. The collector shall be internally connected to the case.
10. Dimension r (radius) applies to both inside corners of tab.
11. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi x$  symbology.
12. Lead 1 = emitter, lead 2 = base, lead 3 = collector.

FIGURE 1. Physical dimensions (similar to TO-18).

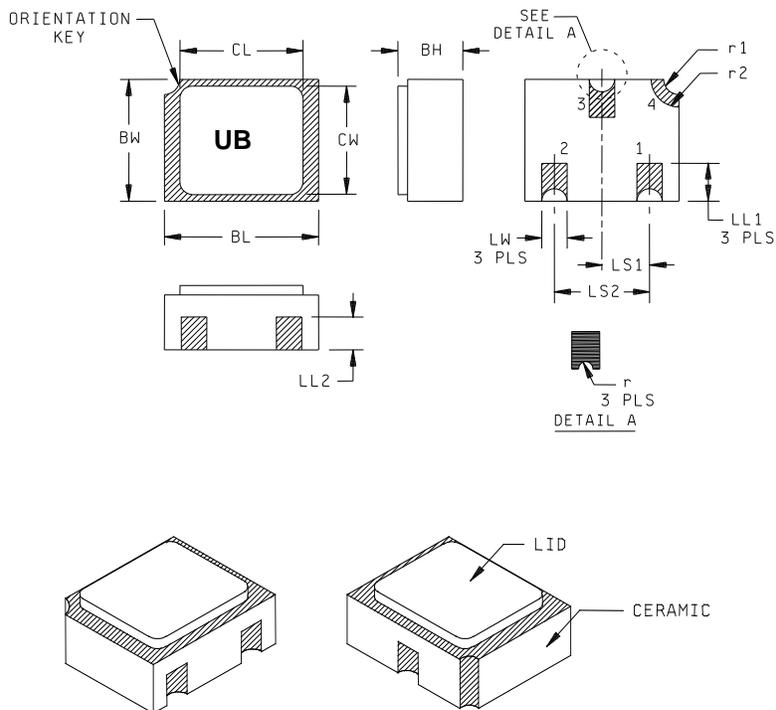


NOTES:

- |                   |   |
|-------------------|---|
| 1. Chip size      | .015 x .019 inch $\pm$ .001 inch, (0.38 x 0.48 $\pm$ 0.02 millimeter).        |
| 2. Chip thickness | .010 $\pm$ .0015 inch, (0.25 $\pm$ 0.04 millimeter).                          |
| 3. Top metal      | Aluminum 15,000Å minimum, 18,000Å nominal.                                    |
| * 4. Back metal   | Gold 3,500Å minimum, 5,000Å nominal.  |
| 5. Backside       | Collector   |
| 6. Bonding pad    | B = .003 inch (0.08 millimeter).<br>E = .004 inch diameter (0.10 millimeter). |
| * 7. Passivation  | Si <sub>3</sub> N <sub>4</sub> (Silicon Nitride) 5.6 kÅ min, 8 kÅ nom.        |
| * 8. See 6.4.     |   |

\* FIGURE 2. Physical dimensions, JANHC and JANKC (B - version) die.

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Symbol	Dimensions				Note	Symbol	Dimensions				Note
	Inches		Millimeters				Inches		Millimeters		
	Min	Max	Min	Max			Min	Max	Min	Max	
BH	.046	.056	1.17	1.42		LS1	.035	.039	0.89	0.99	
BL	.115	.128	2.92	3.25		LS2	.071	.079	1.80	2.01	
BW	.085	.108	2.16	2.74		LW	.016	.024	0.41	0.61	
CL	.115	.128	2.92	3.25		r		.008		0.20	
CW	.085	.108	2.16	2.74		r1		.012		0.31	
LL1	.022	.038	0.56	0.96		r2		.022		0.56	
LL2	.017	.035	0.43	0.89							

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Hatched areas on package denote metallized areas
4. Pad 1 = Base, Pad 2 = Emitter, Pad 3 = Collector, Pad 4 = Shielding connected to the lid.
5. In accordance with ASME Y14.5M, diameters are equivalent to  $\phi$ x symbology.

\* FIGURE 3. Physical dimensions, surface mount (UB version).

## 2. APPLICABLE DOCUMENTS

\* 2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) - Semiconductor Devices, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) - Test Methods for Semiconductor Devices.

\* (Copies of these documents are available online at <http://quicksearch.dla.mil>).

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in [MIL-PRF-19500](#) and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in [MIL-PRF-19500](#) and as follows.

$h_{FE(inv)}$	Forward current transfer ratio except that the collector and emitter shall be interchanged.
$I_e$	Emitter current (rms).
PCB	Printed circuit board.
$r_{ec(on)}$	Small signal emitter to collector on state resistance.
$R_{\theta JA}$	Thermal resistance junction to ambient.
$R_{\theta JC}$	Thermal resistance junction to case.
$R_{\theta JSP}$	Thermal resistance junction to solder pads.
$V_{BC}$	Base to collector voltage.
$V_{(BR)ECO}$	Breakdown voltage, emitter to collector, with base open circuited.
$V_{EC(ofs)}$	Emitter to collector offset voltage, i.e., open circuit voltage between emitter and collector when the base to collector junction is forward biased.
$V_{ec}$	Emitter to collector voltage (rms).

\* 3.4 Interface requirements and physical dimensions. Interface requirements and physical dimensions shall be as specified in [MIL-PRF-19500](#), and on [figure 1](#), [figure 2](#), and [figure 3](#).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with [MIL-PRF-19500](#), [MIL-STD-750](#), and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see [6.2](#)).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in [1.3](#), [1.4](#), and [table I](#).

3.6 Electrical test requirements. The electrical test requirements shall be as specified in [table I](#).

3.7 Marking. Marking shall be in accordance with [MIL-PRF-19500](#).

3.8 Workmanship. Low power transistor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

#### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see [4.2](#)).
- b. Screening (see [4.3](#)).
- c. Conformance inspection (see [4.4](#) and [table I](#) and [table II](#) and [4.5.7](#)).

4.2 Qualification inspection. Qualification inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.2.1 JANHC and JANKC devices. JANHC and JANKC devices shall be qualified in accordance with [MIL-PRF-19500](#).

4.2.2 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table II](#) tests, the tests specified in [table II](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

\* 4.3 Screening (JANS, JANTX, and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500, and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen	Measurement	
	JANS level	JANTX and JANTXV levels
(1) 3c	Thermal impedance, method 3131 of MIL-STD-750, see 4.3.3.	Thermal impedance, method 3131 of MIL-STD-750, see 4.3.3.
7	Optional	Optional
9	$I_{CBO2}$ , $h_{FE1}$	Not applicable
10	48 hours minimum	48 hours minimum
11	$I_{CBO2}$ ; $h_{FE1}$ ; $\Delta I_{CBO2}$ = 100 percent of initial value or 5 nA dc, whichever is greater. $\Delta h_{FE1}$ = $\pm 15$ percent.	$I_{CBO2}$ , $h_{FE1}$
12	See 4.3.1	See 4.3.1
13	Subgroups 2 and 3 of table I herein; $\Delta I_{CBO2}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE1}$ = $\pm 15$ percent.	Subgroup 2 of table I herein; $\Delta I_{CBO2}$ = 100 percent of initial value or 5 nA dc, whichever is greater; $\Delta h_{FE1}$ = $\pm 15$ percent.
14	Required	Required

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

\* 4.3.1 Power burn-in conditions. Power burn-in conditions are as follows:  $V_{CB}$  = 10 - 30 V dc; power shall be applied using a minimum  $P_D$  = 100 percent of  $P_T$  maximum,  $T_A$  ambient rated as defined in 1.3. With approval of the qualifying activity and preparing activity, alternate burn-in criteria (hours, bias conditions,  $T_J$ , and mounting conditions) may be used for JANTX and JANTXV quality levels. A justification demonstrating equivalence is required. In addition, the manufacturing site's burn-in data and performance history will be essential criteria for burn-in modification approval.

4.3.2 Screening (JANHC and JANKC). Screening of JANHC and JANKC die shall be in accordance with MIL-PRF-19500 "Discrete Semiconductor Die/Chip Lot Acceptance". Burn-in duration for the JANKC level follows JANS requirements; the JANHC follows JANTX requirements.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of [MIL-STD-750](#) using the guidelines in that method for determining  $I_M$ ,  $I_H$ ,  $t_H$ ,  $t_{MD}$  (and  $V_C$  where appropriate). The thermal impedance limit shall comply with the thermal impedance graph in [figure 7](#), [figure 8](#), and [figure 9](#) (less than or equal to the curve value at the same  $t_H$  time) or shall be less than the process determined statistical maximum limit as outlined in method 3131 of [MIL-STD-750](#). See [table II](#), subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-19500](#) and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with [MIL-PRF-19500](#), and [table I](#) herein.

\* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the tests and conditions specified for subgroup testing in table E-VIa (JANS) of [MIL-PRF-19500](#) and 4.4.2.1. Electrical measurements (end-points) and delta requirements shall be in accordance with [table I](#), subgroup 2 and 4.5.7 herein. See 4.4.2.2 for JAN, JANTX, and JANTXV group B testing. Electrical measurements (end-points) and delta requirements for JAN, JANTX, and JANTXV shall be after each step in 4.4.2.2 and shall be in accordance with [table I](#), subgroup 2 and 4.5.7 herein.

\* 4.4.2.1 Group B inspection (JANS), table E-VIa of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
* B4	1037	$V_{CB} = 10 - 30$ V dc.
* B5	1027	$V_{CB} = 10 - 30$ V dc; $P_D \geq 100$ percent of maximum rated $P_T$ (see 1.3). (NOTE: If a failure occurs, resubmission shall be at the test conditions of the original sample.)  Option 1: 96 hours minimum sample size in accordance with <a href="#">MIL-PRF-19500</a> , table VIa, adjust $T_A$ to achieve $T_J = +275^\circ\text{C}$ minimum.  Option 2: 216 hours minimum, sample size = 45, $c = 0$ ; adjust $T_A$ to achieve a $T_J = +225^\circ\text{C}$ minimum.

4.4.2.2 Group B inspection, (JAN, JANTX, and JANTXV). Separate samples may be used for each step. In the event of a lot failure, the resubmission requirements of [MIL-PRF-19500](#) shall apply. In addition, all catastrophic failures during CI shall be analyzed to the extent possible to identify root cause and corrective action. Whenever a failure is identified as wafer lot or wafer processing related, the entire wafer lot and related devices assembled from the wafer lot shall be rejected unless an appropriate determined corrective action to eliminate the failures mode has been implemented and the devices from the wafer lot are screened to eliminate the failure mode.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
* 1	1026	Steady-state life: 1,000 hours minimum, $V_{CB} = 10 - 30$ V dc, power shall be applied and adjust $T_A$ to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 100$ percent of maximum rated $P_T$ as defined in 1.3. $n = 45$ devices, $c = 0$ . The sample size may be increased and the test Time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours.
2	1048	Blocking life, $T_A = +150^\circ\text{C}$ , $V_{CB} = 80$ percent of rated voltage, 48 hours minimum. $n = 45$ devices, $c = 0$ .
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$ . $n = 22$ , $c = 0$ .

4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot. For JANS, samples shall be selected from each inspection lot. See [MIL-PRF-19500](#).
- b. Must be chosen from an inspection lot that has been submitted to and passed [table I](#), subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (subgroups B4 and B5 for JANS, and group B for JAN, JANJ, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

\* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of [MIL-PRF-19500](#), and in [4.4.3.1](#) (JANS) and [4.4.3.2](#) (JAN, JANTX, and JANTXV) herein for group C testing. Electrical measurements (end-points) and delta requirements shall be in accordance with [table I](#), subgroup 2 and [4.5.7](#).

\* 4.4.3.1 Group C inspection (JANS), table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; (not applicable for UB devices).
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3) and applied thermal impedance curves.
* C6	1026	1,000 hours at $V_{CB} = 10 - 30$ V dc; power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum and a minimum of $P_D = 100$ percent of maximum rated $P_T$ as defined in <a href="#">1.3</a> $n = 45$ , $c = 0$ . The sample size may be increased and the test time decreased as long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is at least 340 hours, adjust $T_A$ .

4.4.3.2 Group C inspection (JAN, JANJ, JANTX, and JANTXV), table E-VII of [MIL-PRF-19500](#).

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Test condition E; not applicable for UB devices.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see <a href="#">1.3</a> ).
C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes [table I](#) tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of [MIL-PRF-19500](#) and as specified in [table II](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein; delta measurements shall be in accordance with the applicable steps of [4.5.7](#).

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of [MIL-STD-750](#).

4.5.2 Emitter to collector cutoff current. Method of test shall be in accordance with method 3041 of [MIL-STD-750](#), test condition C, except that all references to the collector and emitter of the transistor under test shall be interchanged.

4.5.3 Emitter to collector breakdown voltage. Method of test shall be in accordance with method 3011 of [MIL-STD-750](#), test condition D, except that all references to the collector and emitter of the transistor under test shall be interchanged.

4.5.4 Forward current transfer ratio (inverted connection). Method of test shall be in accordance with method 3076 of [MIL-STD-750](#), except that all references to the collector and emitter of the transistor under test shall be interchanged. Then  $h_{FE(inv)} = I_E / I_B$ .

4.5.5 Emitter to collector offset voltage. The transistor shall be tested in the circuit on [figure 9](#). The base current shall be adjusted to the specified value. The voltage between the emitter and collector shall be measured using a voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement.

4.5.6 Small signal emitter to collector on-state resistance. The transistor shall be tested in the circuit of [figure 10](#). The base current shall be adjusted to the specified value and an ac sinusoidal signal current,  $I_e$ , of the specified rms value shall be applied between the emitter and collector. The rms voltage,  $V_{ec}$ , between the emitter and collector shall be measured using an ac voltmeter with an input impedance high enough that halving it does not change the measured value within the required accuracy of the measurement. The small signal emitter to collector on-state resistance shall then be determined as follows:

$$r_{ec(on)} = V_{ec} / I_e$$

Where  $V_{ec}$  is the rms voltage between the emitter and collector.

4.5.7 Delta requirements. Delta requirements shall be as specified below: (1) (2) (3) (4)

Step	Inspection	MIL-STD-750		Symbol	Limit	Unit
		Method	Conditions			
1	Collector-base cutoff current  2N2432, 2N2432UB 2N2432A, 2N2432AUB	3036	Bias condition D  $V_{CB} = 25 \text{ V dc}$ $V_{CB} = 40 \text{ V dc}$	$\Delta I_{CB02}$	100 percent of initial value or 5 nA dc, whichever is greater.	
2	Forward current transfer ratio	3076	$V_{CE} = 5 \text{ V dc};$ $I_C = 1.0 \text{ mA dc};$ pulsed see <a href="#">4.5.1</a>	$\Delta h_{FE2}$	$\pm 25$ percent change from initial reading.	

- (1) Devices which exceed the [table I](#) limits for this test shall not be accepted.
- (2) The delta measurements for group B, table E-VIa (JANS) of [MIL-PRF-19500](#) are as follows: Subgroup 3 and 5; see [4.5.7](#) herein, steps 1 and 2.
- (3) The delta measurements for [4.4.2.2](#) herein (group B, JAN, JANTX, and JANTXV) are as follows: Steps 1 and 2 of [4.5.7](#) shall be performed after each step in [4.4.2.2](#) herein.
- (4) The delta measurements for group C, table E-VII of [MIL-PRF-19500](#) are as follows: Subgroup 6, see [4.5.7](#) herein, steps 1 and 2 for JANS only.

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\* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071					
Solderability <u>3/ 4/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/ 5/</u>	1022	n = 15 devices, c = 0				
* Salt atmosphere <u>4/</u>	1041	(Laser marked devices only) n = 6 devices, c = 0.				
Temp cycling <u>3/ 4/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>4/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements <u>4/</u>		Table I, subgroup 2				
Bond strength <u>3/ 4/</u>	2037	Precondition T <sub>A</sub> = +250°C at t = 24 hrs or T <sub>A</sub> = +300°C at  t = 2 hrs n = 11 wires, c = 0				
Decap internal visual design verification <u>4/</u>	2075	n = 4, c = 0.				
<u>Subgroup 2</u>						
Thermal impedance <u>6/</u>	3131	See 4.3.3	Z <sub>θJX</sub>			°C/W
Breakdown voltage collector to emitter  2N2432, 2N2432UB 2N2432A, 2N2432AUB	3011	Bias condition D; I <sub>C</sub> = 10 mA dc; pulsed (see 4.5.1).	V <sub>(BR)CEO</sub>	30 45		V dc V dc
Collector to base cutoff current  2N2432, 2N2432UB 2N2432A, 2N2432AUB	3036	Bias condition D  V <sub>CB</sub> = 30 V dc V <sub>CB</sub> = 45 V dc	I <sub>CB01</sub>		100 100	μA dc μA dc
Breakdown voltage emitter to collector  2N2432, 2N2432UB 2N2432A, 2N2432AUB	3011	Bias condition D; I <sub>E</sub> = 100 μA dc; I <sub>B</sub> = 0 (see 4.5.3).	V <sub>(BR)EC01</sub>	15 18		V dc V dc
Breakdown voltage emitter to collector	3011	Bias condition D; I <sub>E</sub> = 10 mA dc; I <sub>B</sub> = 0; pulsed (see 4.5.1 and 4.5.3)	V <sub>(BR)EC02</sub>	10		V dc

See footnotes at end of table.

\* TABLE I. Group A inspection - Continued.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> - Continued						
Collector to base cutoff current	3036	Bias condition D	ICBO2			
2N2432, 2N2432UB		V <sub>CE</sub> = 25 V dc			10	nA dc
2N2432A, 2N2432AUB		V <sub>CE</sub> = 40 V dc			10	nA dc
Collector to emitter cutoff current	3041	Bias condition C	ICES1			
2N2432, 2N2432UB		V <sub>CB</sub> = 25 V dc			10	nA dc
2N2432A, 2N2432AUB		V <sub>CB</sub> = 40 V dc			10	nA dc
Emitter to collector cutoff current	3041	Bias condition C; V <sub>EC</sub> = 15 V dc; V <sub>BC</sub> = 0; (see 4.5.2)	IECS1		2	nA dc
Emitter to base cutoff current	3061	Bias condition D; V <sub>EB</sub> = 15 V dc	IEBO		2	nA dc
Forward-current transfer ratio	3076	V <sub>CE</sub> = 5 V dc; I <sub>C</sub> = 10 μA dc	h <sub>FE1</sub>	30		
Forward-current transfer ratio	3076	V <sub>CE</sub> = 5 V dc; I <sub>C</sub> = 1 mA dc	h <sub>FE2</sub>	80	400	
Forward-current transfer ratio (inverted connection)	3076	V <sub>CE</sub> = 5 V dc; I <sub>E</sub> = 0.2 mA dc; (see 1.4 and 4.5.4)	h <sub>FE(inv)1</sub>			
2N2432, 2N2432UB				2		
2N2432A, 2N2432AUB				3		
Saturation voltage and resistance	3071	I <sub>C</sub> = 10 mA dc; I <sub>B</sub> = 0.5 mA dc See 1.4.	V <sub>CE(sat)</sub>		0.15	V dc
Emitter to collector offset voltage		I <sub>B</sub> = 200 μA dc; I <sub>E</sub> = 0 mA dc (see 4.5.5 and figure 9)	V <sub>EC(ofs)1</sub>			
2N2432, 2N2432UB					0.5	mV dc
2N2432A, 2N2432AUB					0.4	mV dc
Emitter to collector offset voltage		I <sub>B</sub> = 1 mA dc; I <sub>E</sub> = 0 mA dc (see 4.5.5 and figure 9)	V <sub>EC(ofs)2</sub>			
2N2432, 2N2432UB					1.0	mV dc
2N2432A, 2N2432AUB					0.7	mV dc
<u>Subgroup 3</u>						
High-temperature operation:		T <sub>A</sub> = +125°C				
Collector to emitter cutoff current	3041	Bias condition C	ICES2			
2N2432, 2N2432UB		V <sub>CE</sub> = 25 V dc			250	nA dc
2N2432A, 2N2432AUB		V <sub>CE</sub> = 40 V dc			250	nA dc

See footnotes at end of table.

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\* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - Continued						
Emitter to collector cutoff current	3041	Bias condition C; $V_{EC} = 15$ V dc; $V_{BC} = 0$ (see 4.5.2)	$I_{ECS2}$		200	nA dc
Low-temperature operation:		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 5$ V dc; $I_C = 10$ $\mu\text{A}$ dc; pulsed (see 4.5.1)	$h_{FE3}$	10		
Forward-current transfer ratio	3076	$V_{CE} = 5$ V dc; $I_C = 1$ mA dc; pulsed (see 4.5.1)	$h_{FE4}$	25		
Forward-current transfer ratio (inverted connection)	3076	$V_{CE} = 5$ V dc; $I_E = 200$ $\mu\text{A}$ dc; pulsed (see 4.5.1 and 4.5.4)	$h_{FE(inv)2}$	1.8		
<u>Subgroup 4</u>						
Small signal emitter collector on state resistance		$I_B = 1$ mA dc; $I_E = 0$ ; $I_e = 100$ $\mu\text{A}$ ac (rms); $f = 1$ kHz (see 4.5.6 and figure 10)	$r_{ec(on)}$			
2N2432, 2N2432UB 2N2432A, 2N2432AUB					20 15	$\Omega$ $\Omega$
Small-signal short-circuit forward- current transfer ratio	3306	$V_{CE} = 5$ V dc; $I_C = 1$ mA dc; $f = 20$ MHz	$ h_{fe} $	2	10	
Open circuit output capacitance	3236	$V_{CB} = 0$ ; $I_E = 0$ ; $100$ kHz $\leq f \leq 1$ MHz	$C_{obo}$		12.0	pF
Input capacitance	3240	$V_{EB} = 0$ V dc; $I_C = 0$ ; $100$ kHz $\leq f \leq 1$ MHz	$C_{ibo}$		12.0	pF
<u>Subgroups 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not applicable for JANS devices.

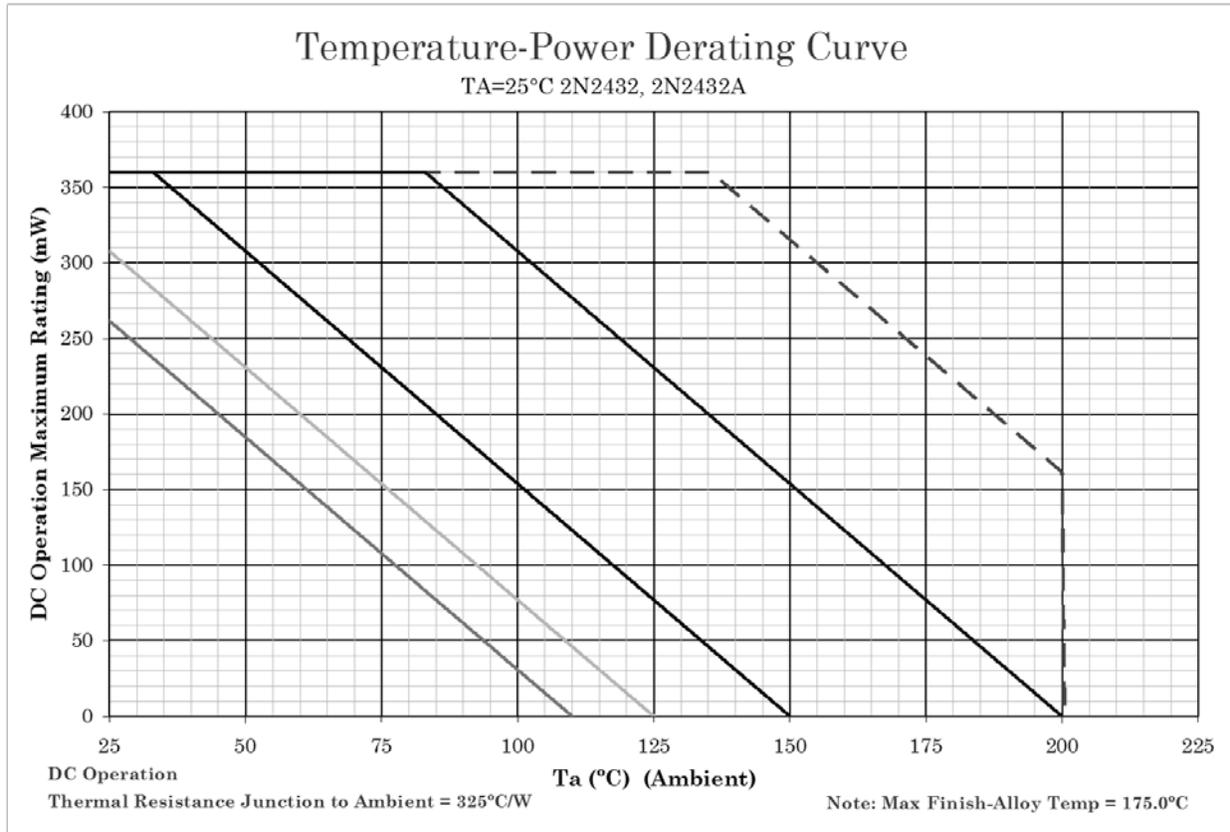
5/ Not required for laser marked devices.

\* 6/ This test required for the following end-point measurements only:  
Group B, subgroup 3, 4, and 5 (JANS).  
Group B, step 1 (TX and TXV).  
Group C, subgroup 2 and 6.

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\* TABLE II. Group E inspection (all quality levels) - for qualification only.

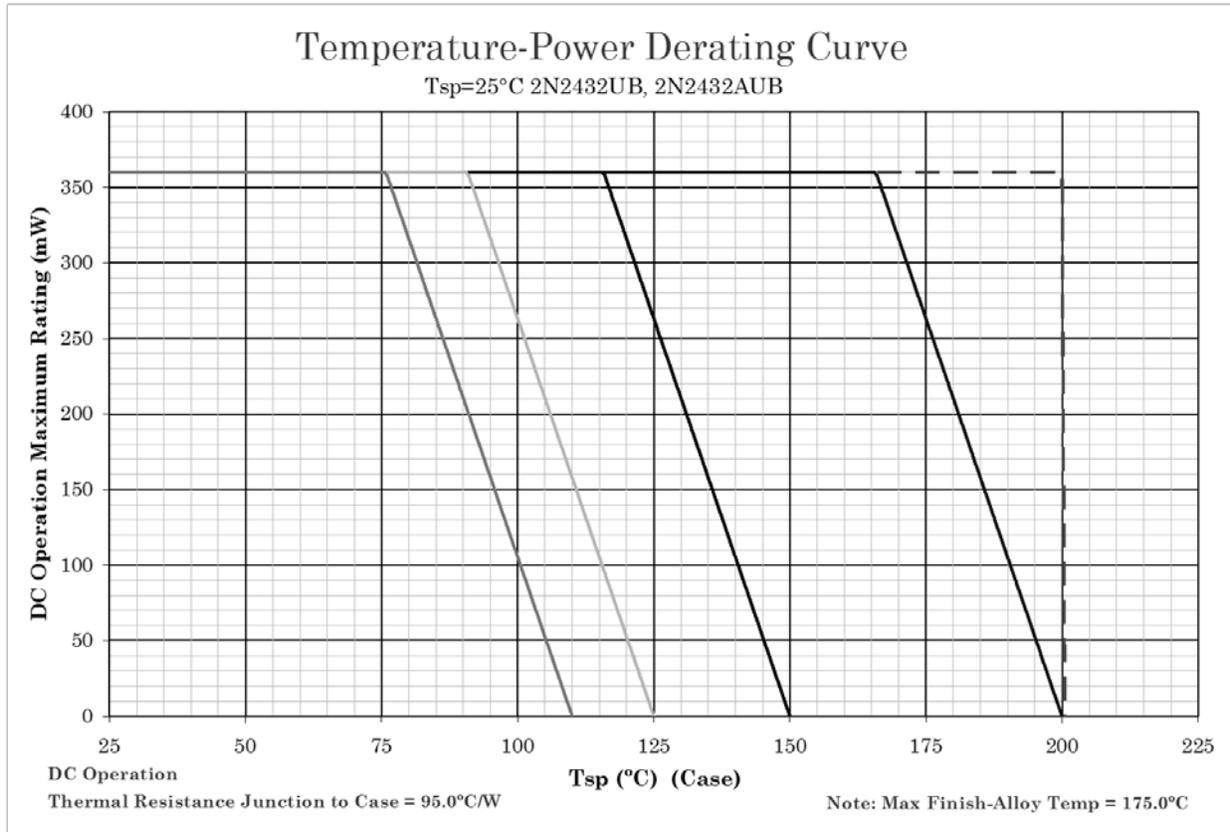
Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak Gross leak			
Electrical measurements		See <a href="#">table I</a> , subgroup 2 and <a href="#">4.5.7</a> herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	V <sub>CB</sub> = 10 V dc, 6,000 cycles, forced air cooling allowed on cooling cycle only.	
Electrical measurements		See <a href="#">table I</a> , subgroup 2 and <a href="#">4.5.7</a> herein.	
<u>Subgroup 4</u>			
Thermal resistance	3131	R <sub>θJSF</sub> can be calculated but shall be measured once in the same package with a similar die size to confirm calculations (may apply to multiple specification sheets).	15 devices, c = 0
Thermal impedance curves		See table E-IX of <a href="#">MIL-PRF-19500</a> , group E, subgroup 4.	Sample size N/A
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			11 devices
ESD	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B	



## NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq +150^\circ\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq +125^\circ\text{C}$ , and  $+110^\circ\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 4. Derating for all devices ( $R_{\theta JA}$ ) for 2N2432 and 2N2432A.

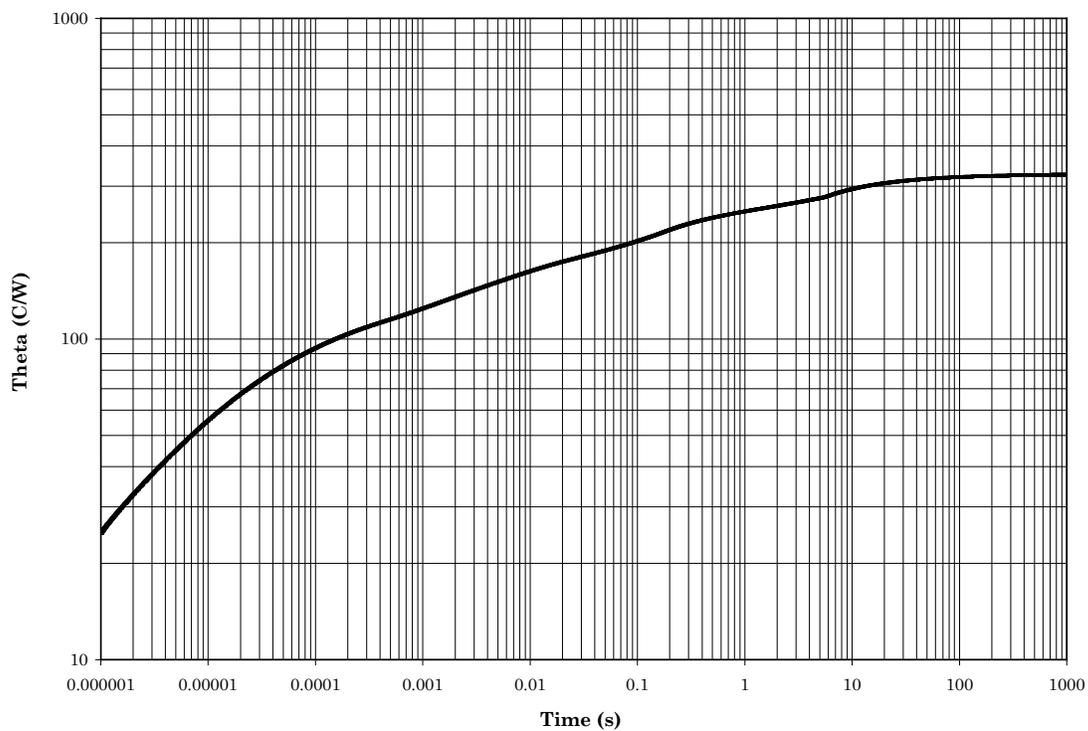


## NOTES:

1. Top curve is thermal runaway loci and cannot be used as a derate design curve since it exceeds the maximum ratings for this part. Operating under this curve using these mounting conditions assures the device will not have a thermal runaway. This is the true inverse of the worst case thermal resistance value extrapolated out to the thermal runaway point.
2. Derate design curve constrained by the maximum junction temperatures and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at  $T_J \leq +150^{\circ}\text{C}$ , where the maximum temperature of electrical test is performed.
4. Derate design curve chosen at  $T_J \leq +125^{\circ}\text{C}$ , and  $+110^{\circ}\text{C}$  to show power rating where most users want to limit  $T_J$  in their application.

FIGURE 5. Derating for all devices ( $R_{\theta JA}$ ) for 2N2432UB and 2N2432AUB.

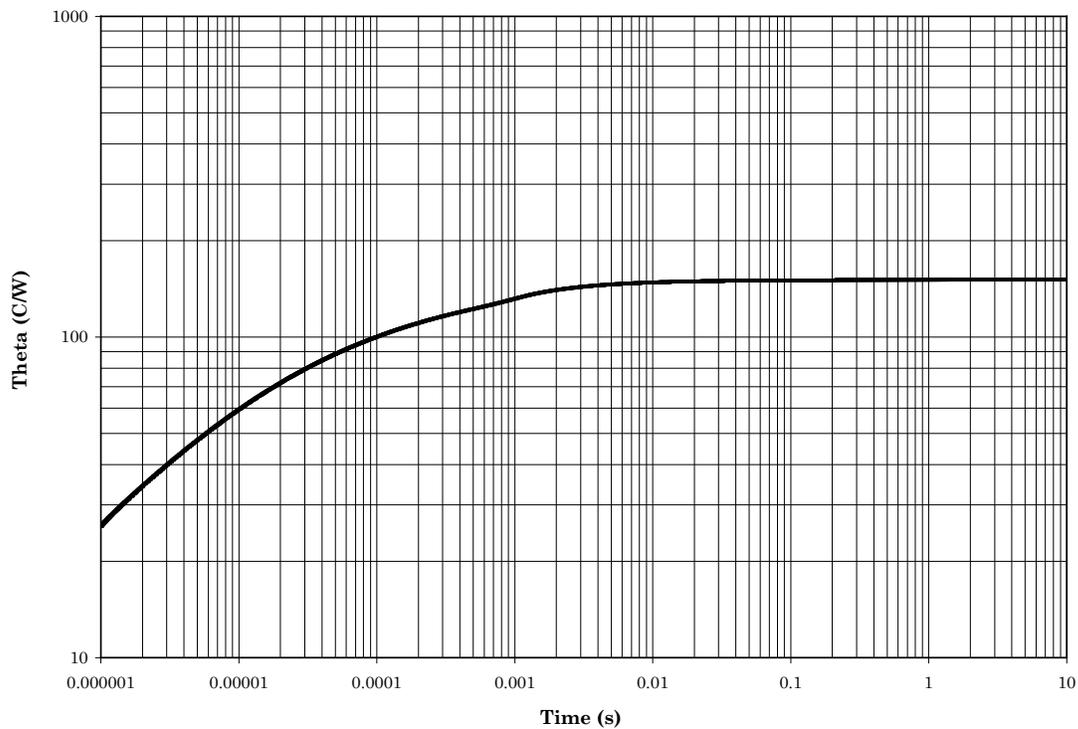
### Maximum Thermal Impedance



Resistance  $R_{\theta JA} = 325^{\circ}\text{C/W}$ .

FIGURE 6. Thermal impedance graph ( $R_{\theta JA}$ ) for 2N2432 and 2N2432A.

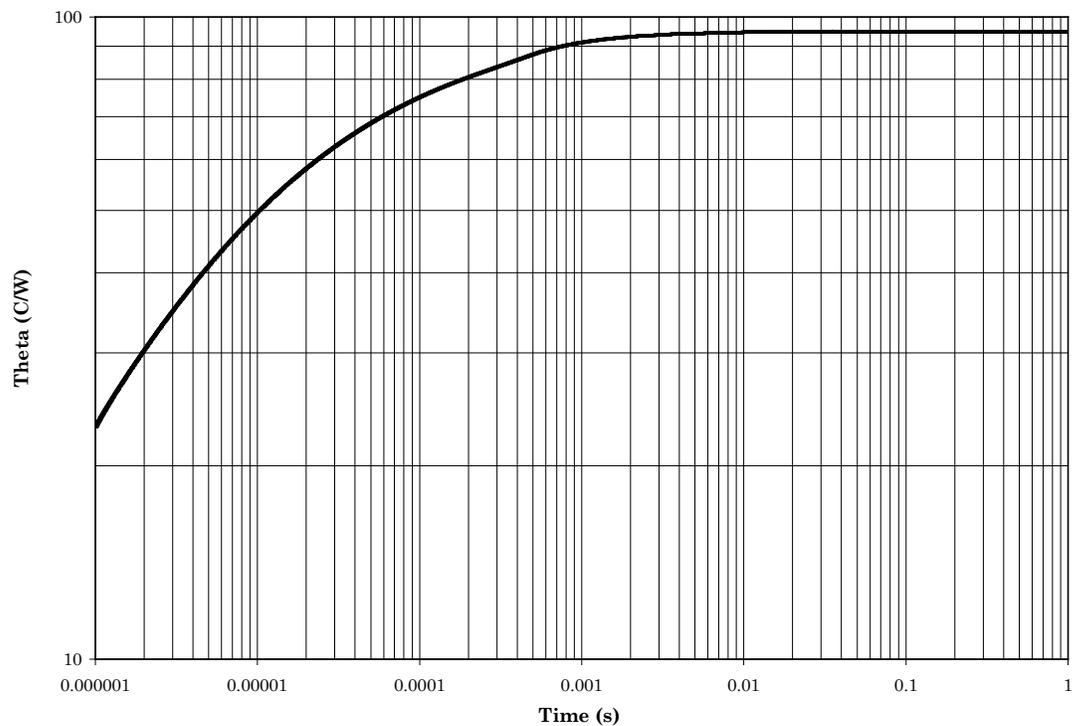
### Maximum Thermal Impedance



Resistance  $R_{\theta JC} = 150^{\circ}\text{C/W}$ .

FIGURE 7. Thermal impedance graph ( $R_{\theta JC}$ ) for 2N2432 and 2N2432A.

### Maximum Thermal Impedance



Resistance  $R_{\theta JSP} = 95^{\circ}\text{C/W}$ .

FIGURE 8. Thermal impedance graph ( $R_{\theta JSP}$ ) for 2N2432UB and 2N2432AUB.

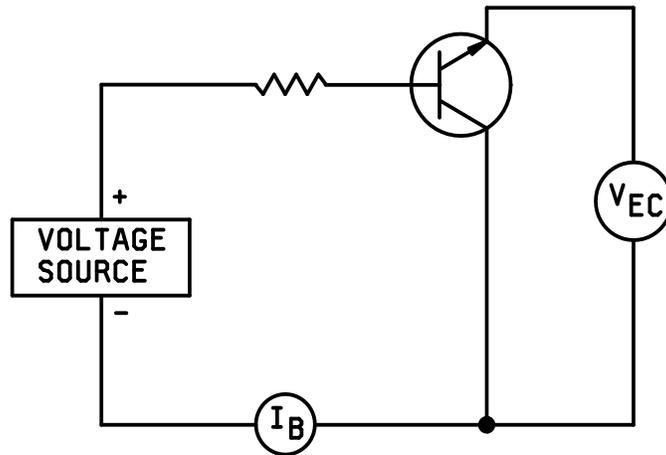


FIGURE 9. Emitter to collector offset voltage test circuit.

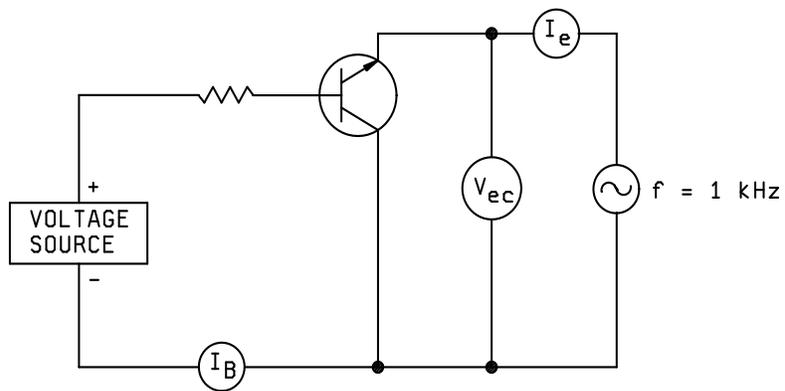


FIGURE 10. Small-signal emitter-collector on-state resistance test circuit.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

\* 6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).

\* d. The complete Part or Identifying Number (PIN), see title and section 1.

\* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List ((QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [vqe.chief@dla.mil](mailto:vqe.chief@dla.mil). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

\* 6.4 Suppliers of JANHC and JANKC die. The qualified JANHC and JANKC suppliers with the applicable letter version (example JANHCB2N2434A) will be identified on the QML.

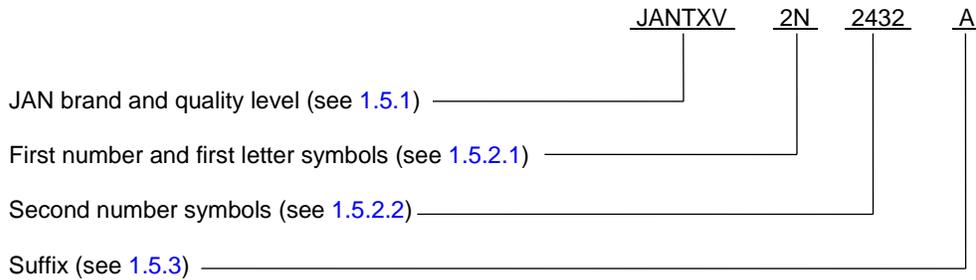
JANC ordering information	
PIN	Manufacturer
	43611
2N2432 2N2434A	JANHCB2N2434A JANKCB2N2434A

NOTE: The previous JANHC and JANKC (A version) was never qualified and has been removed in MIL-PRF19500/313J.

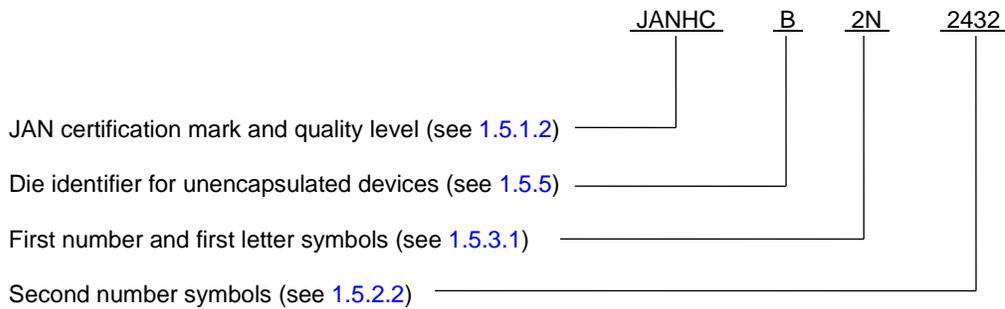
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\* 6.5 PIN construction example. The PINs for encapsulated devices are construction using the following form.

\* 6.5.1 Encapsulated devices The PINs for encapsulated devices are constructed using the following form.



\* 6.5.2 Unencapsulated devices. The PINs for un-encapsulated devices are constructed using the following form.



\* 6.6 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for types 2N2432, 2N2432A, 2N2432UB, and 2N2432AUB			
JAN2N2432	JANTX2N2432	JANTXV2N2432	JANS2N2432
JAN2N2432A	JANTX2N2432A	JANTXV2N2432A	JANS2N2432A
JAN2N2432UB	JANTX2N2432UB	JANTXV2N2432UB	JANS2N2432UB
JAN2N2432AUB	JANTX2N2432AUB	JANTXV2N2432AUB	JANS2N2432AUB
	JANHC2N2432	JANHC2N2432A	

6.7 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR  
Navy - EC  
Air Force - 85  
NASA - NA  
DLA - CC

Preparing activity:

DLA - CC

(Project 5961-2016-079)

Review activities:

Army - MI  
Navy - AS, MC  
Air Force - 19

\* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.