

INCH-POUND

The documentation and process conversion measures necessary to comply with this document shall be completed by 25 April 2011.

MIL-PRF-19500/225K
25 January 2011
SUPERSEDING
MIL-PRF-19500/225J
6 July 2007

PERFORMANCE SPECIFICATION SHEET

* SEMICONDUCTOR DEVICE, TRANSISTOR, NPN, SILICON,
TYPES 2N1711, 2N1711S, 2N1890, AND 2N1890S, JAN, JANTX, AND JANTXV

This specification is approved for use by all Departments
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of
this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for NPN, silicon, low-power transistors. Two levels of product assurance are provided for each device type as specified in MIL-PRF-19500.

1.2 Physical dimensions. See figure 1 (similar to TO-5).

1.3 Maximum ratings. Unless otherwise specified $T_A = +25^\circ\text{C}$.

Type (1)	P_T (2) $T_C = +25^\circ\text{C}$	P_T (2) $T_A = +25^\circ\text{C}$	$R_{\theta JA}$ (3)	$R_{\theta JC}$ (3)	I_C	V_{CBO}	V_{CER} $R_{BE} = 10 \Omega$	V_{CEO}	V_{EBO}	T_J and T_{STG}
	<u>W</u>	<u>W</u>	<u>$^\circ\text{C/W}$</u>	<u>$^\circ\text{C/W}$</u>	<u>mA dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>$^\circ\text{C}$</u>
2N1711	3.0	0.8	175	30	500	75	50	30	7	-65 to
2N1890	3.0	0.8	175	30	500	100	80	60	7	+200

- (1) Also applies to the corresponding "S" suffix device.
- (2) For derating see figures 2 and 3.
- (3) For thermal impedance curves see figures 4 and 5.

* Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.daps.dla.mil>.

1.4 Primary electrical characteristics.

Limits	h_{FE1} (1)	h_{FE2} (1)	$ h_{fe} $	$V_{CE(SAT)}$		
	$V_{CE} = 10$ V dc $I_C = 10$ μ A dc	$V_{CE} = 10$ V dc $I_C = 150$ mA dc		f = 20 MHz $V_{CE} = 10$ V dc $I_E = 50$ mA dc	2N1711, S (1) $I_C = 150$ mA dc $I_B = 15$ mA dc	2N1890, S (1) $I_C = 150$ mA dc $I_B = 15$ mA dc
Min	20	100	3.5	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>
Max		300	12	1.5	5.0	1.2

(1) Pulsed (see 4.5.1).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.

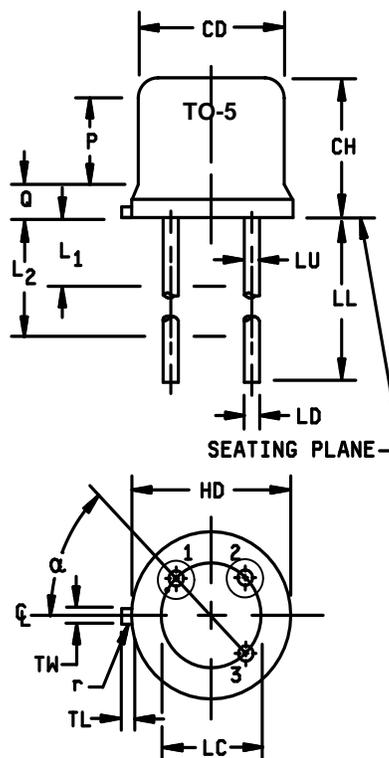
DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Methods for Semiconductor Devices.

* (Copies of these documents are available online at <https://assist.daps.dla.mil/quicksearch> or <https://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

* 2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CD	.305	.335	7.75	8.51	
CH	.240	.260	6.10	6.60	
HD	.335	.370	8.51	9.40	
LC	.200 TYP		5.08 TYP		7
LD	.016	.021	0.41	0.53	6
LL	See notes 7, 9, and 10				
LU	.016	.019	0.41	0.48	7
L ₁		.050		1.27	7
L ₂	.250		6.35		7
P	.100		2.54		5
Q		.050		1.27	
r		.010		0.254	8
TL	.029	.045	0.74	1.14	4
TW	.028	.034	0.71	0.86	3
α	45° TP		45° TP		6
Term 1	Emitter				
Term 2	Base				
Term 3	Collector				



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. Beyond r maximum, TW must be held to a minimum length of .021 inch (0.53 mm).
4. TL measured from maximum HD.
5. CD shall not vary more than ± 0.010 inch (0.25 mm) in zone P. This zone is controlled for automatic handling.
6. Leads at gauge plane .054 - .055 inch (1.37 - 1.40 mm) below seating plane shall be within .007 inch (0.18 mm) radius of true position (TP) at a maximum material condition (MMC) relative to the tab at MMC. The device may be measured by direct methods or by gauge and gauging procedure.
7. LU applies between L₁ and L₂. LD applies between L₂ and L minimum. Diameter is uncontrolled in L₁ and beyond LL minimum.
8. r (radius) applies to both inside corners of tab.
9. For transistor types 2N1711S and 2N1890S, LL is .500 inch (12.70 mm) minimum, and .750 inch (19.05 mm) maximum (TO-5).
10. For transistor types 2N1711 and 2N1890, LL is 1.500 inches (38.10 mm) minimum, and 1.750 inches (44.45 mm) maximum (TO-5).
11. In accordance with ASME Y14.5M, diameters are equivalent to ϕx symbology.

FIGURE 1. Physical dimensions (TO-5).

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. Interface and physical dimensions shall be as specified in MIL-PRF-19500, and on figure 1 (TO-5).

3.4.1 Lead finish. Lead finish shall be solderable in accordance with MIL-PRF-19500, MIL-STD-750, and herein. Where a choice of lead finish is desired, it shall be specified in the acquisition document (see 6.2).

3.5 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I.

3.6 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.7 Marking. Marking shall be in accordance with MIL-PRF-19500.

3.8 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of table II tests, the tests specified in table II herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.3 Screening (list applicable JANTX and JANTXV levels). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500)	Measurement
	JANTX and JANTXV level
(1) 3c	Thermal impedance (see 4.3.2), method 3131 of MIL-STD-750.
9	Not applicable.
11	h_{FE2} ; I_{CBO1}
12	See 4.3.1.
13	ΔI_{CBO1} = 100 percent of initial value or 5 nA dc; whichever is greater; Δh_{FE2} = ± 15 percent of initial value.

(1) Shall be performed anytime after temperature cycling, screen 3a; and does not need to be repeated in screening requirements.

4.3.1 Burn-in conditions. Burn-in conditions are as follows: $V_{CB} = 10 - 30$ V dc. Power shall be applied to achieve $T_J = +135^\circ\text{C}$ minimum using a minimum $P_D = 75$ percent of P_T maximum, T_A ambient rated as defined in 1.3. NOTE: No heat sink or forced air cooling of the devices shall be permitted.

4.3.2 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3131 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} (V_C and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μs max. See table II, group E, subgroup 4 herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with MIL-PRF-19500, and table I herein. The test conditions for $Z_{\theta JX}$ shall be those used in 4.3.2.

4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified in 4.4.2.1 herein. Electrical measurements (end-points) shall be in accordance with the applicable inspections of table I, group A, subgroup 2 herein.

* 4.4.2.1 Group B inspection, JAN, JANTX, and JANTXV.

<u>Step</u>	<u>Method</u>	<u>Condition</u>
1	1026	Steady-state life: Test condition B, 1,000 hours minimum, $V_{CB} = 10$ V dc, power shall be applied to achieve $T_J = +150^\circ\text{C}$ minimum using a minimum of $P_D = 75$ percent of maximum rated P_T as defined in 1.3. $n = 45$ devices, $c = 0$. The sample size may be increased and the test time decreased so long as the devices are stressed for a total of 45,000 device hours minimum, and the actual time of test is a minimum of 340 hours.
* 2	1048	Blocking life, $T_A = 150^\circ\text{C}$, $V_{CB} = 80$ percent of rated voltage, without going over the maximum rated V_{CE} , 48 hours minimum. $n = 45$ devices, $c = 0$.
3	1032	High-temperature life (non-operating), $t = 340$ hours, $T_A = +200^\circ\text{C}$. $n = 22$, $c = 0$.

* 4.4.2.3 Group B sample selection. Samples selected from group B inspection shall meet all of the following requirements:

- * a. For JAN, JANTX, and JANTXV samples shall be selected randomly from a minimum of three wafers (or from each wafer in the lot) from each wafer lot.
- * b. Shall be chosen from an inspection lot that has been submitted to and passed table I, subgroup 2, conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for life test (group B for JAN, JANTX, and JANTXV) may be pulled prior to the application of final lead finish.

* 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500, and as follows. Electrical measurements (end-points) shall be in accordance with table I, group A, subgroup 2 herein.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
C2	2036	Lead fatigue: Test condition E.
C5	3131	$R_{\theta JA}$ and $R_{\theta JC}$ only, as applicable (see 1.3 and 4.3.2).
* C6		Not applicable.

4.4.3.3 Group C sample selection. Samples for subgroups in group C shall be chosen at random from any inspection lot containing the intended package type and lead finish procured to the same specification which is submitted to and passes table I tests herein for conformance inspection. When the final lead finish is solder or any plating prone to oxidation at high temperature, the samples for C6 life test may be pulled prior to the application of final lead finish. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup.

4.4.4 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in table II herein. Electrical measurements (end-points) shall be in accordance with table I, subgroup 2 herein.

4.5 Method of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

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* TABLE I. Group A inspection.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1 2/</u>						
Visual and mechanical examination <u>3/</u>	2071	n = 45 devices, c = 0				
Solderability <u>3/</u>	2026	n = 15 leads, c = 0				
Resistance to solvents <u>3/ 4/</u>	1022	n = 15 devices, c = 0				
Temp cycling <u>3/</u>	1051	Test condition C, 25 cycles. n = 22 devices, c = 0				
Hermetic seal <u>5/</u> Fine leak Gross leak	1071	n = 22 devices, c = 0				
Electrical measurements		Table I, subgroup 2				
Bond strength <u>3/</u>	2037	Precondition T _A = +250°C at t = 24 hours or T _A = +300°C at t = 2 hours n = 11 wires, c = 0				
Decap internal visual (design verification)	2075	n = 4 devices, c = 0				
<u>Subgroup 2</u>						
* Thermal impedance <u>6/</u>	3131	See 4.3.2	Z _{θJX}			°C/W
Breakdown voltage, collector to emitter 2N1711, 2N1711S 2N1890, 2N1890S	3011	Bias condition D; I _C = 30 mA dc; pulsed (see 4.5.1).	V _{(BR)CEO}	30 60		V dc V dc
Breakdown voltage, collector to emitter 2N1711, 2N1711S 2N1890, 2N1890S	3011	Bias condition D; I _C = 100 mA dc; pulsed (see 4.5.1). R _{BE} = 10 Ω.	V _{(BR)CER}	50 80		V dc V dc
Collector to base cutoff current 2N1711, 2N1711S 2N1890, 2N1890S	3036	Bias condition D V _{CB} = 60 V dc V _{CB} = 80 V dc	I _{CB01}		10 10	nA dc nA dc

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1</u> /	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 2</u> – Continued.						
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 5 \text{ V dc}$	I_{EBO1}		5.0	nA dc
Collector to base cutoff current	3036	Bias condition D	I_{CBO2}			
2N1711, 2N1711S 2N1890, 2N1890S		$V_{CB} = 75 \text{ V dc}$ $V_{CB} = 100 \text{ V dc}$			100 100	$\mu\text{A dc}$ $\mu\text{A dc}$
Emitter to base cutoff current	3061	Bias condition D; $V_{EB} = 7 \text{ V dc}$	I_{EBO2}		100	$\mu\text{A dc}$
Collector-emitter saturation voltage	3071	$I_C = 150 \text{ mA dc}$; $I_B = 15 \text{ mA dc}$; pulsed (see 4.5.1)	$V_{CE(sat)1}$		1.5 5.0	V dc V dc
2N1711, 2N1711S 2N1890, 2N1890S						
Collector-emitter saturation voltage	3071	$I_C = 50 \text{ mA dc}$; $I_B = 5 \text{ mA dc}$; pulsed (see 4.5.1)	$V_{CE(sat)2}$			V dc
2N1890, 2N1890S					1.2	V dc
Base emitter saturation voltage	3066	Test condition A, $I_C = 150 \text{ mA dc}$, $I_B = 15 \text{ mA dc}$, pulsed (see 4.5.1).	$V_{BE(sat)1}$		1.3	V dc
Base emitter saturation voltage	3066	Test condition A, $I_C = 50 \text{ mA dc}$, $I_B = 5 \text{ mA dc}$, pulsed (see 4.5.1).	$V_{BE(sat)2}$			V dc
2N1890, 2N1890S					0.9	V dc
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}$; $I_C = 10 \mu\text{A dc}$ pulsed (see 4.5.1).	h_{FE1}	20		
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}$; $I_C = 150 \text{ mA dc}$ pulsed (see 4.5.1).	h_{FE2}	100	300	
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}$; $I_C = 500 \text{ mA dc}$ pulsed (see 4.5.1).	h_{FE3}	50		
2N1711, 2N1711S						
<u>Subgroup 3</u>						
High temperature operation		$T_A = +150^\circ\text{C}$				
Collector to base cutoff current	3036	Bias condition D;	I_{CBO3}			
2N1711, 2N1711S 2N1890, 2N1890S		$V_{CB} = 60 \text{ V dc}$ $V_{CB} = 80 \text{ V dc}$			10 15	$\mu\text{A dc}$ $\mu\text{A dc}$
Low temperature operation		$T_A = -55^\circ\text{C}$				
Forward-current transfer ratio	3076	$V_{CE} = 10 \text{ V dc}$; $I_C = 10 \text{ mA dc}$, pulsed (see 4.5.1).	h_{FE4}	35		

See footnotes at end of table.

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* TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limit		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 4</u>						
Small-signal short-circuit forward current transfer ratio	3206	$V_{CE} = 5 \text{ V dc}; I_C = 1 \text{ mA dc}$ $f = 1 \text{ KHz}$	h_{fe}	80	200	
		$V_{CE} = 10 \text{ V dc}; I_C = 5 \text{ mA dc}$ $f = 1 \text{ KHz.}$	h_{fe}	90	270	
Magnitude of small-signal short-circuit forward current transfer ratio	3306	$V_{CE} = 10 \text{ V dc}; I_C = 50 \text{ mA dc};$ $f = 20 \text{ MHz}$	$ h_{fe} $	3.5	12	
* Small-signal short-circuit input impedance	3201	$V_{CB} = 10 \text{ V dc};$ $I_C = 5 \text{ mA dc } f = 1 \text{ kHz}$	h_{ib}	4	8	ohms
* Small-signal short-circuit input admittance	3216	$V_{CB} = 10 \text{ V dc};$ $I_C = 5 \text{ mA dc } f = 1 \text{ kHz}$	h_{ob}	0.0	1.0	μhos
				0.0	.3	μhos
* Small-signal open-circuit reverse voltage transfer ratio	3211	$V_{CB} = 10 \text{ V dc};$ $I_C = 5 \text{ mA dc } f = 1 \text{ kHz}$	h_{rb}		5×10^{-4}	μhos
					1.5×10^{-4}	μhos
Open circuit output capacitance		$V_{CB} = 10 \text{ V dc}; I_E = 0 \text{ mA dc}$ $100 \text{ kHz} \leq f \leq 1 \text{ MHz}$	C_{obo}	8	25	pF
				5	15	pF
Pulse response	3251	Test condition A, except test circuit and pulse requirements. See figure 6 herein.	$t_{on} + t_{off}$		30	ns
<u>Subgroup 5, 6, and 7</u>						
Not applicable						

1/ For sampling plan see MIL-PRF-19500.

2/ For resubmission of failed test in subgroup 1 of table I, double the sample size of the failed test or sequence of tests. A failure in table I, subgroup 1 shall not require retest of the entire subgroup. Only the failed test shall be rerun upon submission.

3/ Separate samples may be used.

4/ Not required for laser marked devices.

5/ This hermetic seal test is an end-point to temp-cycling in addition to electrical measurements.

6/ This test required for the following end-point measurement only:

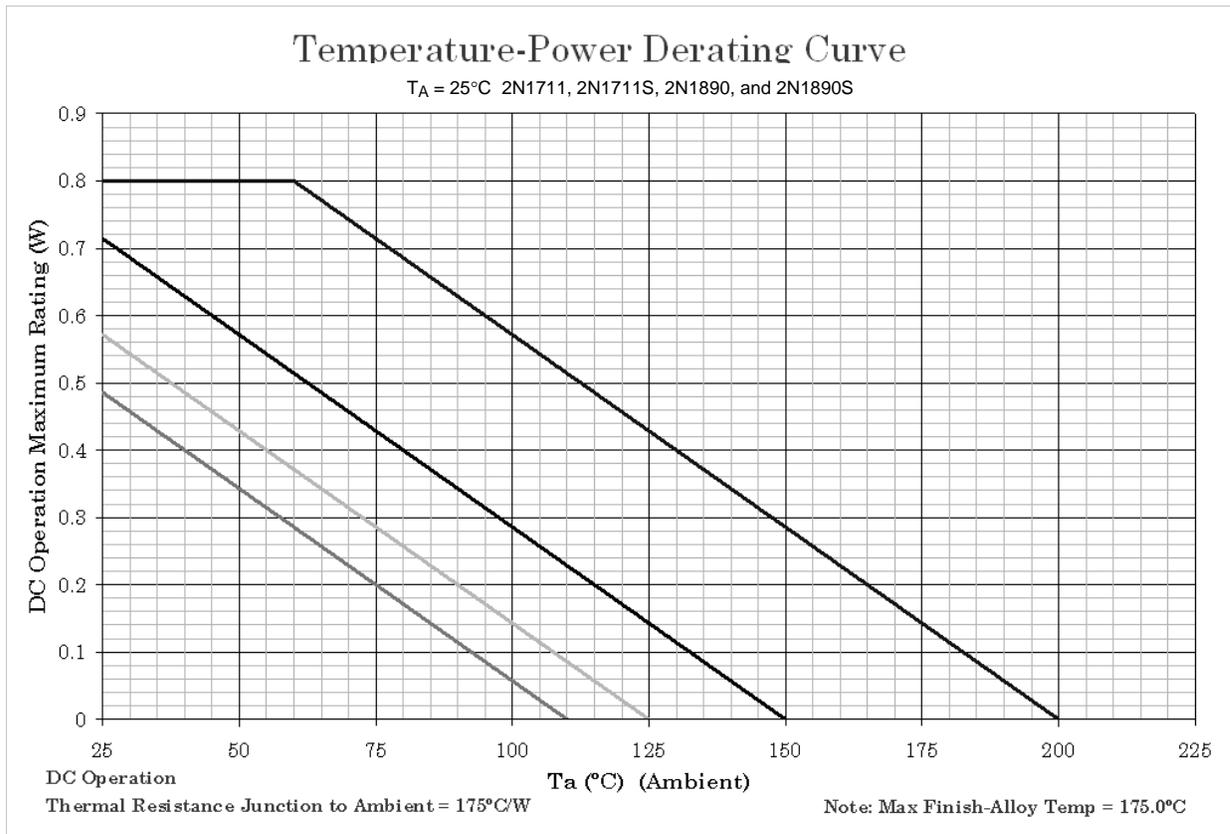
- * Group B, subgroups 3, 4, and 5 (JANTX and JANTXV).
- * Group B, step 1.
- * Group C, subgroups 2 and 6.
- * Group E, subgroups 1 and 2.

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* TABLE II. Group E inspection (all quality levels) - for qualification or re-qualification only.

Inspection	MIL-STD-750		Qualification
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling (air to air)	1051	Test condition C, 500 cycles	
Hermetic seal	1071		
Fine leak			
Gross leak			
Electrical measurements		See table I, subgroup 2 herein.	
<u>Subgroup 2</u>			45 devices c = 0
Intermittent life	1037	Intermittent operation life: $V_{CB} = 10$ V dc, 6,000 cycles Adjust device current, or power, to achieve a minimum ΔT_j of +100°C.	
Electrical measurements		See table I, subgroup 2 herein.	
<u>Subgroup 4</u>			
Thermal impedance curves		See table E-IX of MIL-PRF-19500, group E, subgroup 4.	
<u>Subgroup 5</u>			
Not applicable			
<u>Subgroup 6</u>			3 devices
Electrostatic discharge (ESD)	1020		
<u>Subgroup 8</u>			45 devices c = 0
Reverse stability	1033	Condition B.	

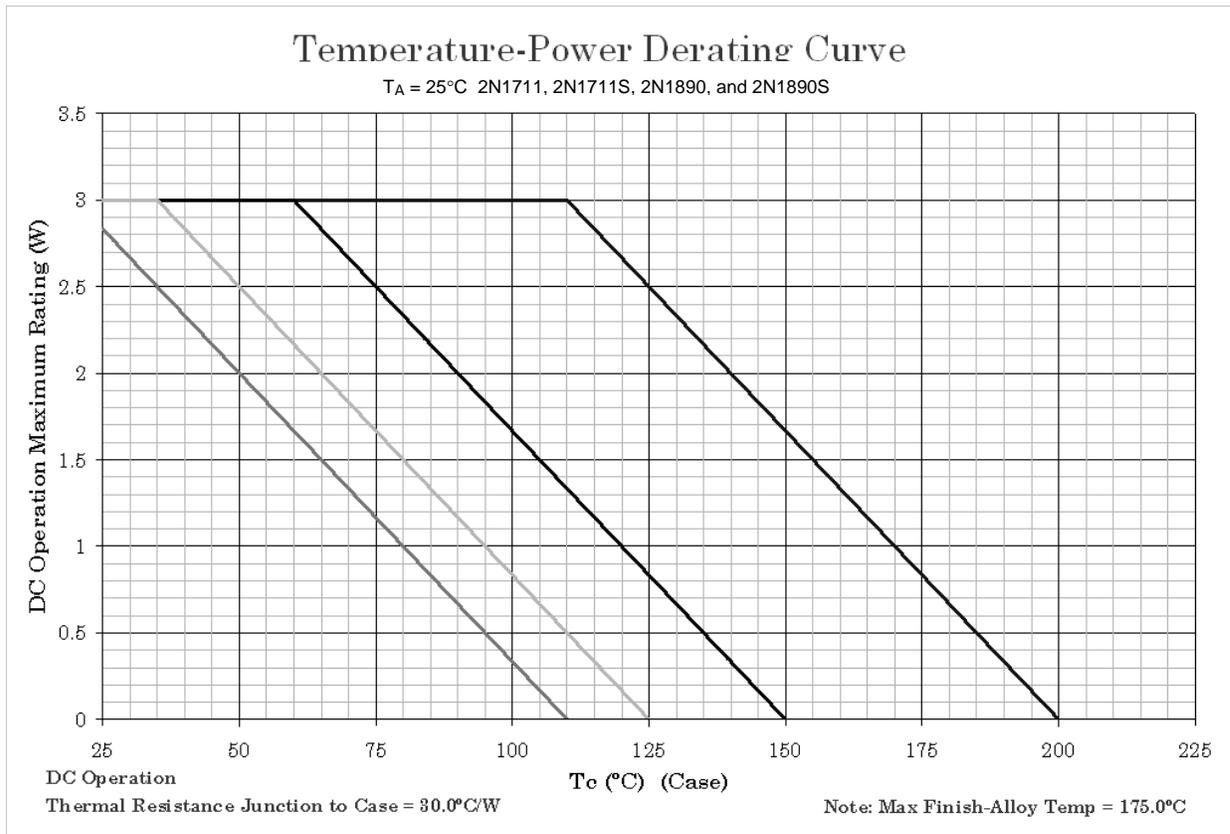
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NOTES:

1. This is the true inverse of the worst case thermal resistance value. All devices are capable of operating at $\leq T_J$ specified on this curve. Any parallel line to this curve will intersect the appropriate power for the desired maximum T_J allowed.
2. Derate design curve constrained by the maximum junction temperature ($T_J \leq 200^\circ\text{C}$) and power rating specified. (See 1.3 herein.)
3. Derate design curve chosen at $T_J \leq 150^\circ\text{C}$, where the maximum temperature of electrical test is performed.
4. Derate design curves chosen at $T_J \leq 125^\circ\text{C}$, and 110°C to show power rating where most users want to limit T_J in their application.

FIGURE 2. Temperature-power derating for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5).



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FIGURE 3. Temperature-power derating for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5).

Maximum Thermal Impedance

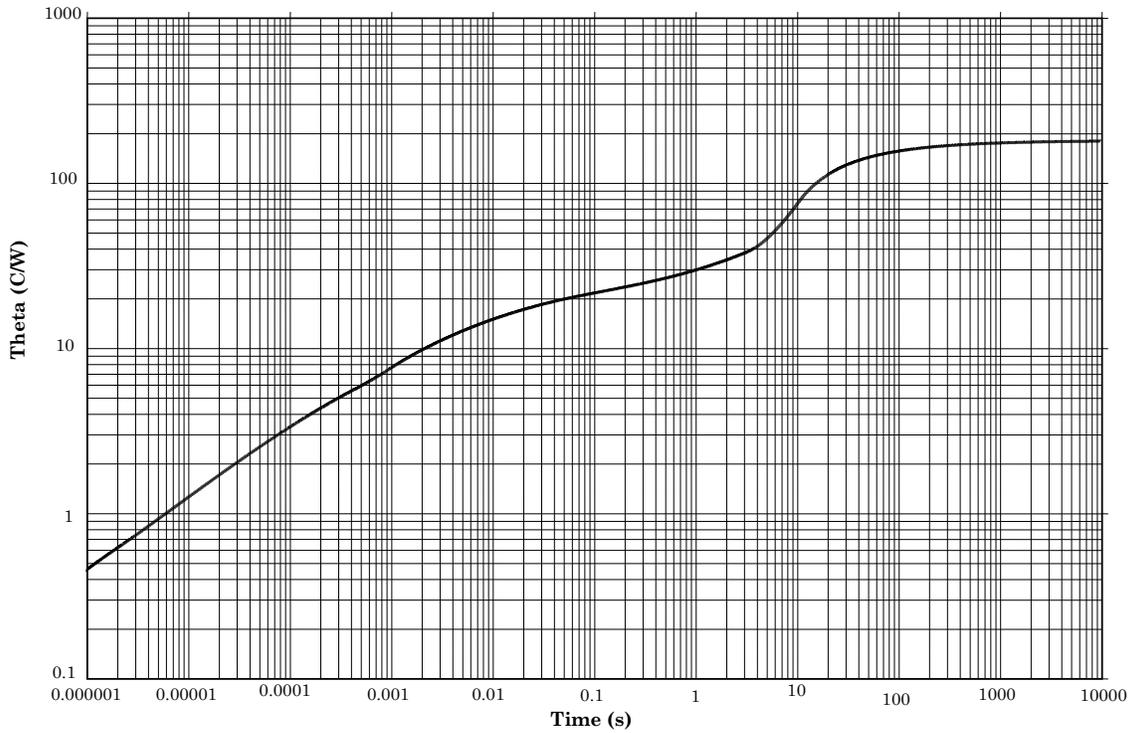


FIGURE 4. Thermal impedance graph ($R_{\theta JA}$) for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5).

Maximum Thermal Impedance

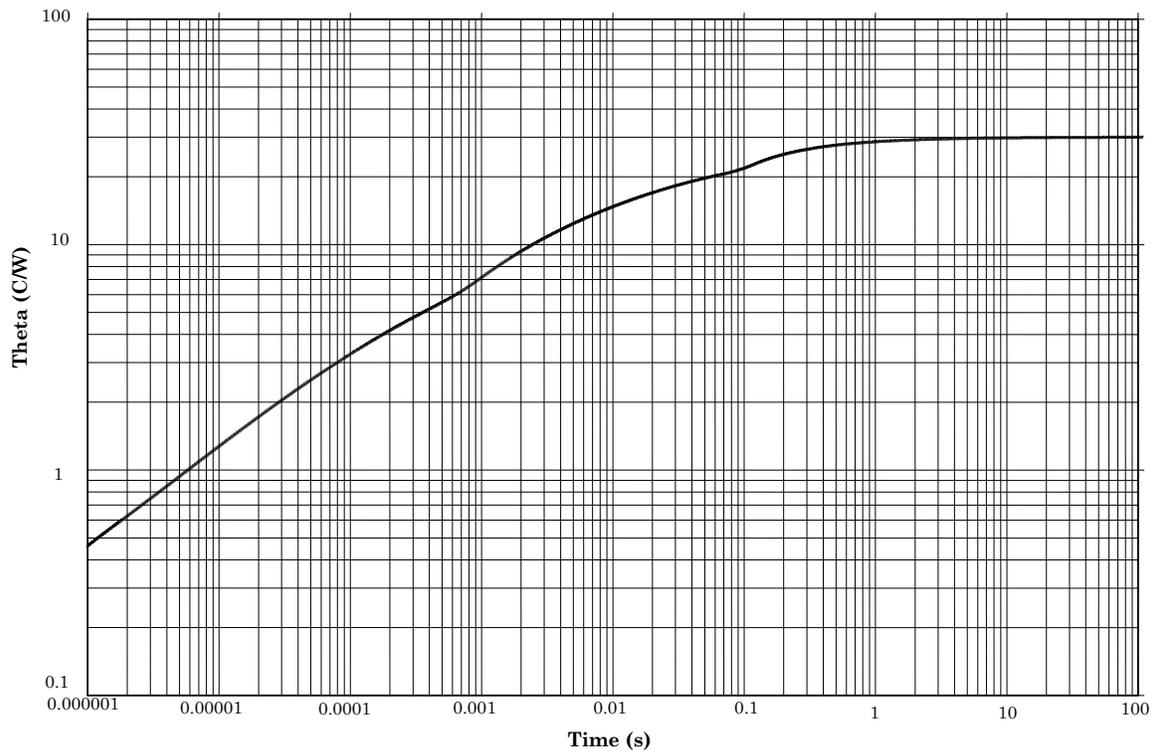
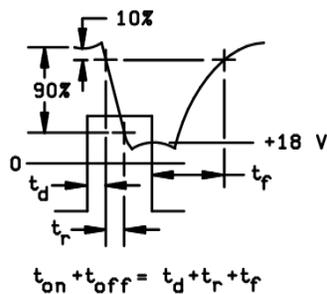
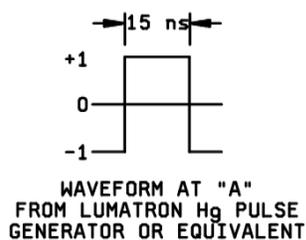
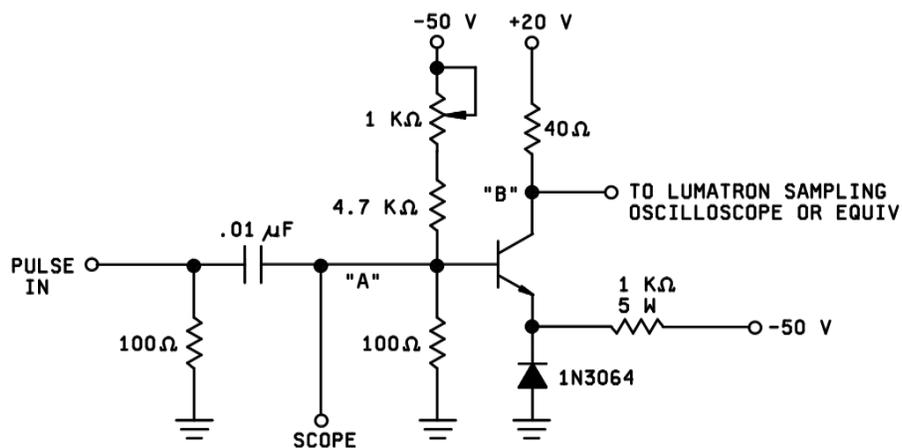


FIGURE 5. Thermal impedance graph ($R_{\theta JC}$) for 2N1711, 2N1711S, 2N1890, and 2N1890S (TO-5).



NOTES:

1. The rise time (T_r) of the applied pulse shall be $2.0 \leq ns$, duty cycle ≤ 2 percent, and the generator source impedance shall be 50Ω .
2. Sampling oscilloscope: $Z_{in} \geq 100 k\Omega$, $C_{in} \leq 12 pF$, rise time $\leq 2 ns$.

FIGURE 6. Pulse response (turn-on plus turn-off) measurement circuit and waveforms.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead finish (see 3.4.1).
- d. Product assurance level and type designator.

* 6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.daps.dla.mil>.

6.4 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

Custodians:

Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2010-053)

Review activities:

Army - AR, AV, MI, SM
Navy - AS, MC
Air Force - 19

* NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.daps.dla.mil>.