

INCH-POUND

MIL-M-38510/76C
7 October 2005
SUPERSEDING
MIL-M-38510/76B
4 December 1985

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR SCHOTTKY TTL, CASCADABLE,
SHIFT REGISTERS, MONOLITHIC SILICON

Inactive for new design after 23 August 1996.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF 38535

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic, silicon, Schottky TTL, shift register microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.4).

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>
01	4 bit cascadable bidirectional shift register
02	4 bit cascadable parallel-access shift register

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16		16 Dual-in-line
F	GDFP2-F16 or CDFP3-F16		16 Flat-pack

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, P. O. Box 3990, Columbus, OH 43218-3990, or emailed to bipolar@dsccl.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.2 V dc at -18 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) <u>1/</u>	
Device type 01	700 mW
Device type 02	700 mW
Lead temperature (soldering 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	
Cases E and F	(See MIL-STD-1835)
Junction temperature (T_J) <u>2/</u>	175°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL}) <u>3/</u>	0.8 V dc
Case operating temperature range (T_C)	-55°C to 125°C
Fan out	
Device type 01	
High logic level	20
Low logic level	10
Device type 02	
High logic level	20
Low logic level	10
Device type 01	
Width of clock input pulse	10 ns minimum
Width of clear input pulse	12 ns minimum
t_P (data)	8 ns minimum
Data input setup time	5 ns minimum
Hold time at any input	3 ns minimum
Mode control setup time	11 ns minimum
Device type 02	
Width of clock input pulse	10 ns minimum
Width of clear input pulse	12 ns minimum
t_P (data)	8 ns minimum
Shift load input setup time	11 ns minimum
Data input setup time	5 ns minimum
Clear input setup time	9 ns minimum
Shift load release time	6 ns minimum
Data hold time	3 ns minimum

1/ Must withstand the added P_D due to short circuit condition (e.g. I_{OS}).2/ Maximum junction temperature should not be exceeded except in accordance with allowable short duration burn-in screening condition in accordance with MIL-PRF-38535.3/ $V_{IL} = 0.7$ V at +125°C.

2.0 APPLICABLE DOCUMENT

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications and standards. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.3).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Case outlines. Case outlines shall be as specified in 1.2.3.

3.3.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.3 Truth tables and timing diagrams. The truth tables and timing diagrams shall be as specified on figure 2.

3.3.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.3.5 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.4 Lead material and finish. Lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table 1 and apply over the full recommended case operating temperature range, unless otherwise specified.

3.6 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 12 (see MIL-PRF-38535, appendix A).

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

4.3 Screening. Screening shall be in accordance with MIL-PRF-38535 and shall be conducted on all devices prior to qualification and conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Device type	Limits		Units
				Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, V _{IH} = 2.0 V, V _{IL} = 0.8 V, I _{OH} = -1 mA	01, 02	2.5		V
		T _C = +125°C, V _{IL} = 0.7 V	02			
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, V _{IH} = 2.0 V, V _{IL} = 0.8 V, I _{OL} = 20 mA	01, 02		0.5	V
		T _C = +125°C, V _{IL} = 0.7 V	01, 02		0.45	
Input clamp voltage	V _{IC}	V _{CC} = 4.5 V, I _{IN} = -18 mA, T _C = 25°C	01, 02		-1.2	V
High level input current, all inputs	I _{IH1}	V _{CC} = 5.5 V, V _{IN} = 2.7 V	01, 02		50	μA
High level input current, all inputs	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 5.5 V	01, 02		1	mA
Low level input current, all inputs	I _{IL}	V _{CC} = 5.5 V, V _{IN} = 0.5 V	01, 02	-0.5	-2	mA
Short-circuit output current	I _{OS}	V _{CC} = 5.5 V ^{1/}	01, 02	-40	-100	mA
Supply current	I _{CC}	V _{CC} = 5.5 V ^{2/}	01, 02		130	mA
Collector cut-off current	I _{CEX}	V _{CC} = 5.5 V, V _{IH} = 5.5 V, V _{OH} = 5.5 V	01, 02		250	μA
Maximum clock frequency	f _{MAX}	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 280Ω (See figure 4)	01	70		MHz
Propagation delay time, high-to-low level output from clear	t _{PHL1}			4	28	ns
Propagation delay time, low-to-high level output from clock	t _{PLH2}			4	19	ns
Propagation delay time, high-to-low level output from clock	t _{PHL2}			4	25	ns
Maximum clock frequency	f _{MAX}	V _{CC} = 5.0 V, C _L = 50 pF, R _L = 280Ω (See figure 5)	02	70		MHz
Propagation delay time, high-to-low level output from clear	t _{PHL1}			4	28	ns
Propagation delay time, low-to-high level output from clock	t _{PLH2}			4	19	ns
Propagation delay time, high-to-low level output from clock	t _{PHL2}			4	25	ns

^{1/} Not more than one output should be shorted at a time.

^{2/} Device type:

01 - With all outputs open, inputs A thru D grounded, 5.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested by applying clock pulse.

02 - With the outputs open, clear at 4.5 V, shift load, J, \bar{K} , and data inputs grounded, I_{CC} is measured by applying clock pulse.

TABLE II. Electrical test requirements.

MIL-PRF-38535 Test requirement	Subgroups (see table III)	
	Class S Devices	Class B Devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 7, 9, 10, 11	1*, 2, 3, 7, 9
Group A test requirements	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 9, 10, 11
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3, 7, 8, 9, 10, 11	N/A
Groups C end point electrical parameters	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3
Group D end point electrical parameters	1, 2, 3	1, 2, 3

*PDA applies to subgroup 1.

4.4 Technology Conformance Inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroups 4, 5, and 6, shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

Terminal number	Terminal name	
	Device type 01	Device type 02
	Cases E and F	Cases E and F
1	Clear	Clear
2	Shift Right	J
3	Input A	\bar{K}
4	Input B	Input A
5	Input C	Input B
6	Input D	Input C
7	Shift Left	Input D
8	GND	GND
9	S0	Shift/Load
10	S1	Clock
11	Clock	Output \bar{Q}_D
12	Output Q_D	Output Q_D
13	Output Q_C	Output Q_C
14	Output Q_B	Output Q_B
15	Output Q_A	Output Q_A
16	V_{CC}	V_{CC}

Figure 1. Terminal connections.

Device type 01

The register has four modes of operation:

- Parallel (broadside) load
- Shift right (in the direction Q_A toward Q_D)
- Shift left (in the direction Q_D toward Q_A)
- Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S_0 and S_1 , high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift left serial input. Clocking of the flip-flop is inhibited when both mode control inputs are low.

INPUTS										OUTPUTS			
CLEAR	MODE		CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D
	S_1	S_0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d, = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most recent ↑ transition of the clock.

Figure 2. Truth tables and timing diagrams.

DEVICE TYPE 01

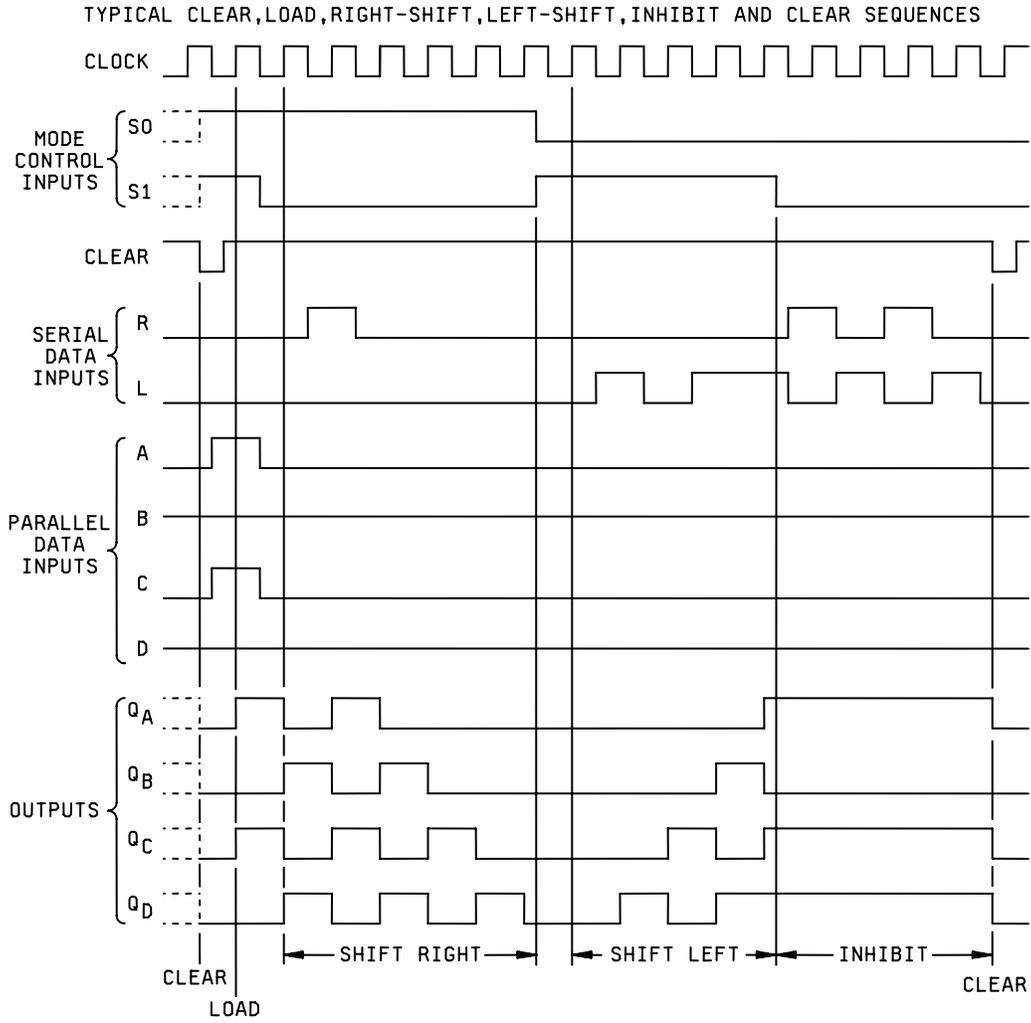


Figure 2. Truth tables and timing diagrams - Continued.

Device type 02

The register has two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D, or T-type flip-flop as shown in the truth table.

			INPUTS						OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	\overline{Q}_D
			J	\overline{K}	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	\overline{d}
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\overline{Q}_{D0}
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\overline{Q}_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	\overline{Q}_{Cn}
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	\overline{Q}_{Cn}
H	H	↑	H	L	X	X	X	X	\overline{Q}_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\overline{Q}_{Cn}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d, = the level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} = the level of Q_A , Q_B , or Q_C , respectively, before the most recent transition of the clock.

Figure 2. Truth tables and timing diagrams - Continued.

DEVICE TYPE 02

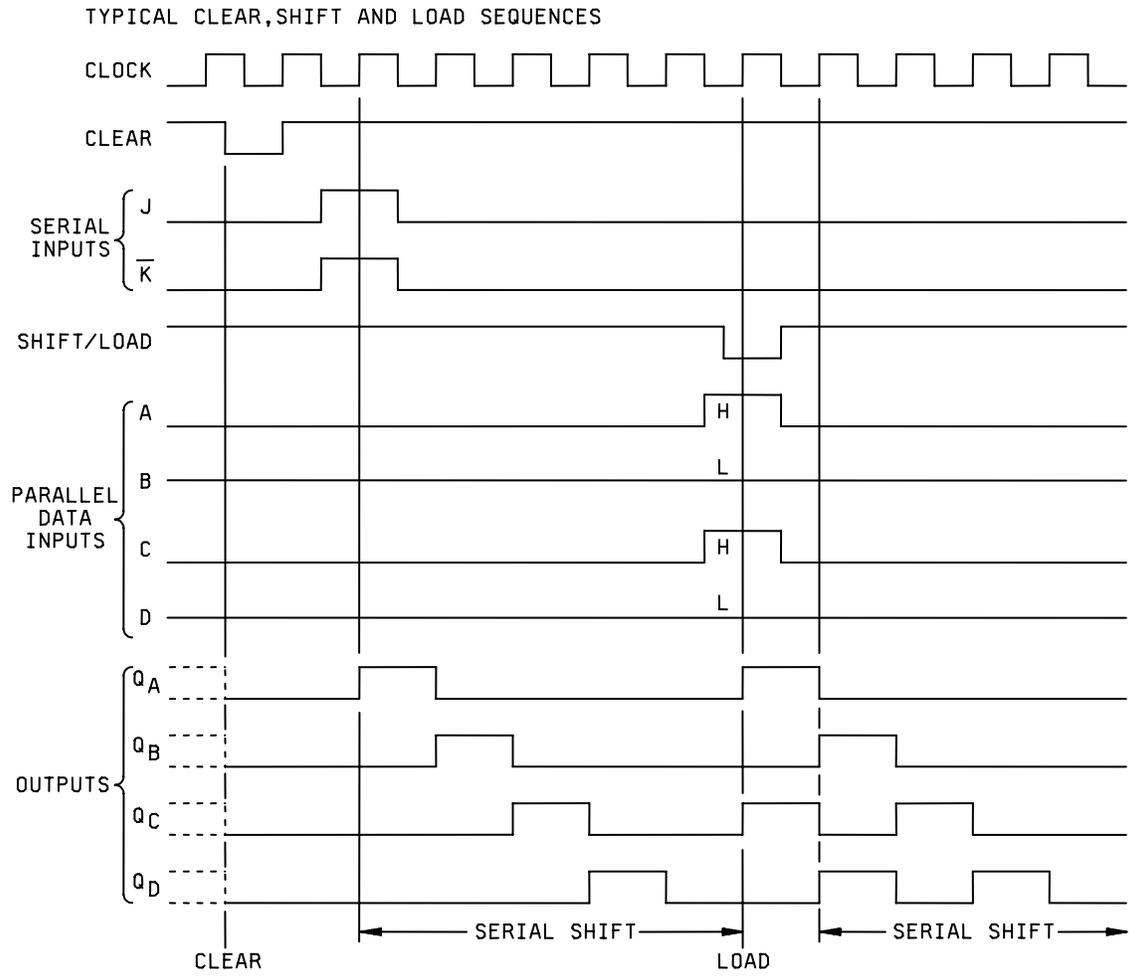


Figure 2. Truth tables and timing diagrams - Continued.

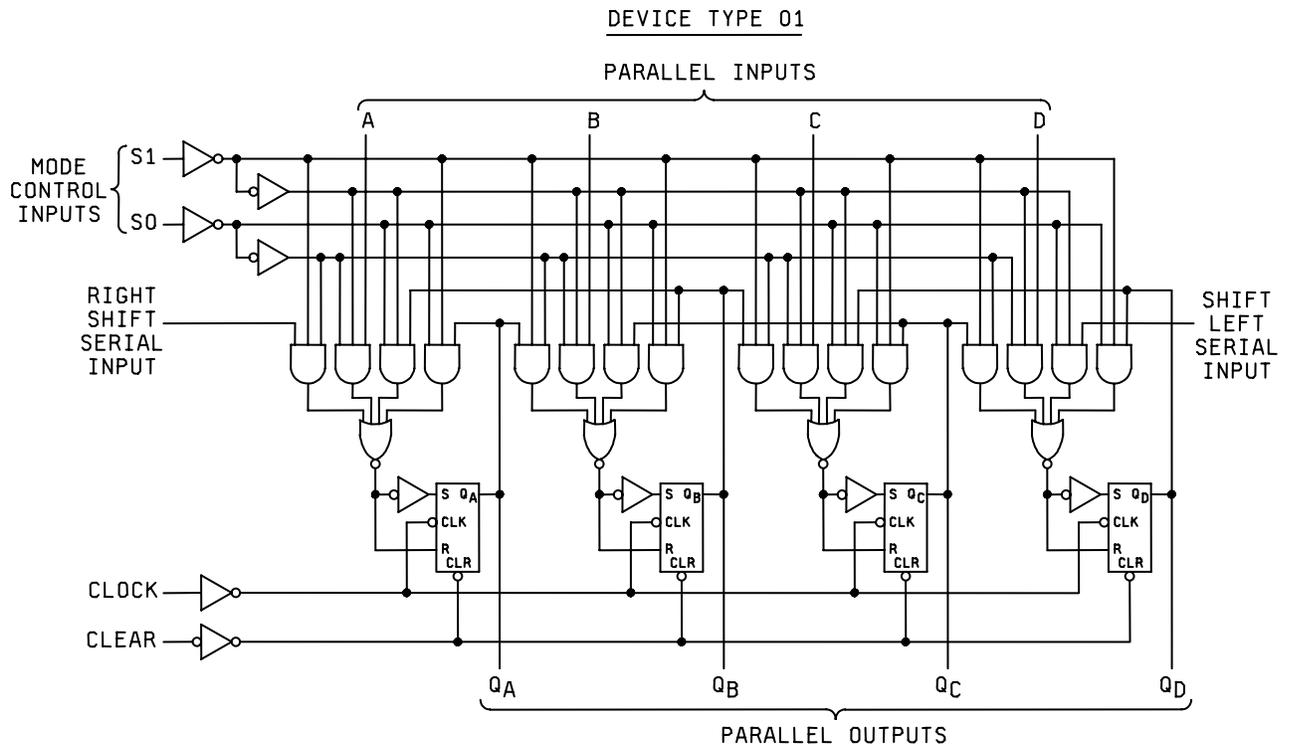


Figure 3. Logic diagrams.

DEVICE TYPE 02

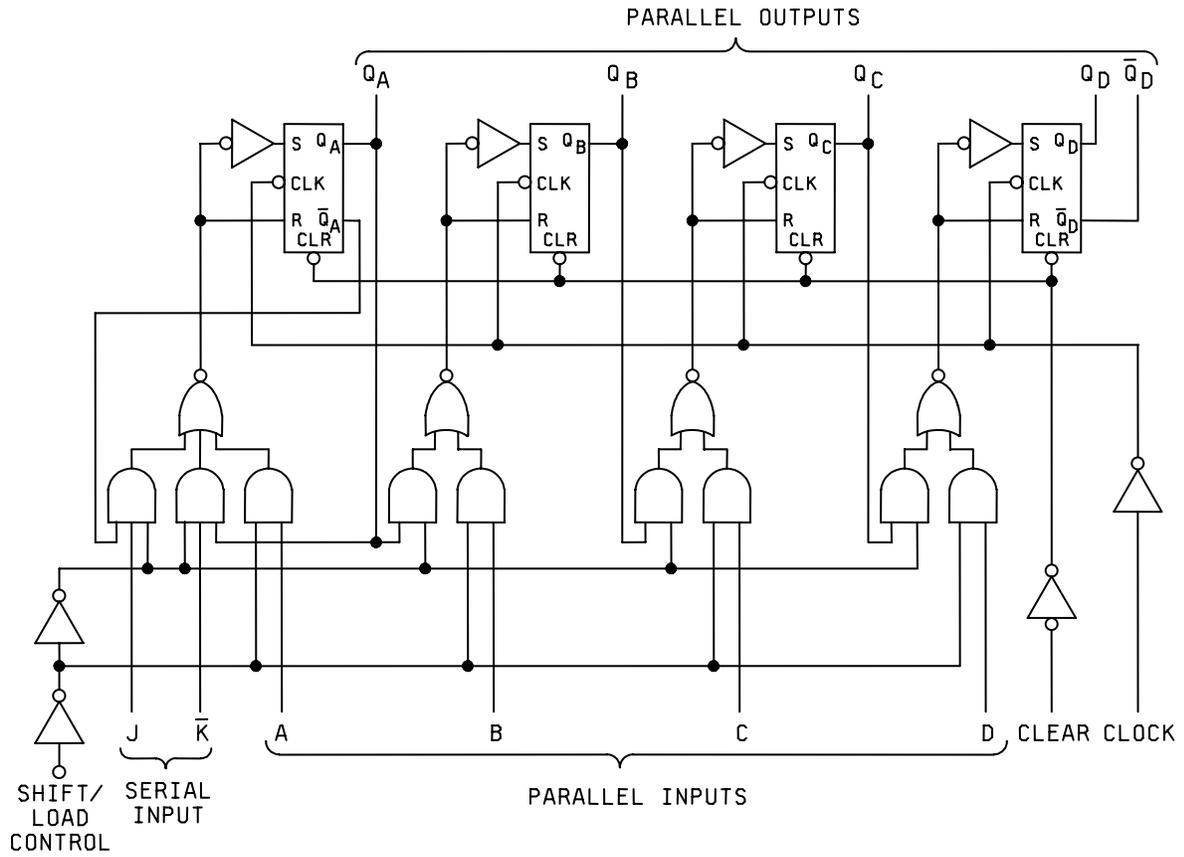
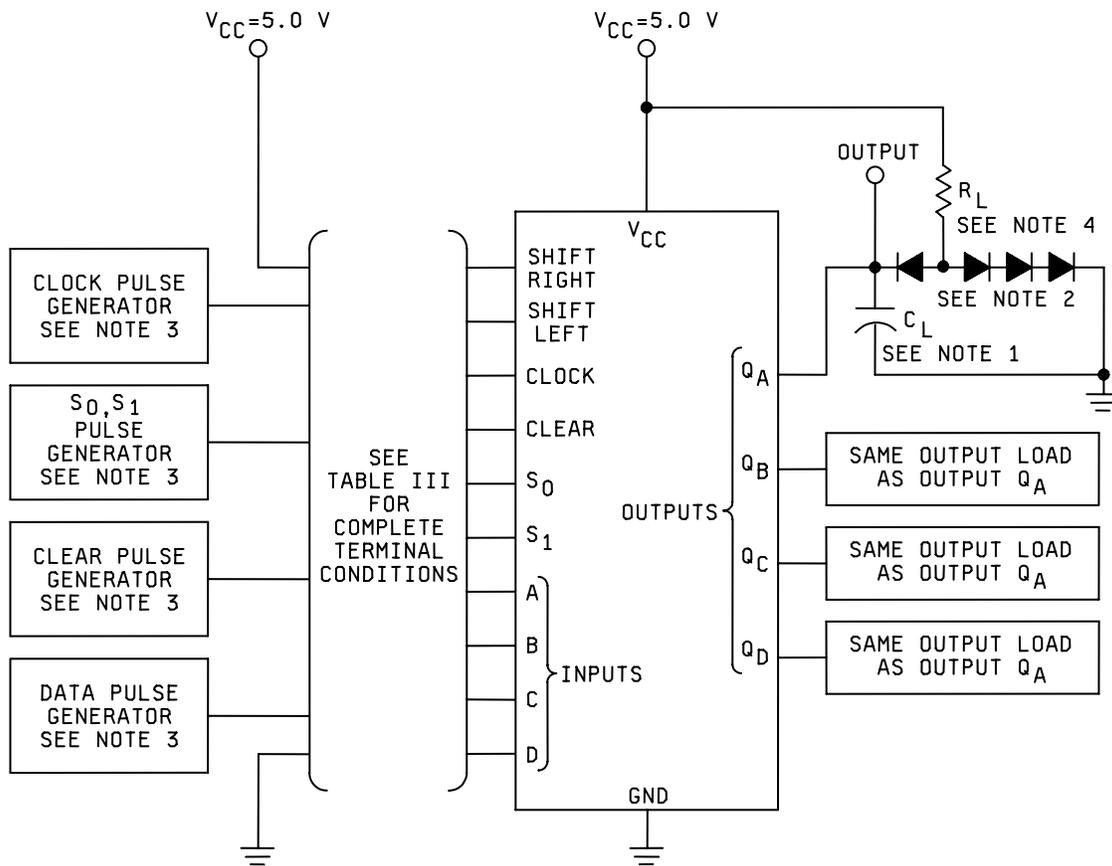


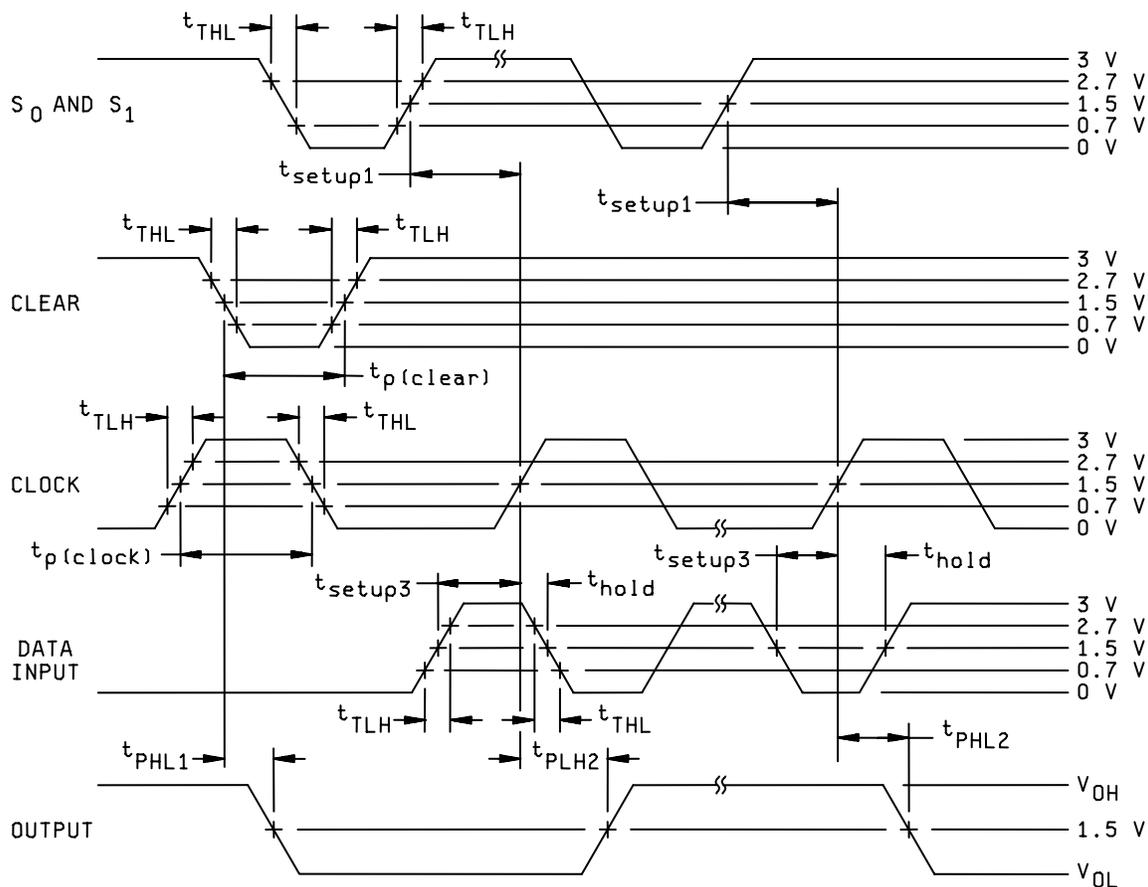
Figure 3. Logic diagrams - Continued.



NOTES:

1. $C_L = 50 \text{ pF} \pm 10\%$, including scope probe, wiring, and stray capacitance without package in test fixture.
2. All diodes are 1N3064, or equivalent.
3. Unless otherwise specified in the notes associated with the individual tests, all pulse generators have the following characteristics: $Z_{OUT} \cong 50 \Omega$, $t_{TLH} \leq 2.5 \text{ ns}$.
4. $R_L = 280 \Omega \pm 5\%$.

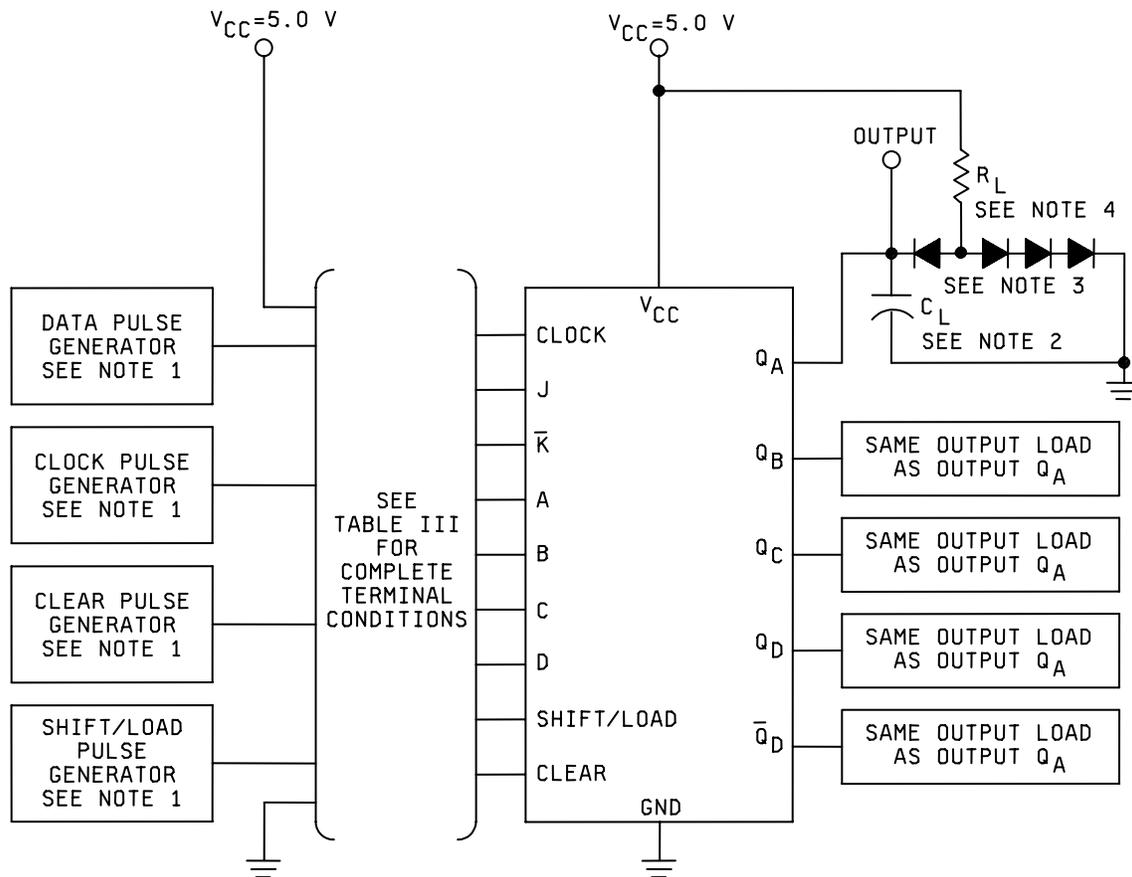
Figure 4. Switching time test circuit and waveforms for device types 01.



NOTES:

1. S₀ and S₁, $t_{setup} = 11$ ns.
2. The clear pulse has the following characteristics: $t_p(\text{clear}) = 12$ ns, and $PRR \leq 1$ MHz.
3. The data pulse has the following characteristics: $t_p(\text{data}) = 8$ ns, $t_{setup} = 5$ ns, $t_{hold} = 3$ ns and $PRR \leq 1$ MHz.
4. The clock pulse has the following characteristics: $t_p(\text{clock}) = 10$ ns, and $PRR \leq 1$ MHz for t_{PHL1} measurement and 2 MHz for t_{PLH2} and t_{PHL2} measurements.
5. For each clock to output t_{PLH2} and t_{PHL2} measurement the clear input is momentarily grounded then raised to and held at 3 V minimum.
6. For f_{MAX} measurement at -55°C and 125°C the clock input $PRR \leq 56$ MHz and the shift right input $PRR \leq 28$ MHz; at 25°C the clock input $PRR \leq 70$ MHz and the shift right input $PRR \leq 35$ MHz.
7. Load circuits or a given output are only required where the specific test given in table III indicated OUT on that output. Load circuits may otherwise be omitted.

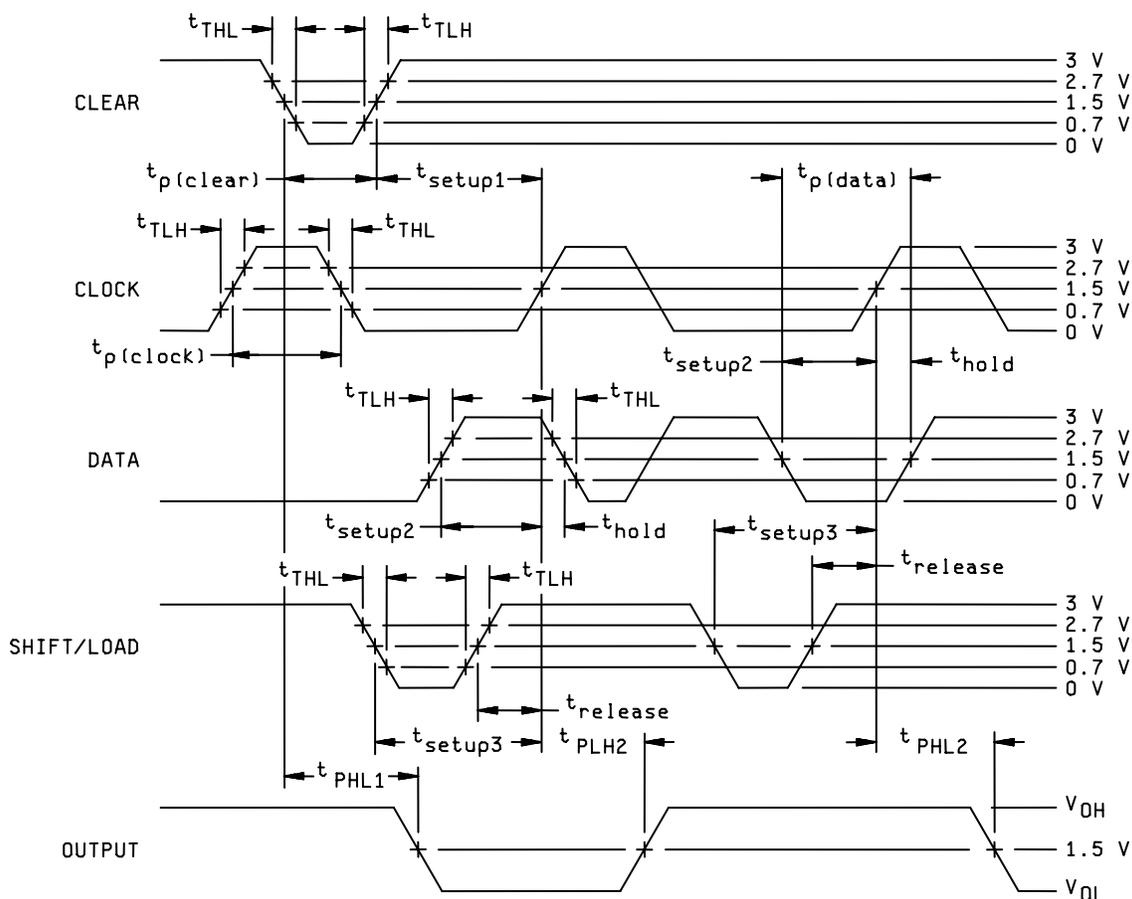
Figure 4. Switching time test circuit and waveforms for device types O1 - Continued.



NOTES:

1. Unless otherwise specified in the notes with the individual waveforms, all pulse generators shall have the following characteristics: $t_{TLH} \leq 2.5 \text{ ns}$, $t_{THL} \leq 2.5 \text{ ns}$, $Z_{OUT} \approx 50 \Omega$.
2. $C_L = 50 \text{ pF} \pm 10\%$, including scope probe, wiring, and stray capacitance without package in test fixture.
3. All diodes are 1N3064, or equivalent.
4. $R_L = 280 \Omega \pm 5\%$.
5. Load circuit on a given output are only required where the specific test given in table III indicates "OUT" on the output.

Figure 4. Switching time test circuit and waveforms for device types 02.



NOTES:

1. The shift/load pulse has the following characteristics: $t_p(\text{shift/load}) = 5$ ns minimum, $t_{\text{setup}} = 11$ ns, $t_{\text{release}} = 6$ ns maximum and $\text{PRR} \leq 2$ MHz.
2. The clear pulse has the following characteristics: $t_p(\text{clear}) = 12$ ns, $t_{\text{setup}} = 9$ ns, and $\text{PRR} \leq 1$ MHz.
3. The data pulse has the following characteristics: $t_p(\text{data}) = 8$ ns, $t_{\text{setup}} = 5$ ns, $t_{\text{hold}} = 3$ ns and $\text{PRR} \leq 1$ MHz.
4. The clock pulse has the following characteristics: $t_p(\text{clock}) = 10$ ns, and $\text{PRR} \leq 1$ MHz for t_{PHL1} measurement and 2 MHz for t_{PLH2} and t_{PHL2} measurements.
5. For each clock to output t_{PLH2} and t_{PHL2} measurement the clear input is momentarily grounded then raised to and held at 3 V minimum.
6. For f_{MAX} measurement at -55°C and 125°C the clock input $\text{PRR} \leq 56$ MHz; at 25°C the clock input $\text{PRR} \leq 70$ MHz.

Figure 4. Switching time test circuit and waveforms for device types 01 - Continued.

TABLE III. Group A inspection for device type 01.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit		
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S0	S1	Clock	QD	QC	QB	QA	V _{CC}		Min	Max			
1 T _c = 25°C	V _{OH}	3006	1	2.0 V		2.0 V	2.0 V	2.0 V	2.0 V		GND	2.0 V	2.0 V	1/			-1 mA	-1 mA	-1 mA	4.5 V	QA	2.5		V	
		"	2	"		"	"	"	"		"	"	"	"						"	QB	"		"	
		"	3	"		"		"	"	"		"	"	"	"						"	QC	"		"
		"	4	"		"		"	"	"		"	"	"	"	-1 mA					"	QD	"		"
	V _{OL}	3007	5	"		0.8 V	0.8 V	0.8 V	0.8 V			"	"	"	"			20 mA	20 mA	20 mA	"	QA		0.5	"
		"	6	"		"	"	"	"		"	"	"	"	"						"	QB	"		"
		"	7	"		"		"	"		"	"	"	"	"						"	QC	"		"
		"	8	"		"		"	"		"	"	"	"	"	20 mA					"	QD	"		"
	V _{IC}		9	-18 mA	-18 mA							"									"	Clear		-1.2	"
			10			-18 mA						"									"	Shift R			"
			11				-18 mA					"									"	Input A			"
			12					-18 mA				"									"	Input B			"
			13						-18 mA			"									"	Input C			"
			14							-18 mA		"									"	Input D			"
			15								-18 mA										"	Shift L			"
			16									-18 mA									"	S0			"
			17										-18 mA								"	S1			"
			18											-18 mA							"	Clock			"
I _{IL}	3009	19	0.5 V	0.5 V							"		GND						5.5 V	Clear	2/	2/	mA		
	"	20			0.5 V						"		5.5 V	5.5 V					"	Shift R	"	"	"		
	"	21				0.5 V					"		"	"					"	Input A	"	"	"		
	"	22					0.5 V				"		"	"					"	Input B	"	"	"		
	"	23						0.5 V			"		"	"					"	Input C	"	"	"		
	"	24							0.5 V		"		"	"					"	Input D	"	"	"		
	"	25								0.5 V			"	"					"	Shift L	"	"	"		
	"	26									0.5 V		"	"					"	S0	"	"	"		
	"	27										0.5 V		"					"	S1	"	"	"		
	"	28		5.5 V									0.5 V		0.5 V					"	Clock	"	"	"	
I _{IH1}	3010	29	2.7 V	2.7 V							"								"	Clear		50	μA		
	"	30		2.7 V							"		5.5 V	GND					"	Shift R		"	"		
	"	31			2.7 V						"		GND	"					"	Input A		"	"		
	"	32				2.7 V					"		"	"					"	Input B		"	"		
	"	33					2.7 V				"		"	"					"	Input C		"	"		
	"	34						2.7 V			"		"	"					"	Input D		"	"		
	"	35							2.7 V		"		"	"					"	Shift L		"	"		
	"	36								2.7 V			"	"					"	S0		"	"		
	"	37									2.7 V		"	"					"	S1		"	"		
	"	38										2.7 V		2.7 V					"	Clock		"	"		
I _{IH2}	"	39	5.5 V	5.5 V							"								"	Clear		1.0	mA		
	"	40			5.5 V						"		5.5 V	GND					"	Shift R		"	"		
	"	41				5.5 V					"		"	"					"	Input A		"	"		
	"	42					5.5 V				"		"	"					"	Input B		"	"		
	"	43						5.5 V			"		"	"					"	Input C		"	"		
	"	44							5.5 V		"		"	"					"	Input D		"	"		
	"	45								5.5 V			"	"					"	Shift L		"	"		
	"	46									5.5 V		"	"					"	S0		"	"		
	"	47										5.5 V		"					"	S1		"	"		
	"	48											5.5 V		5.5 V				"	Clock		"	"		

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 – Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit	
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S0	S1	Clock	QD	QC	QB	QA	V _{CC}		Min	Max		
1 T _C = 25°C	I _{OS}	3011	49	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V		GND	5.5 V	5.5 V	1/			GND	GND	5.5 V	QA	-40	-100	mA	
		"	50	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	QB	"	"	"	
		"	51	"		"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	QC	"	"	"
		"	52	"		"	"	"	"	"	"	"	"	"	"	GND	"	"	"	"	QD	"	"	"
	I _{CC}	3005	53	5.5 V	5.5 V	GND	GND	GND	GND	5.5 V	"	5.5 V	5.5 V	1/					"	V _{CC}		130	mA	
I _{CEX}	"	54	5.5 V		5.5 V	5.5 V	5.5 V	5.5 V		"	5.5 V	5.5 V	1/					"	QA		250	μA		
	"	55	"		"	"	"	"	"	"	"	"	"	"		5.5 V	5.5 V	5.5 V	QB		"	"		
	"	56	"		"	"	"	"	"	"	"	"	"	"		"	"	"	QC		"	"		
	"	57	"		"	"	"	"	"	"	"	"	"	"	5.5 V	"	"	"	QD		"	"		
2	Same tests, terminal conditions, and limits as subgroup 1, except T _C = 125°C, V _{IC} tests are omitted, V _{IL} = 0.7 V and V _{OL} (max) = 0.45 V.																							
3	Same tests, terminal conditions, and limits as subgroup 1, except T _C = -55°C, V _{IC} tests are omitted.																							
7 3/ T _C = 25°C	Truth table test	3014	58	B	B	A	B	A	B	B	GND	A	A	A	L	L	L	L	5.0 V					
		"	59	A	"	"	"	"	"	"	"	"	"	"	A	"	L	L	L	"				
		"	60	"	"	"	"	"	"	"	"	"	"	"	B	"	L	L	L	"				
		"	61	"	"	"	"	"	"	"	"	"	"	"	A	"	H	"	H	"				
		"	62	"	"	"	B	A	B	A	"	"	"	"	A	"	H	"	H	"				
		"	63	"	"	"	"	"	"	"	"	"	"	"	B	"	H	"	H	"				
		"	64	"	"	"	"	"	"	"	"	"	"	"	A	H	L	H	L	"				
		"	65	"	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"				
		"	66	"	"	"	A	B	A	B	"	"	"	B	B	"	"	"	"	"				
		"	67	"	"	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"				
		"	68	"	"	"	"	"	"	"	"	"	"	"	A	"	"	"	"	"				
		"	69	"	"	"	"	"	"	"	"	"	"	"	"	"	L	"	L	"				
		"	70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	73	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	75	"	"	"	A	B	B	B	"	"	"	A	"	"	"	"	"	"				
		"	76	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	77	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	78	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"			4/	
		"	79	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
		"	81	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"				
"	82	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"						
"	83	"	"	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"						
"	84	"	"	"	B	"	"	"	"	"	"	"	"	"	"	H	L	L	"					
"	85	"	"	"	B	"	"	"	"	"	"	"	"	"	"	H	L	L	"					
"	86	"	"	"	B	"	"	"	"	"	"	"	"	"	"	H	L	L	"					
"	87	"	"	"	A	"	"	"	"	"	"	"	"	"	"	H	L	L	"					
"	88	"	"	"	A	"	"	"	"	"	"	"	"	"	"	H	L	L	"					
"	89	"	"	"	A	"	"	"	"	"	"	"	"	"	"	L	H	L	"					
"	90	"	"	"	B	"	"	"	"	"	"	"	"	"	"	L	H	L	"					
"	91	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B	L	H	"					
"	92	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A	H	L	"					
"	93	"	"	"	"	"	"	"	"	"	"	"	"	"	"	B	H	L	"					
"	94	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A	L	H	"					

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 – Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit					
				Test no.	Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S0	S1	Clock	QD	QC	QB	QA		V _{CC}	Min		Max				
7 $\frac{3}{/}$ T _c = 25°C	Truth table test	3014	95	A	B	B	B	B	B	B	GND	A	B	B	L	H	L	L	L	5.0 V								
			96	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	
			97	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			98	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			99	"	"	"	"	"	"	"	"	"	"	B	A	A	"	"	"	"				"	"	"	"	"
			100	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			101	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			102	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			103	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			104	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			105	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			106	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			107	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			108	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			109	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			110	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			111	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			112	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			113	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			114	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			115	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			116	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			117	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
			118	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"	"	"	"	"
119	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"						
120	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"						
121	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"						
122	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"						
123	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"						
124	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"						
8	Repeat subgroup 7 at T _c = 125°C and T _c = -55°C.																											
9 T _c = 25°C	f _{MAX}	$\frac{5}{/}$	125	$\frac{6}{/}$	IN	GND	GND	GND	GND	GND	GND	5.0 V	GND	IN	OUT				5.0 V	QD	35		MHz					
	t _{PHL1}	3003	126	IN		5.0 V	5.0 V	5.0 V	5.0 V		"	5.0 V	5.0 V	IN		OUT	OUT	OUT	"	Clear/QA	4	21	ns					
		"	127	"		"	"	"	"	"	"	"	"	"	"		OUT	OUT	"	Clear/QB	"	"	"					
		"	128	"		"	"	"	"	"	"	"	"	"	"		OUT	OUT	"	Clear/QC	"	"	"					
		"	129	"		"	"	"	"	"	"	"	"	"	"		OUT	OUT	"	Clear/QD	"	"	"					
	t _{PLH2}	"	130	$\frac{6}{/}$		IN		IN			"	$\frac{7}{/}$	$\frac{7}{/}$	"			OUT	OUT	"	Clock/QA	"	15	"					
		"	131	"		"		IN			"	"	"	"			OUT	OUT	"	Clock/QB	"	"	"					
	"	132	"		"			IN		"	"	"	"			OUT	OUT	"	Clock/QC	"	"	"						
	"	133	"		"				IN	"	"	"	"			OUT	OUT	"	Clock/QD	"	"	"						
t _{PHL2}	"	134	$\frac{7}{/}$		IN		IN			"	"	"	"				OUT	OUT	"	Clock/QA	"	19	"					
	"	135	"		"		IN			"	"	"	"				OUT	OUT	"	Clock/QB	"	"	"					
	"	136	"		"			IN		"	"	"	"				OUT	OUT	"	Clock/QC	"	"	"					
	"	137	"		"				IN	"	"	"	"				OUT	OUT	"	Clock/QD	"	"	"					

See notes at end of device type 01.

TABLE III. Group A inspection for device type 01 – Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit	
				Clear	Shift right	Input A	Input B	Input C	Input D	Shift left	GND	S0	S1	Clock	QD	QC	QB	QA	V _{CC}		Min	Max		
10 T _C =125°C	f _{MAX}	5/	138	6/	IN	GND	GND	GND	GND	GND	GND	5.0 V	GND	IN	OUT				5.0 V	QD	28.0		MHz	
	t _{PHL1}	3003 5/	139	IN		5.0 V	5.0 V	5.0 V	5.0 V				5.0 V	5.0 V	IN						Clear/QA	4	28	ns
			140	"		"	"	"	"				"	"	"						Clear/QB	"	"	"
			141	"		"	"	"	"				"	"	"			OUT			Clear/QC	"	"	"
			142	"		"	"	"	"				"	"	"			OUT			Clear/QD	"	"	"
	t _{PLH2}	"	143	6/		IN						"	7/	7/	"						Clock/QA	"	19	"
			144	"			IN					"	"	"	"						Clock/QB	"	"	"
			145	"				IN				"	"	"	"						Clock/QC	"	"	"
			146	"					IN			"	"	"	"			OUT			Clock/QD	"	"	"
	t _{PHL2}	"	147	7/		IN						"	"	"	"						Clock/QA	"	25	"
			148	"			IN					"	"	"	"						Clock/QB	"	"	"
			149	"				IN				"	"	"	"						Clock/QC	"	"	"
150			"					IN			"	"	"	"			OUT			Clock/QD	"	"	"	
11	Same tests, terminal conditions, and limits as subgroup 10, except T _C = -55°C.																							

NOTES:

- 1/ Input is a single clock pulse.
- 2/ I_{IL} = limits shall be as follows:

Measured terminal	min/max limits (mA) for circuit			
	A	B	C	D
Clear, S0, S1	-0.7/-1.3	-1/-2	-1/-2	-1/-2
Shift R, Shift L, A, B, C, D, Clock	-1/-2	-1/-2	-1/-2	-1/-2

- 3/ A = terminal connected to 2.0 V minimum. B = terminal connected to 0.8 V maximum.
- 4/ Tests shall be performed in the sequence specified. Output voltages shall be either high "H" or "L" as indicated in the terminal conditions columns. Output voltage test limits over the specified temperature range shall be either: (1) H = 2.5 V minimum and L = 0.5 V maximum when using a high speed checker double comparator, or (2) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
- 5/ See figure 4 herein for switching test circuit and waveforms.
- 6/ The clear input is momentarily grounded, then raised to and held at 3.0 V minimum/5.5 V maximum.
- 7/ 3.0 V minimum, 5.0 V maximum.

TABLE III. Group A inspection for device type 02.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E, F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				Test no.	Clear	J	\bar{K}	Input A	Input B	Input C	Input D	GND	Shift/load	Clock	\bar{Q} D	QD	QC	QB	QA		V _{CC}	Min		Max		
1 T _c = 25°C	V _{OH}	3006	1	2.0 V			2.0 V	2.0 V	2.0 V	2.0 V	GND	0.8 V	1/					-1 mA	4.5 V	QA	2.5		V			
			2	"			"	"	"	"	"	"	"	"					"	QB	"		"			
			3	"			"	"	"	"	"	"	"	"					"	QC	"		"	"		
			4	"			"	"	"	"	"	"	"	"					"	QD	"		"	"		
			5	"			"	0.8 V	0.8 V	0.8 V	0.8 V	"	"	"		-1 mA	-1 mA	-1 mA	"	"	QD	"		"	"	
	V _{OL}	3007	6	2.0 V			0.8 V	0.8 V	0.8 V	0.8 V	"	"	"	"					20 mA	"	QA		0.5	"		
			7	"			"	"	"	"	"	"	"	"					"	QB	"		"	"		
			8	"			"	"	"	"	"	"	"	"					"	QC	"		"	"		
			9	"			"	"	"	"	"	"	"	"					"	QD	"		"	"		
			10	"			"	2.0 V	2.0 V	2.0 V	2.0 V	"	"	"		20 mA	20 mA	20 mA	"	"	QD	"		"	"	
	V _{IC}		11	-18 mA	-18 mA						"	"	"	"						"	Clear		-1.2	"		
			12								"	"	"	"						"	J			"	"	
			13								"	"	"	"						"	K			"	"	
			14								"	"	"	"						"	A			"	"	
			15								"	"	"	"						"	B			"	"	
			16								"	"	"	"						"	C			"	"	
			17								"	"	"	"						"	D			"	"	
			18																	"	Shift/load			"	"	"
			19																	"	Clock			"	"	"
	I _{IL}	3009	20	0.5 V	0.5 V	0.5 V	5.5 V	0.5 V			"	"	"	"						5.5 V	Clear	2/	2/	mA		
			21	GND							"	"	"	"						"	J			"	"	
			22	3/							"	"	"	"						"	K			"	"	
			23								"	"	"	"						"	A			"	"	
			24								"	"	"	"						"	B			"	"	
			25								"	"	"	"						"	C			"	"	
			26								"	"	"	"						"	D			"	"	
			27																	"	Shift/load			"	"	"
			28	5.5 V																"	Clock			"	"	"
I _{IH1}	3010	29	2.7 V	2.7 V	2.7 V	5.5 V	2.7 V			"	"	"	"						"	Clear		50	μA			
		30	5.5 V							"	"	"	"						"	J			"	"		
		31	GND							"	"	"	"						"	K			"	"		
		32								"	"	"	"						"	A			"	"		
		33								"	"	"	"						"	B			"	"		
		34								"	"	"	"						"	C			"	"		
		35								"	"	"	"						"	D			"	"		
		36																	"	Shift/load			"	"	"	
		37																	"	Clock			"	"	"	
I _{IH2}		38	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V			"	"	"	"						"	Clear		1	mA			
		39	5.5 V							"	"	"	"						"	J			"	"		
		40	GND							"	"	"	"						"	K			"	"		
		41								"	"	"	"						"	A			"	"		
		42								"	"	"	"						"	B			"	"		
		43								"	"	"	"						"	C			"	"		
		44								"	"	"	"						"	D			"	"		
		45																	"	Shift/load			"	"	"	
		46	GND																"	Clock			"	"	"	

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				Clear	J	\bar{K}	Input A	Input B	Input C	Input D	GND	Shift/load	Clock	\bar{Q} D	QD	QC	QB	QA	V _{CC}		Min	Max				
1 T _C = 25°C	I _{OS}	3011	47	5.5 V				5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	1/				GND	GND	5.5 V	QA	-40	-100	mA		
			48	"				"	"	"	"	"	"	"	"				"	"	"	QB	"	"	"	
			49	"				"	"	"	"	"	"	"	"				"	"	"	QC	"	"	"	
			50	"				"	"	"	"	"	"	"	"		GND			"	"	"	QD	"	"	"
			51	"	GND				"	"	"	"	"	"	"	GND				"	"	"	QD	"	"	"
	I _{CC}	3005	52	5.5 V	GND	GND	GND	GND	GND	GND	GND	"	"	"					"	"	V _{CC}		130	mA		
I _{CEX}			53	5.5 V			5.5 V	5.5 V	5.5 V	5.5 V	"	"	"	"				5.5 V	5.5 V	"	QA		250	μA		
			54	"			"	"	"	"	"	"	"	"				"	"	"	QB		"	"		
			55	"			"	"	"	"	"	"	"	"				5.5 V	5.5 V	"	QC		"	"		
			56	"			"	"	"	"	"	"	"	"				"	"	"	QD		"	"		
			57	"				GND	GND	GND	GND	"	"	"	5.5 V	5.5 V		"	"	"	"	QD		"	"	
2	Same tests, terminal conditions, and limits as subgroup 1, except T _C = 125°C, V _{IC} tests are omitted, V _{IL} = 0.7 V and V _{OL} (max) = 0.45 V.																									
3	Same tests, terminal conditions, and limits as subgroup 1, except T _C = -55°C, V _{IC} tests are omitted.																									
7 4/ T _C = 25°C	Truth table test	3014	58	B	B	B	B	B	B	B	GND	A	A	H	L	L	L	L	5.0 V							
			59	A	A	A	"	"	"	"	"	"	"	A	A	"	"	"	"	"	"					
			60	"	"	"	"	"	"	"	"	"	"	"	B	"	"	"	"	"	"	"				
			61	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			62	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			63	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			64	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	H	"	"	"				
			65	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			66	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			67	"	"	"	"	"	"	"	"	"	"	"	"	L	H	"	"	"	"	"				
			68	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			69	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			70	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			71	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			72	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			73	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			74	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			75	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			76	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			77	"	"	"	"	B	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
			78	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				
79	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"			5/				
80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
81	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"							
85	"	"	"	"	"	"	"	"	"	"	"	"	"	H	L	"	"	"	"							
86	"	"	"	"	"	"	A	"	A	"	"	B	"	"	"	"	"	"	"							
87	"	"	"	"	"	"	A	"	A	"	"	A	"	"	"	"	"	"	"							
88	"	"	"	"	"	"	A	"	A	"	"	A	"	"	"	"	"	"	"							
89	"	"	"	"	"	"	B	A	B	A	"	A	"	"	"	"	"	"	"							
90	"	"	"	"	"	"	B	"	B	"	"	B	"	"	"	"	"	"	"							
91	"	"	"	"	"	"	B	"	B	"	"	B	"	"	"	"	"	"	"							
92	"	"	"	"	"	"	A	"	A	"	"	A	"	"	"	"	"	"	"							
93	"	"	"	"	"	"	A	"	A	"	"	B	"	"	"	"	"	"	"							

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				Clear	J	\bar{K}	Input A	Input B	Input C	Input D	GND	Shift/load	Clock	\bar{Q} D	QD	QC	QB	QA	V _{CC}		Min	Max				
7 4/ T _C = 25°C	Truth table test	3014	94	A	B	B	A	A	A	A	GND	B	A	L	H	H	H	H	H	5.0 V		5/				
			95	B	B	B	"	"	"	"	"	"	B	B	H	L	L	L	L	"						
			96	B	B	B	"	"	"	"	"	"	"	A	"	"	"	"	"	"				"		
			97	B	A	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		
			98	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		
			99	B	"	"	"	"	"	"	"	"	A	"	"	"	"	"	"	"				"		
			100	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		
			101	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"				"		
102	A	"	"	"	"	B	B	B	B	"	"	B	"	"	"	"	"	"	"							
8	Repeat subgroup 7 at T _C = 125°C and T _C = -55°C.																									
9 T _C = 25°C	f _{MAX}	6/	103	3/	5.0 V	GND					GND	5.0 V	IN		OUT				5.0 V	QD	35		MHz			
	t _{PHL1}	3003 6/	104	IN			5.0 V	5.0 V	5.0 V	5.0 V	"	GND	IN					OUT	OUT	OUT	"	Clear/QA	4	19	ns	
			105	"			"	"	"	"	"	"	"					OUT	OUT	OUT	"	Clear/QB	"	"	"	
			106	"			"	"	"	"	"	"	"	"					OUT	OUT	OUT	"	Clear/QC	"	"	"
			107	"			"	"	"	"	"	"	"	"					OUT	OUT	OUT	"	Clear/QD	"	"	"
	t _{PLH2}	"	108	"			IN	IN	IN	IN	"	IN	IN					OUT	OUT	OUT	"	Clock/QA	"	15	"	
			109	"			"	IN	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QB	"	"	"	
			110	"			"	"	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QC	"	"	"	
111	"			"	"	IN	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QD	"	"	"			
t _{PHL2}	"	112	"			IN	IN	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QA	"	20	"		
		113	"			"	IN	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QB	"	"	"		
		114	"			"	"	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QC	"	"	"		
		115	"			"	"	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QD	"	"	"		
10 T _C =125°C	f _{MAX}	6/	116	3/	5.0 V	GND					"	5.0 V	IN		OUT				"	QD	28.0		MHz			
	t _{PHL1}	3003 6/	117	IN			5.0 V	5.0 V	5.0 V	5.0 V	"	GND	IN					OUT	OUT	OUT	"	Clear/QA	4	28	ns	
			118	"			"	"	"	"	"	"	"					OUT	OUT	OUT	"	Clear/QB	"	"	"	
			119	"			"	"	"	"	"	"	"					OUT	OUT	OUT	"	Clear/QC	"	"	"	
			120	"			"	"	"	"	"	"	"					OUT	OUT	OUT	"	Clear/QD	"	"	"	
	t _{PLH2}	"	121	"			IN	IN	IN	IN	"	IN	IN					OUT	OUT	OUT	"	Clock/QA	"	19	"	
122			"			"	IN	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QB	"	"	"		
123			"			"	"	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QC	"	"	"		
124			"			"	"	IN	IN	"	"	"					OUT	OUT	OUT	"	Clock/QD	"	"	"		

See notes at end of device type 02.

TABLE III. Group A inspection for device type 02 – Continued.
Terminal conditions (pins not designated may be H ≥ 2.0 V, L ≤ 0.8 V or open)

Subgroup	Symbol	MIL-STD-883 method	Cases E,F	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	Measured terminal	Test limits		Unit			
				Test no.	Clear	J	\bar{K}	Input A	Input B	Input C	Input D	GND	Shift/load	Clock	\bar{Q} D	QD	QC	QB	QA		V _{CC}	Min		Max		
10 T _C =125°C	t _{PHL2}	3003 6/ "	125	IN			IN				GND	IN	IN							"	Clock/QA	4	25	ns		
			126	"					IN			"	"	"						"	"	Clock/QB	"	"	"	
			127	"						IN			"	"	"						"	"	Clock/QC	"	"	"
			128	"							IN		"	"	"		OUT	OUT			"	"	Clock/QD	"	"	"
11	Same tests, terminal conditions, and limits as subgroup 10, except T _C = -55°C.																									

NOTES:

- 1/ Input is a single clock pulse.
- 2/ I_{IL} = limits shall be as follows:

Measured terminal	min/max limits (mA) for circuit			
	A	B	C	D
Clear, Shift/load	-0.5/-1.5	-0.5/-1.5	-0.5/-1.5	-0.5/-1.5
J, \bar{K} , A, B, C, D, Clock	-1/-2	-1/-2	-1/-2	-1/-2

- 3/ The clear input is momentarily grounded, then raised to and held at 5.5 V.
- 4/ A = terminal connected to 2.0 V minimum. B = terminal connected to 0.8 V maximum.
- 5/ Tests shall be performed in the sequence specified. Output voltages shall be either high "H" or "L" as indicated in the terminal conditions columns. Output voltage test limits over the specified temperature range shall be either: (1) H = 2.5 V minimum and L = 0.5 V maximum when using a high speed checker double comparator, or (2) H > 1.5 V and L < 1.5 V when using a high speed checker single comparator.
- 6/ See figure 5 herein for switching test circuit and waveforms.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the military service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory)

6.1 Intended use. Microcircuits conforming to this specification are intended for logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. PIN and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirement for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to acquiring activity in addition to notification to the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of method 5003), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43123-1199.

6.4 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.5 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331, and as follows:

GND Electrical ground (common terminal)
 V_{IN} Voltage level at an input terminal
 I_{IN} Current-flowing into an input terminal

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer lead lengths and lead forming shall not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-35810 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Device type</u>	<u>Commercial type</u>
01	54S194
02	54S195

6.8 Manufacturers' designators. Manufacturers' circuits which form a part of this specification are designated with an "X" as shown in table IV herein.

TABLE IV. Manufacturers' designations.

Device type	Circuits			
	A	B	C	E
	Texas Instruments	Advanced Micro Devices	Fairchild Semiconductor	National Semiconductor
01	X	X	X	X
02	X	X	X	X

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
 Army - CR
 Navy - EC
 Air Force - 11
 DLA - CC

Preparing activity:
 DLA - CC
 (Project 5962-2005-030)

Review activities:
 Army - MI, SM
 Navy - AS, CG, MC, SH, TD
 Air Force - 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.