

INCH-POUND
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SUPERSEDING
MIL-M-38510/702
29 September 1989

MILITARY SPECIFICATION
MICROCIRCUITS, LINEAR, REGULATING, PULSE WIDTH MODULATORS, MONOLITHIC SILICON

Inactive for new design after 13 July 1995.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product herein shall consist of this specification sheet and MIL-PRF-38535.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, regulating, pulse width modulator microcircuits. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number. For this product, the requirements of MIL-M-38510 have been superseded by MIL-PRF-38535, (see 6.3)

1.2 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-38535, and as specified herein.

1.2.1 Device types. The device types are as follows:

<u>Device type</u>	<u>Circuit</u>
01	Current mode pulse width modulator controller
02	Current mode pulse width modulator controller

1.2.2 Device class. The device class is the product assurance level as defined in MIL-PRF-38535.

1.2.3 Case outlines. The case outlines are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
E	GDIP1-T16 or CDIP2-T16	16	Dual in line
2	CQCC1-N20	20	Square leadless chip carrier

Comments, suggestions, or questions on this document should be addressed to: Commander, Defense Supply Center Columbus, ATTN: DSCC-VAS, 3990 East Broad St., Columbus, OH 43218-3990, or email linear@dsc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <http://assist.daps.dla.mil>.

1.3 Absolute maximum ratings.

Supply voltage	+40 V dc
Collector supply voltage	+40 V dc
Output current, source, sink	500 mA dc
Analog inputs	-0.3 V to $+V_{IN}$
Reference output current	-30 mA dc
Sync output current	-5 mA
Error amplifier output current	-5 mA
Soft start sink current	50 mA
Oscillator charging current	5 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C.
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage range	+8.0 V dc to +35.0 V dc
Collector supply voltage range	+4.5 V dc to +35.0 V dc
Continuous output current source or sink	0 to ± 200 mA dc
Reference output current	0 to -10 mA dc
Sync output current	0 to -1.3 mA dc
Oscillator charging current	-50 μ A to -2 mA dc
Current sense amplifier input common mode range	0 V to ($V_{IN} - 3$ V)
Shutdown terminal input voltage	0 V to V_{IN}
Error amplifier differential input voltage range	$\pm V_{REF}$
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{JC}	Maximum θ_{JA}
16 lead dual in line	E	250 mW at $T_A = +125^\circ\text{C}$	60°C/W	100°C/W
20 terminal square leadless chip carrier	2	277 mW at $T_A = +125^\circ\text{C}$	30°C/W	90°C/W

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications and standards form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard for Microelectronics.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

(Copies of these documents are available online at <http://assist.daps.dla.mil/quicksearch/> or <http://assist.daps.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Qualification. Microcircuits furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.3 and 6.4).

3.2 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.3 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein.

3.3.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3.2 Block diagrams. The block diagrams shall be as specified on figure 2.

3.3.3 Schematic circuits. The schematic circuits shall be maintained by the manufacturer and made available to the qualifying activity and the preparing activity upon request.

3.3.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.4 Lead material and finish. The lead material and finish shall be in accordance with MIL-PRF-38535 (see 6.6).

3.5 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C see figure 3 unless otherwise specified	Device type	Limits		Units
				Min	Max	
Cold start/PWM latch	L _{RESET}	T _J = -55°C, R _T = 10 kΩ, C _T = 4700 pF, sync I _{OUT} = -1 mA	All	<u>2/</u>		kHz
Reference section						
Output voltage	V _{REF}	I _O = -1 mA	All	5.05	5.15	V
Line regulation	V _{RLINE}	8 V ≤ V _{IN} ≤ 40 V	All	-20	20	mV
Load regulation	V _{RLOAD}	1 mA ≤ I _L ≤ 10 mA	All	-15	15	mV
Output voltage (total variation)	V _{TVO}	Line, load, and temperature	All	5.00	5.20	V
Ripple rejection	ΔV _{IN} / ΔV _{REF}	1 V _{RMS} , f = 2400 Hz	All	55		dB
Output noise voltage	N _O	T _C = +25°C, see figure 4	All		200	μV rms
Short circuit output	I _{OS}	V _{REF} = 0 V	All	-10		mA
Oscillator section						
Initial accuracy	f _{OSC1}	T _C = +25°C, R _T = 10 kΩ, C _T = 4700 pF	All	39	47	kHz
Oscillator frequency	f _{OSC2}	T _C = -55°C and +125°C, R _T = 10 kΩ, C _T = 4700 pF		38	48	
Frequency change with voltage (voltage stability)	Δ f _{OSC} / ΔV _{IN}	8 V ≤ V _{IN} ≤ 40 V	All		2.0	%
Sync output voltage high level	V _{SOH}	I _L = -1.3 mA	All	3.9		V
Sync output voltage low level	V _{SOL}	I _L = -1.3 mA	All		2.5	V
Sync input voltage high level	V _{SIH}	C _T = 0 V	All	3.9		V
Sync input voltage low level	V _{SIL}	C _T = 0 V	All		2.5	V
Sync input current	I _{SYNC}	Sync voltage = 5.25 V, C _T = 0 V	All		1.5	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C see figure 3 unless otherwise specified	Device type	Limits		Units
				Min	Max	
Error amplifier section						
Input offset voltage	V _{IO1}		All	-5.0	5.0	mV
Input bias current	±I _{B1}		All	-1.0		μA
Input offset current	I _{IO1}		All	-250	250	nA
Open loop voltage gain	A _{VS}	ΔV _O = 1.2 V to 3 V, V _{CM} = 2 V	All	80		dB
Unity gain bandwidth	GBW	T _C = +25°C	All	0.7		Hz
Common mode rejection ratio	CMRR1	0 V ≤ V _{CM} ≤ 38 V, V _{IN} = 40 V	All	75		dB
Power supply rejection ratio	PSRR1	8 V ≤ V _{IN} ≤ 40 V, V _{CM} = 2 V	All	80		dB
Output sink current (COMPENSATION pin)	I _{SINK}	-15 mV ≤ V _{ID} ≤ -5 V, V _{COMP} pin = 1.2 V	All	2.0		mA
Output source current (COMPENSATION pin)	I _{SOURCE}	15 mV ≤ V _{ID} ≤ 5 V, V _{COMP} pin = 2.5 V	All	-0.4		mA
High level output voltage	V _{OH1}	R _L = (COMP) 15 kΩ	All	4.3		V
Low level output voltage	V _{OL1}	R _L = (COMP) 15 kΩ	All		1.0	V
Current sense amplifier section						
Amplifier gain	A _V	V _(-CUR SENSE pin) = 0 V, V _(CUR LIM/SS pin) open <u>3/ 4/</u>	All	2.5	3.15	V
Maximum differential signal (positive and negative current sense pin voltages)	V _{DIFF}	V _(CUR LIM/SS pin) open, <u>3/</u> (COMP pin) = 15 kΩ	All	1.1		V
Input offset voltage	V _{IO2}	V _(CUR LIM/SS pin) = 0.5 V, COMP pin open <u>3/</u>	All	-25	25	mV
Common mode rejection ratio	CMRR2	1 V ≤ V _{CM} ≤ 12 V	All	60		dB
Power supply rejection ratio	PSRR2	8 V ≤ V _{IN} ≤ 40 V	All	60		dB

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions ^{1/} -55°C ≤ T _C ≤ +125°C see figure 3 unless otherwise specified	Device type	Limits		Units
				Min	Max	
Current sense amplifier section - continued						
Input bias current	I _{IB2}	V(CUR LIM/SS pin) = 0.5 V, COMP pin open ^{3/}	All	-10		μA
Input offset current	I _{IO2}	V(CUR LIM/SS pin) = 0.5 V, COMP pin open ^{3/}	All	-1.0	1.0	μA
Time delay to outputs	t _{D1}	T _C = +25°C	All		500	ns
Current limit adjust section						
Current limit offset voltage	V _{CLO}	V(-CUR SENSE pin) = 0 V, V(+CUR SENSE pin) = 0 V, COMP pin open ^{3/}	All	0.40	0.55	V
Input bias current voltage	I _{IB3}	V(+ERROR AMP pin) = V _{REF} , V(-ERROR AMP pin) = 0 V	All	-30		μA
SHUTDOWN terminal section						
Threshold voltage	V _{TH}		All	250	400	mV
Latching voltage	V _{LATCH}	Current into CUR LIM/SS pin = 3.0 mA ^{5/}	All		2.0	V
Nonlatching voltage	V _{NLATCH}	Current into CUR LIM/SS pin = 0.8 mA ^{6/}	All	5.0		V
Time delay to outputs	t _{D2}	T _C = +25°C	All		600	ns
Output section						
Collector emitter voltage	V _{CE}		All	40		V
Collector leakage current	I _C	V _C = 40 V ^{7/}	All		200	μA
Low level output voltage	V _{OL2}	I _{SINK} = 20 mA	All		0.4	V
		I _{SINK} = 100 mA			2.1	
High level output voltage	V _{OH2}	I _{SOURCE} = -20 mA	All	13		V
		I _{SOURCE} = -100 mA		12		
Rise time	t _r	C _L = 1,000 pF	All		130	ns
Fall time	t _f	C _L = 1,000 pF	All		130	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _C ≤ +125°C see figure 3 unless otherwise specified	Device type	Limits		Units
				Min	Max	
Under voltage lockout section						
Start up threshold voltage	V _{SU}		All		8.0	V
Shutdown threshold voltage	V _{SD}		All	6.0		V
Total standby current section						
Supply current	I _{IN}	CURR LIM/SS pin = 0.7 V	All		21	mA

1/ Standard test conditions (unless otherwise specified): +V_{IN} = 15 V dc, timing resistance = 10 kΩ, and timing capacitance = 4,700 pF.

2/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWM LATCH SET command. To minimize the effects of self heating, the test must be completed with the first 50 ms of applied power. The minimum limit shall be equal to 0.49 times the oscillator frequency.

3/ Parameter measured at trip point of latch with V_{+ERROR AMP} = V_{REF}, V_{-ERROR AMP} = 0 V.

4/ Amplifier gain defined as:

$$G = \Delta V_{\text{COMP pin}} / \Delta V_{\text{+CURRENT SENSE pin}} ; \Delta V_{\text{+CURRENT SENSE pin}} = 0 \text{ to } 10 \text{ V.}$$

5/ Current into CUR LIM/SS pin guaranteed to latch circuit in shutdown state.

6/ Current into CUR LIM/SS pin guaranteed not to latch circuit in shutdown state.

7/ This parameter only applies to device type 01.

3.6 Electrical test requirements. Electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.7 Marking. Marking shall be in accordance with MIL-PRF-38535.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 52 (see MIL-PRF-38535, appendix A).

TABLE II. Electrical test requirements.

MIL-PRF-38535 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters	1	1
Final electrical test parameters	1*, 2, 3, 4, 5, 6	1*, 2, 3, 4, 5, 6
Group A test requirements	1, 2, 3, 4, 5, 6, 7, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 9
Group B electrical test parameters when using the method 5005 QCI option	1, 2, 3, and table IV delta limits	N/A
Group C end-point electrical parameters	1, 2, 3, and table IV delta limits	1 and table IV delta limits
Additional electrical subgroup for group C Periodic inspections	N/A	10,11
Group D end-point electrical parameters	1, 2, 3	1

*PDA applies to subgroup 1.

4. VERIFICATION.

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. The burn-in test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- c. Additional screening for space level product shall be as specified in MIL-PRF-38535.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-38535.

Device types	01 and 02	
Case outlines	E	2
Terminal number	Terminal symbol	
1	CUR LIMIT / SOFTSTART	NC
2	V _{REF}	CUR LIMIT / SOFTSTART
3	-CUR SENSE	V _{REF}
4	+CUR SENSE	NC
5	+ERROR AMP	-CUR SENSE
6	-ERROR AMP	+CUR SENSE
7	COMPENSATION	+ERROR AMP
8	C _T	-ERROR AMP
9	R _T	COMPENSATION
10	SYNC	C _T
11	OUTPUT A	NC
12	GND	R _T
13	V _C	SYNC
14	OUTPUT B	OUTPUT A
15	V _{IN}	GND
16	SHUTDOWN	V _C
17	---	OUTPUT B
18	---	NC
19	---	V _{IN}
20	---	SHUTDOWN

NOTE: NC = no connection

Figure 1. Terminal connections.

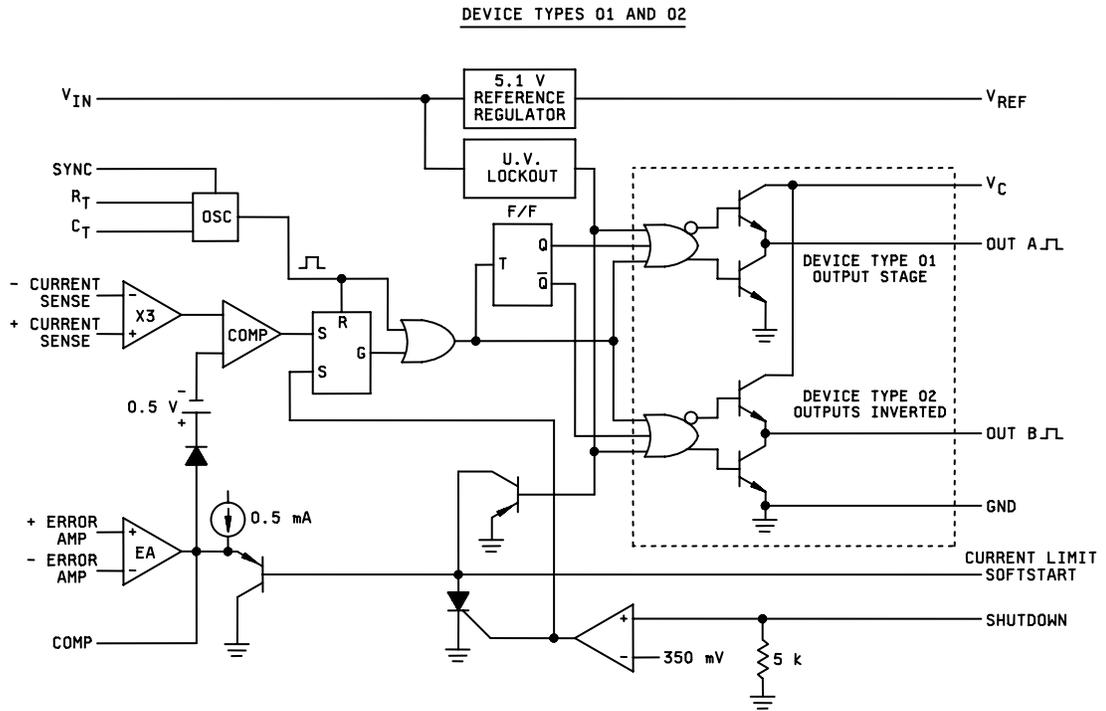


FIGURE 2. Block diagram.

DEVICE TYPES 01 AND 02

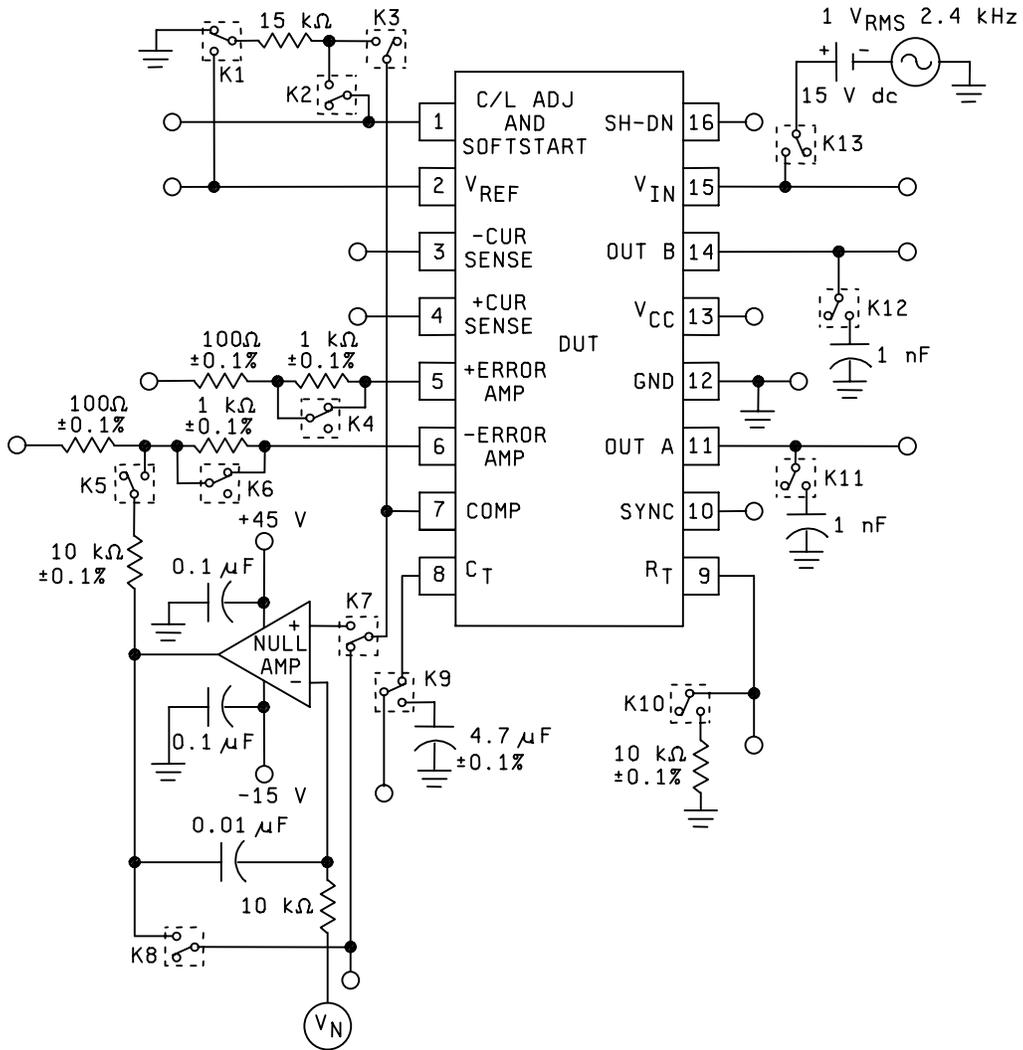
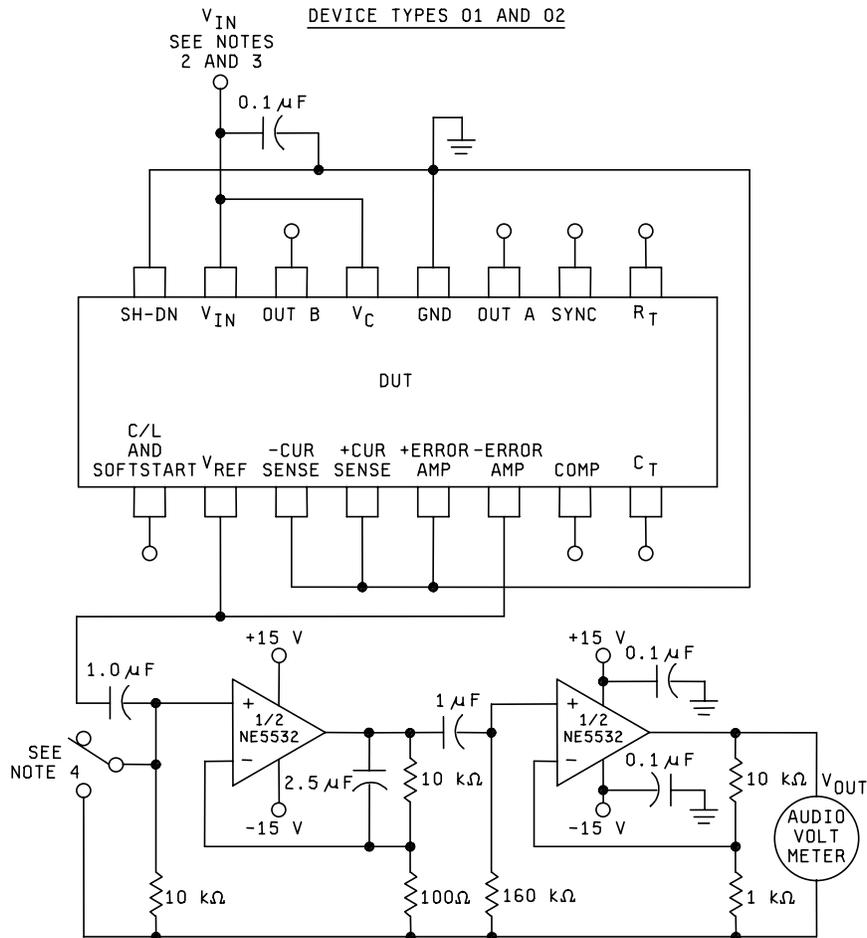


FIGURE 3. Test circuit for static and dynamic tests.



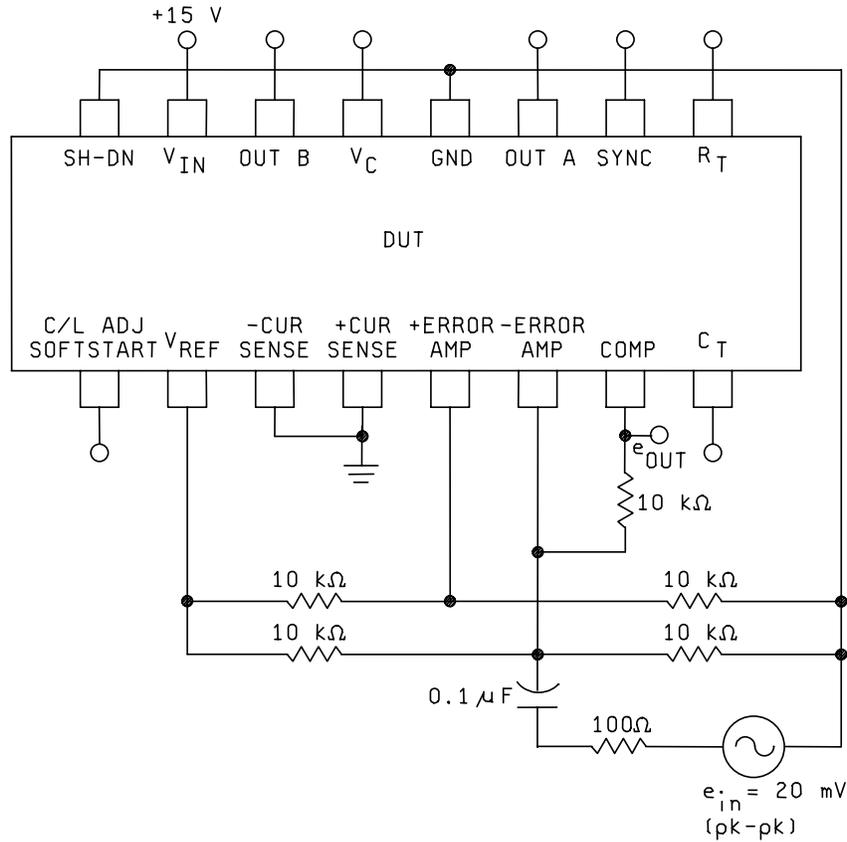
NOTES:

1. All resistors are $\pm 1\%$, all capacitors are $\pm 5\%$.
2. $V_{IN} = 15\text{ V}$ for V_{REF} output noise voltage test.
3. $V_{IN} = 15\text{ V} + 1\text{ V}_{RMS}$ 2.4 kHz for V_{REF} ripple rejection test.
4. V_{REF} output noise voltage is measured by determining both the measurement system noise (V_{OUT} with input grounded) and the noise with V_{REF} output connected and then applying the following formula.

$$N_O = \sqrt{(\text{Measurement})^2 - (\text{Measurement System Noise})^2} / \text{GAIN} (= 1,111)$$

FIGURE 4. Output noise voltage and ripple rejection test circuit.

DEVICE TYPES 01 AND 02

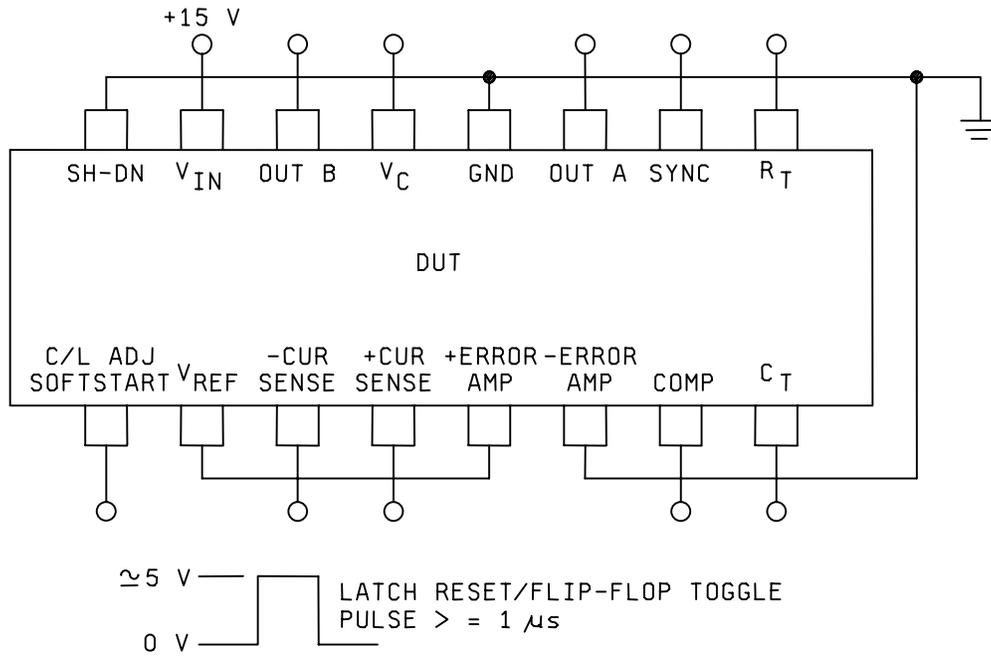


NOTES:

1. GBW is measured by increasing signal frequency (starting at 100 kHz) until $e_{OUT} = e_{in}$. The frequency at which this occurs is GBW .
2. Alternate method: Set frequency to 700 kHz. If $e_{OUT} \geq e_{in}$ then $GBW \geq 700$ kHz.
3. All resistors are $\pm 1\%$, all capacitors are $\pm 5\%$.

FIGURE 5. Error amplifier unity gain bandwidth test circuit.

DEVICE TYPES 01 AND 02



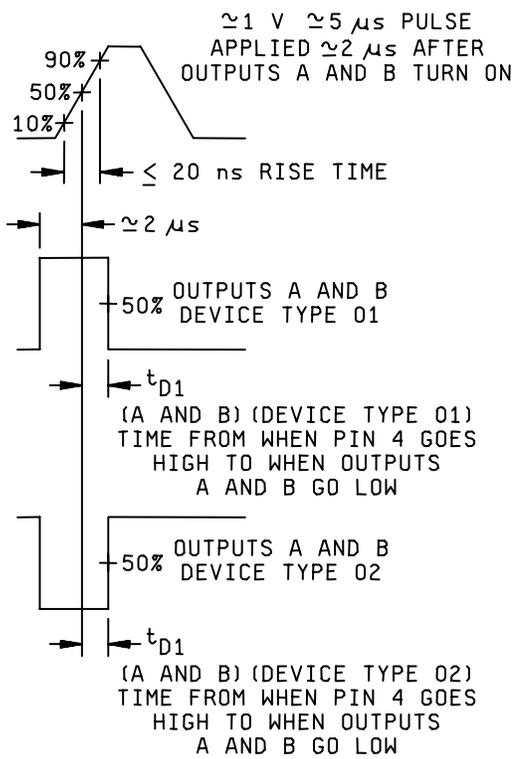
NOTE: Refer to table III for conditions of pins 1, 3, 4, 7, and 15.

FIGURE 6. Latch reset and flip-flop toggle test circuit.

DEVICE TYPES 01 AND 02

a. CURRENT SENSE AMPLIFIER
DELAY TO OUTPUTS

PIN 4 (C/S +INPUT)



b. SHUTDOWN TERMINAL
DELAY TO OUTPUTS

PIN 16 (SHUTDOWN)

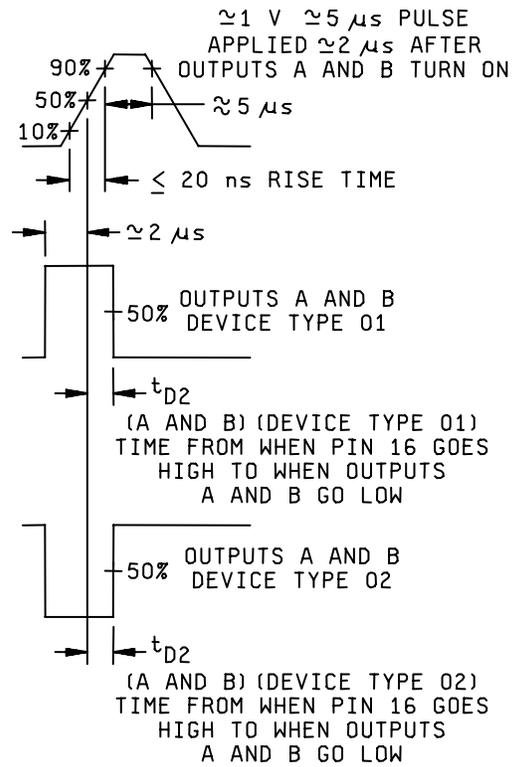


FIGURE 7. Test waveforms.

TABLE III. Group A inspection for device types 01 and 02.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/																Energy relays	Measured pin(s)			Notes and equations	Limits		Unit	
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V _N		No.	Val.	Unit		Min	Max		
			C.L. adj.	V _{REF}	Cur -	Sense +	Error +	Amp -	Comp	C _T	R _T	Sync	Output A	V _C	Output B	V _{IN}	Shut-down										
1 T _c = +25°C	V _{REF}	1	Open	-1 mA	GND	GND	GND	V _{REF}	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	2	E1	V	V _{REF} = E1	5.05	5.15	V	
	V _{RLOAD}	2	"	-10 mA	"	"	"	"	"	"	"	"	"	"	"	15 V	"		"	2	E2	V	V _{RLOAD} = E2-E1	-15	15	mV	
	V _{RLINE}	3	"	0 mA	"	"	"	"	"	"	"	"	"	"	"	8 V	"		"	2	E3	V	V _{RLINE} = E4-E3	-20	20	mV	
			"	"	"	"	"	"	"	"	"	"	"	"	"	40 V	"		"	2	E4	V					
	V _{TVO}	4																						VTVO = E2	5.00	5.20	V
		5																						VTVO = E1 + V _{RLINE}	5.00	5.20	V
		6																						VTVO = E2 + V _{RLINE}	5.00	5.20	V
	I _{OS}	7	Open	0 V	GND	GND	GND	V _{REF}	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	2	I1	mA	I _{OS} = I1 3/	-80		mA	
	V _{SOH}	8	"	Pin 6	"	"	"	"	"	V _{REF} (Pin 2)	Open	-1.3 mA	"	"	"	"	"	"	"	"	10	E5	V	V _{SOH} = E5	3.9		V
	V _{SOL}	9	"	"	"	"	"	"	"	GND	"	Open	"	"	"	"	"	"	"	"	10	E6	V	V _{SOL} = E6		2.5	V
	V _{SIH}	10	"	Pin 5	"	"	V _{REF}	GND	"	0 V	"	3.9 V	"	"	"	"	"	"	None	11	E7	V	V _{SIH} ≥ 3.9 V if both E7 and E8 = limit 4/ 5/	13 (Type 02 only)	0.4 (Type 01 only)	V	
			"	"	"	"	"	"	"	"	4/	"	5/	"	"	"	"	"	"	14	E8	V					
	V _{SIL}	11	"	"	"	"	"	"	"	"	"	2.5 V	"	"	"	"	"	"	"	"	11	E9	V	V _{SIL} ≥ 2.5 V if both E9 or E10 = limit 4/ 5/	13 (Type 01 only)	0.4 (Type 02 only)	V
"			"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	E10	V					
I _{SYNC}	12	"	Pin 6	"	"	GND	V _{REF}	"	"	"	5.25 V	"	"	"	"	"	"	"	"	10	I2	mA	I _{SYNC} = I2		1.5	mA	
V _{IO1}	13	"	Open	"	"	2.6 V	2.6 V	"	Open	Open	Open	"	"	"	"	"	"	2.6 V	K5, K7, K8	7 to 6	E11	V	V _{IO1} = E11/101	-5	5	mV	
-I _{IB1}	14	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	K5, K6, K7, K8	"	E12	V	-I _{IB1} = (E12 - E11) / 101000	-1		μA	
+I _{IB1}	15	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	K4, K5, K7, K8	"	E13	V	+I _{IB1} = (E11 - E13) / 101000	-1		μA	

See footnote at end of table.

TABLE III. Group A inspection for device types 01 and 02 – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers <u>1/</u>																Energ. relays	Measured pin(s)			Notes and equations	Limits		Unit	
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V _N		No.	Val.	Unit		Min	Max		
			C.L. adj.	V _{REF}	Cur -	Sense +	Error +	Amp -	Comp	C _T	R _T	Sync	Output A	V _C	Output B	V _{IN}	Shut-down										
1 T _c = +25°C	I _{IO1}	16																				I _{IO1} = (-I _{B1}) - (+I _{B1})	-250	250	nA		
	CMRR1	17	Open	Open	GND	GND	0 V	0 V	Open	Open	Open	Open	Open	15 V	Open	40 V	GND	2.6 V	K5, K7, K8	7 to 6	E14	V	CMRR1 = 20 log (101 x 38 V) / E14-E15	75		dB	
			"	"	"	"	38 V	38 V	"	"	"	"	"	"	"	"	"	"	"	"	"	E15					"
	I _{SINK}	18	"	"	"	"	GND	15 mV	2 mA	"	"	"	"	"	"	15 V	"		None	7	E16	V	I _{SINK} ≥ 2 mA if E16 = limit		1.2	V	
	I _{SOURCE}	19	"	"	"	"	15 mV	GND	-4 mA	"	"	"	"	"	"	"	"		"	"	E17	V	I _{SOURCE} ≤ -0.4 mA if E17 = limit	2.5		V	
	V _{OH1}	20	"	"	"	"	15 mV	"	15 kΩ to GND	"	"	"	"	"	"	"	"		K3	"	E18	V	V _{OH1} = E18	4.3		V	
	V _{OL1}	21	"	"	"	"	GND	15 mV	15 kΩ to V _{REF}	"	"	"	"	"	"	"	"	"		K1, K3	"	E19	V	V _{OL1} = E19		2.5	V
			"	Pin 5	"	"	V _{REF}	GND	1.5 V <u>g/</u>	0 V <u>4/</u>	"	"	"	"	15 V <u>5/</u>	"	"	"	"		None	"	E20	V	A _v = (E21-E20) / (1 V <u>4/ 6/ 7/ 8/</u>)	2.5	3
	"	"	"	1 V	"	"	4.5 V <u>g/</u>	"	"	"	"	"	"	"	"	"	"	"	"	"	E21	V					
	V _{DIFF}	23	"	"	"	1 V <u>g/</u>	"	"	15 kΩ to GND	"	"	"	"	"	"	"	"	"		K3	4 to 3	E22	V	V _{DIFF} = E22 <u>4/ 6/ 7/ 8/</u>	1.1		V
V _{IO2}	24	0.5 V	"	"	-40 mV <u>7/ 8/</u>	"	"	Open	"	"	"	"	"	"	"	"	"		None	"	E23	mV	V _{IO2} = E23 <u>4/ 6/ 7/ 8/</u>	-25	25	mV	
CMRR2	25	"	"	1 V	"	"	"	"	"	"	"	"	"	"	"	"	"		"	"	E24	mV	CMRR2 = 20 log (11 V) / E25-E24 <u>4/ 6/ 7/ 8/</u>	60		dB	
		"	"	12 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	"	E25					mV
-I _{B2}	26	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	"		"	3	I3	μA	-I _{B2} = I3 <u>4/ 6/ 7/ 8/</u>	-10		μA	
+I _{B2}	27	"	"	GND	"	"	"	"	"	"	"	"	"	"	"	"	"		"	4	I4	mA	+I _{B2} = I4 <u>4/ 6/ 7/ 8/</u>	-10		μA	

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/																Energ. relays	Measured pin(s)			Notes and equations	Limits		Unit
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V _N		No.	Val.	Unit		Min	Max	
			C.L. adj.	V _{REF}	Cur -	Sense +	Error +	Amp -	Comp	C _T	R _T	Sync	Output A	V _C	Output B	V _{IN}	Shut-down									
1 T _c = +25°C	I _{IO2}	28																				I _{IO2} = I4-I3	-1	1	μA	
	V _{IO2}	29	0.5 V _{g/}	Pin 5	GND	GND	V _{REF}	GND	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	1	E26	V	V _{IO2} = E26 4/ 6/ 7/ 9/	0.45	0.55	V
	I _{B3}	30	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1	I5	μA	I _{B3} = I5	-30		μA
	V _{TH(LO)}	31	15 kΩ to V _{REF} 10/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	250 mV	"	11	E27	V	V _{TH(LO)} ≤ 250 mV if E27 or E28 = limit 4/ 5/	13 (Type 01 only)	0.4 (Type 02 only)	V
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	E28		V		
	V _{TH(HI)}	32	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	400 mV	"	11	E29	V	V _{TH(HI)} ≤ 0.4 V if both E29 and E30 = limit 4/ 5/ and E31 = limit	13 (Type 01 only)	0.4 (Type 02 only)	V
					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	E30		V		
					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		1	E31	V
	V _{NLATCH}	33	0.8 mA	Pin 5	"	"	"	"	"	"	GND	"	"	"	"	"	"	400 mV	None	1	E32	V	V _{NLATCH} ≤ 0.8 mA if E32 and E33 = limit		0.45	V
					"	"	"	"	"	"	"	"	"	"	"	"	0 V	"		E33	V	4				
	V _{LATCH}	34	3 mA	Pin 5	"	"	"	"	"	"	"	"	"	"	"	"	"	400 mV	"	"	E34	V	V _{LATCH} ≥ 3 mA if E34 and E35 = limit		0.45	V
					"	"	"	"	"	"	"	"	"	"	"	"	0 V	"		E35	V			0.45		
	I _C	35	Open	Pin 6	"	"	GND	V _{REF}	"	"	"	"	"	"	"	"	40 V	0.4 V	"	13	I6	μA	I _C = I6	200	μA	
	V _{OL2A(LO)}	36	"	Pin 5	"	"	V _{REF}	GND	"	11/	"	"	"	20 mA	"	"	15 V	GND	"	11	E36	V	V _{OL2A(LO)} = E36		0.4	V
V _{OL2A(HI)}	37	"	"	"	"	"	"	"	"	"	"	"	100 mA	"	"	"	"	"	"	E37	V	V _{OL2A(HI)} = E37		2.1	V	
V _{OL2B(LO)}	38	"	"	"	"	"	"	"	"	"	"	"	Open	"	20 mA	"	"	"	14	E38	V	V _{OL2B(LO)} = E38		0.4	V	
V _{OL2B(HI)}	39	"	"	"	"	"	"	"	"	"	"	"	"	"	100 mA	"	"	"	"	E39	V	V _{OL2B(HI)} = E39		2.1	V	
V _{OH2A(LO)}	40	"	"	"	"	"	"	"	"	"	"	"	-20 mA	"	Open	"	"	"	11	E40	V	V _{OH2A(LO)} = E40	13		V	
V _{OH2A(HI)}	41	"	"	"	"	"	"	"	"	"	"	"	-100 mA	"	"	"	"	"	"	E41	V	V _{OH2A(HI)} = E41	12		V	
V _{OH2B(LO)}	42	"	"	"	"	"	"	"	"	"	"	"	Open	"	-20 mA	"	"	"	14	E42	V	V _{OH2B(LO)} = E42	13		V	
V _{OH2B(HI)}	43	"	"	"	"	"	"	"	"	"	"	"	"	"	-100 mA	"	"	"	"	E43	V	V _{OH2B(HI)} = E43	12		V	

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 and 02 – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 1/																Energ. relays	Measured pin(s)			Notes and equations	Limits		Unit	
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V _N		No.	Val.	Unit		Min	Max		
			C.L. adj.	V _{REF}	Cur -	Sense +	Error +	Amp -	Comp	C _T	R _T	Sync	Output A	Output B	V _{IN}	Shut-down											
1 T _C = +25°C	V _{SU}	44	15 kΩ to V _{REF} 10/	GND	GND	V _{REF}	GND	Open	4/	Open	Open	Open	5/	Open	Raise from ≤ 6 V to 8 V	GND		K1, K2	11 14 1	E44 E45 E46	V V V	V _{SU} ≤ 8 V if E44 or E45 = limit and E46 = limit 4/ 5/	13 (Type 01)	0.4 (Type 02)	V V V		
	V _{SD}	45	15 kΩ to V _{REF} 10/	GND	GND	V _{REF}	GND	Open	4/	Open	Open	Open	5/	Open	Lower from ≥ 8 V to 6 V	GND		K1, K2	11 14 1	E47 E48 E49	V V V	V _{SD} ≥ 6 V if both E47 and E48 = limit and E49 = limit 4/ 5/	13 (Type 02)	0.4 (Type 01)	V V V		
	I _{IN}	46	0.7 V	Pin 5	"	"	"	"	"	Open	"	"	"	15 V	"	15 V	GND		None	15	I7	mA	I _{IN} = I7 4/		22	mA	
2 T _C = +125°C	V _{TVO}	47	Open	-1 mA	"	"	GND	V _{REF}	"	"	"	"	"	"	"	"	"	"	"	2	E50	V	V _{TVO} = E50	5.00	5.20	V	
		48 through 92	All test parameters, test conditions, and test limits remaining are identical with tests 2-46 specified in table III, subgroup 1, T _C = +25°C.																								
3 T _C = -55°C		93 through 138	All test parameters, test conditions, and test limits remaining are identical with those specified in table III, subgroup 2, T _C = +125°C.																								
3 T _J = -55°C	LRESET		Open		GND	GND	GND	GND	Open	4.7 nF to GND	10 kΩ to GND	-1 mA		15 V		15 V	GND		K9, K10	11 and 14					2/		
4 T _J = +25°C	ΔV _{IN} / ΔV _{REF}	139	"	Pin 6	"	"	"	V _{REF}	"	Open	Open	Open	Open	"	Open	15 V + 1 V RMS at 2.4 kHz	"		K13	2	E152	mV rms	ΔV _{IN} / ΔV _{REF} = 20 log (1 V / E152) (see figure 4)	55		dB	
	f _{OSC1}	140	"	"	"	"	"	"	"	4.7 nF to GND	10 kΩ to GND	"	"	"	"	15 V	"		K9, K10	11	F1	kHz	f _{OSC1} = 2 x F1	39	47	kHz	
	Δf _{OSC} / ΔV _{IN}	141	"	"	"	"	"	"	"	"	"	"	"	"	"	8 V	"		"	"	F2	kHz	Δf _{OSC} / ΔV _{IN} = 100 x (F3-F2) / F2	-2	2	%	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	40 V	"		"	"	F3	kHz						

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers <u>1/</u>																Energ. relays	Measured			Notes and equations	Limits		Unit									
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V _N		No.	Val.	Unit		Min	Max										
			C.L. adj.	V _{REF}	Cur -	Sense +	Error +	Amp -	Comp	C _T	R _T	Sync	Output A	V _C	Output B	V _{IN}	Shut-down																		
4 T _J = +25°C	A _{VS}	142	Open	Open	GND	GND	2 V	2V	Open	Open	Open	Open	Open	15 V	Open	15 V	GND	1.2 V	K5, K7, K8	7 to 6	E153	V	A _{VS} = 20 log (101 x 1.8 V) / E154-E153	80		dB									
																											E154	V							
4 T _C = +25°C	PSRR1	143	"	"	"	"	"	"	"	"	"	"	"	"	"	8 V	"	2 V	None	3	E155	V	PSRR1 = 20 log (101 x 32 V) / E156-E155	80		dB									
																											E156	V							
4 T _C = +25°C	PSRR2	144	0.5 V	Pin 5	40 mV 8/	GND	V _{REF}	GND	Open	4/	Open	Open	Open	15 V 5/	Open	8 V	"	None	3	E157	mV	PSRR2 = 20 log (32 V) / E158-E157 4/ 6/ 8/	60		dB										
																											E158	mV							
5 T _C = +125°C		145, 147 through 150	(With the exception of f _{OSC2} (see test 146), all test parameters, test conditions, equations, notes and test limits are identical with those specified in table III, subgroup 4, T _C = +25°C.)																																
	f _{OSC2}	146	(Test parameters and conditions are identical with those specified in table III, subgroup 4, test 140.)																11	F4	kHz	f _{OSC} = 2 x F4	38	48	kHz										
6 T _C = -55°C		151 through 156	(All test parameters, test conditions, equations, notes, and test limits are identical with those specified in table III, subgroup 5, T _C = +125°C.)																																
7 T _C = +25°C	N _O	157	Open	See fig. 4	GND	GND	GND	V _{REF}	Open	Open	Open	Open	Open	15 V	Open	15 V	GND		None	See fig. 4	E175	V RMS	See figure 4 for N _O test figure and equation	200		μV RMS									
	GBW	158	"	See fig. 5	"	"	See fig. 5			"	"	"	"	"	"	"	"		"	7	F7	MHz	GBW = F7, see figure 5	0.7		MHz									
9 T _C = +25°C	t _{D1A}	159	0.7 V	Pin 5	"	See fig. 7	V _{REF}	GND	Open	4.7 nF to GND	10 kΩ to GND	Open	See fig. 7	15 V	See fig. 7	"	"		K9, K10	11	t1	ns	t _{D1A} = t1, see figure 7	500		μV RMS									
	t _{D1B}	160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t2	ns	t _{D1B} = t2, see figure 7	500		ns									
	t _{D2A}	161	15 kΩ to V _{REF} 10/			GND	"	"	"	"	"	"	"	"	"	"	"	See fig. 7	K1, K2, K9, K10	11	t3	ns	t _{D2A} = t3, see figure 7 10/	600		ns									
	t _{D2B}	162	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t4	ns	t _{D2B} = t4, see figure 7 10/	600		ns									
	t _{rA}	163	Open	Pin 5	"	"	"	"	"	"	"	"	"	1 nF to GND	"	1 nF to GND	"	GND		K11, K12	11	t5	ns	t _{rA} = t5 12/	130		ns								
	t _{rB}	164	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"		"	14	t6	ns	t _{rB} = t6 12/	130		ns								

See footnotes at end of table.

TABLE III. Group A inspection for device types 01 and 02 – Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers ^{1/}																Energ. relays	Measured			Notes and equations	Limits		Unit
			1	2	3	4	5	6	7	8	9	10	11	13	14	15	16	V _N		No.	Val.	Unit		Min	Max	
			C.L. adj.	V _{REF}	Cur -	Sense +	Error +	Amp -	Comp	C _T	R _T	Sync	Output A	V _C	Output B	V _{IN}	Shut-down									
9	t _{fA}	165	Open	Pin 5	GND	GND	V _{REF}	GND	Open	4.7 nF to GND	10 kΩ to GND	Open	1 nF to GND	15 V	1 nF to GND	15 V	GND		K11, K12	11	t7	ns	t _{fA} = t7 ^{12/}	130	ns	
	T _C = +25°C	t _{fB}	166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	t8	ns	t _{fB} = t8 ^{12/}	130	ns
10	T _C = +125°C	t _{rA}	167	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	11	t9	ns	t _{rA} = t9 ^{12/}	130	ns
		t _{rB}	168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	t10	ns	t _{rB} = t10 ^{12/}	130
	t _{fA}	169	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	11	t11	ns	t _{fA} = t11 ^{12/}	130	ns
	t _{fB}	170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	t12	ns	t _{fB} = t12 ^{12/}	130
11	T _C = -55°C	171 through 174	All test parameters, test conditions, equations, notes, and test limits are identical with those specified in table III, subgroup 10, T _C = +125°C.																							

- 1/ Pin 12 = ground.
- 2/ To verify that the PWM latch is resetting properly, the output stage must resume switching after the completion of a PWM LATCH SET command. To minimize the effects of self heating, the test must be completed within the first 50 ms of applied power. The minimum limit shall be equal to 0.49 times the oscillator frequency.
- 3/ t < 100 ms, continuous I_{OS} will be less than indicated limits.
- 4/ Test may need to be preceded by a PWM LATCH RESET pulse. To reset latch, see figure 6.
- 5/ Digital logic methods may be used to determine the "on" or "off" status of the outputs (pins 11, 14). The voltage applied to the V_C pin (13) and the (min, max) limits may then be changed to accommodate the appropriate logic levels.
- 6/ Measuring at trip point of latch.
- 7/ Voltage on pin 4 measured and or applied with respect to voltage at pin 3.
- 8/ Raise voltage on designated pin until both outputs are in the off state. (0.4 V maximum for type 01, 13 V minimum for type 02). See note 5.
- 9/ Lower voltage on designated pin until both outputs are in the off state. (0.4 V maximum for type 01, 13 V minimum for type 02). See note 5.
- 10/ To enable testing of the intended shutdown path, pin 1 must be pulled up by a minimum of 250 μA (at pin 1 = 0.5 V).
- 11/ For type 01 V_{OL} and type 02 V_{OH}, pin 8 = 5 V. For type 02 V_{OL} and type 01 V_{OH}, see note 13.
- 12/ Measured from 1 V to 11 V at device pins 11 and 14, to 12 (not at adapter pins), see table I, note 8.
- 13/ Toggle flip flop to turn on desired output (see figure 6).

4.4 Technology Conformance inspection (TCI). Technology conformance inspection shall be in accordance with MIL-PRF-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table III of MIL-PRF-38535 and as follows:

- a. Tests shall be as specified in table II herein.
- b. Subgroup 8 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of MIL-PRF-38535.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table IV of MIL-PRF-38535 and as follows:

- a. End point electrical parameters shall be as specified in table II herein.
- b. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document control by the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- c. Special subgroups shall be added to group C inspection requirements for class B devices and shall consist of the tests, conditions, and limits of subgroups 10 and 11 as specified in table III herein.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table V of MIL-PRF-38535. End point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified and as follows.

4.5.1 Voltage and current. All voltage values given are referenced to the external zero reference level of the supply voltage. Current values are given for conventional current and are positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When actual packaging of materiel is to be performed by DoD personnel, these personnel need to contact the responsible packaging activity to ascertain requisite packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Department of Defense Agency, or within the Military Department's System Command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

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TABLE IV. Group C end-point electrical parameters. $T_C = +25^\circ\text{C}$

Table III test number	Device types	Test	Limits		Unit	Delta		Unit
			Min	Max		Min	Max	
13	01, 02	V_{IO1}	-5.0	+5.0	mV	-0.7	+0.7	mV
14	01, 02	$\pm I_B$	-1.0		μA	-0.1	+0.1	μA
1	01, 02	V_{REF}	+5.00	+5.10	V	-20	+20	mV

1/ Delta limits apply to the measured value (see MIL-PRF-38535).

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of the specification.
- b. Pin and compliance identifier, if applicable (see 1.2).
- c. Requirements for delivery of one copy of the conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- d. Requirements for certificate of compliance, if applicable.
- e. Requirements for notification of change of product or process to acquiring activity in addition to notification of the qualifying activity, if applicable.
- f. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.
- g. Requirements for product assurance options.
- h. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements should not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- i. Requirements for "JAN" marking.
- j. Packaging requirements (see 5.1).

6.3 Superseding information. The requirements of MIL-M-38510 have been superseded to take advantage of the available Qualified Manufacturer Listing (QML) system provided by MIL-PRF-38535. Previous references to MIL-M-38510 in this document have been replaced by appropriate references to MIL-PRF-38535. All technical requirements now consist of this specification and MIL-PRF-38535. The MIL-M-38510 specification sheet number and PIN have been retained to avoid adversely impacting existing government logistics systems and contractor's parts lists.

6.4 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List QML-38535 whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or purchase orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DSCC-VQ, 3990 E. Broad Street, Columbus, Ohio 43128-3990.

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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

LRESET	Cold start/PWM latch.
VTVO	Total variation of output voltage.
V _{SOL} and V _{SOH}	Sync output voltage (high and low levels) of the oscillator section.
V _{SIL} and V _{SIH}	Sync input voltage (high and low levels) of the oscillator section.
ISYNC	Sync input current.
ISINK	Output sync current (compensation pin) of the error amplifier.
ISOURCE	Output source current (compensation pin) of the error amplifier.
V _{DIFF}	Maximum differential input signal (negative and positive current) sense pin voltages.
V _{CLO}	Current limit offset voltage.
V _{TH}	Threshold voltage of the shutdown section.
V _{LATCH}	Latching voltage of the shutdown terminal.
V _{NLATCH}	Nonlatching voltage of the shutdown terminal.
V _{SU}	Start-up threshold voltage.
V _{SD}	Shutdown threshold voltage.

6.6 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish A (see 3.4). Longer length leads and lead forming should not affect the part number.

6.7 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information should not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-PRF-38535.

<u>Military device type</u>	<u>Generic-industry type</u>
01	UC1846
02	UC1847

MIL-M-38510/702A

6.8 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:

Army – CR
Navy - EC
Air Force - 11
DLA – CC

Preparing activity:

DLA - CC

Project 5962-2074

Review activities:

Army - MI, SM
Navy - AS, CG, SH, TD
Air Force – 03, 19, 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <http://assist.daps.dla.mil>.