

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, BIPOLAR,
SEMICUSTOM (GATE ARRAY) DEVICES, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, Bipolar, semicustom (gate array) devices. Two product assurance classes (B and S) and a choice of case outline/lead finish are provided for each type, and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type (total number of usable gates) and circuit organization shall be as identified in the specific altered item drawing (AID) and as follows:

<u>Device type</u>	<u>Circuit</u>
01	< 1000 gate, gate array
02	< 3500 gate, gate array
03	< 5000 gate, gate array

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline and letter shall be in accordance with MIL-M-38510, appendix C.

<u>Letter</u>	<u>Case outline</u>	<u>Manufacturer</u>
X	P-AF (148-pin), square pin grid array	A, B

1.3 Absolute maximum ratings.

Current mode logic (CML) supply voltage - - -	6.0 V dc
TTL supply voltage - - - - -	7.0 V dc
Supply voltage range V_{CC} - - - - -	-0.5 V dc to 7.0 V dc
Supply voltage range V_{EE} - - - - -	+0.5 V dc to -7.0 V dc
Input voltage range - - - - -	V_{EE} to V_{CC}
Input current continuous - - - - -	-30 mA to 1.0 mA
Voltage applied to open-collector outputs in off-state - - - - -	-0.5 V dc to 7.0 V dc
Thermal resistance, junction-to-case (θ_{JC}) - -	12 °C/W
Junction temperature (T_J) - - - - -	+140 °C
Maximum power dissipation - - - - -	14 W

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended dc operating conditions.

V _{CC1}	CML logic supply voltage- - (reduced power)	2.97 minimum to 3.63 maximum V dc
V _{CC1}	CML logic supply voltage- -	4.5 minimum to 5.5 maximum V dc
V _{CC2}	TTL I/O supply voltage- - -	4.5 minimum to 5.5 maximum V dc
V _{EE1} (reduced)	CML supply voltage- - - -	-3.63 minimum to -2.97 maximum V dc
V _{EE1} (ECL 100K)	CML supply voltage- - - -	-4.95 minimum to -4.05 maximum V dc
V _{EE1} (ECL 10K)	CML supply voltage- - - -	-5.72 minimum to -4.68 maximum V dc
T _C	Case operating temperature-	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification, standard, and publications required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Other publications. The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted shall be those listed in the issue of the DODISS specified in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS shall be the issue of the nongovernment documents which is current on the date of the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 12-X - Bipolar Gate Array Macrocell Standard.
 JEDEC Standard No. 12 - Standard for Gate Array Benchmark Set.

(Applications for copies should be addressed to the Electronic Industries Association, 2001 Eye Street, N.W., Washington, DC 20006.)

(Nongovernment standards and other publications are normally available from the organizations which prepare or which distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Altered item drawing (AID) 1/requirements. The following items must be provided to the device manufacturer by the customer as part of an altered item drawing:

3.2.1 Terminal connections and pin assignments.

3.2.2 Package type selected from manufacturer's offering and in accordance with MIL-M-38510, appendix C (see 1.2.3).

3.2.3 Functional block diagram.

3.2.4 Functional description, terms, and symbols.

3.2.5 Logic diagram.

3.2.6 Pin function description.

3.2.7 Schematic circuits. The schematic circuits shall be in terms of the JEDEC Bipolar gate array macrocell standard (whenever possible). Until JEDEC documentation becomes available, the schematic circuits shall be in terms of a qualifying activity approved manufacturer bipolar gate array macrocell standard (whenever possible).

3.2.8 Test vectors. The test vectors must, as a minimum, detect 95 percent of all detectable single stuck-at-0 and stuck-at-1 faults. (An undetectable fault is defined here to be a fault for which it is shown that no test or set of tests can detect it. An example would be an unused output of a flip-flop.) The qualifying activity shall approve the particular fault simulator. The vectors shall be supplied on magnetic tape and shall be identified by test tape number and revision letter.

3.2.9 Device electrical performance characteristics. To include dc parametric (see table I herein for minimum requirements), ac functional and ac critical paths, as selected from the manufacturer data sheet. Electrical performance characteristics apply over the full recommended case operating temperature range.

3.2.10 Timing diagram. The timing diagram will show all critical interrelated inputs and outputs. Timing diagrams shall consist of one or more diagrams showing critical inter-relationships between two or more signals. Timing requirements such as set-up and hold times shall also be shown.

3.2.11 Burn-in circuit. The burn-in circuit shall be as specified on figure 1 herein for the AID device.

3.2.12 Maximum power dissipation. Per design.

3.3 Case outline. Case outline shall be as specified in MIL-M-38510 appendix C and 1.2.3 herein.

3.4 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.4.1 Silver-filled glass die attach. The use of silver-filled glass die attach material is allowed, subject to requirements as outlined in DESC-EQM letter 84-663, dated 16 May 84, entitled "Silver-Glass Die Attach Requirements MIL-M-38510, FSC 5962."

3.5 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510.

I/ An altered item drawing, (AID) contains all essential information (design, test, etc.) regarding a particular customer personalization of a gate array microcircuit.

3.6 Electrical performance characteristics. Each manufacturer shall submit to the qualifying activity a data sheet defining the gate array family being qualified. The data sheet shall contain all dc parametric, ac functional and parametric data and any other data which is manufacturer dependent but would be considered required by a design engineer. All devices, regardless of manufacturer must meet the minimum dc parameter limits in table I. All electrical performance characteristics apply over the full recommended case operating temperature range. (The Standard Evaluation Circuit (SEC; see 4.3.2.2) electrical performance characteristics are as specified in the AID for each manufacturer's SEC).

3.7 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups in table II herein. The electrical tests for each subgroup are described in the AID (for the user design) and in the AID for each manufacturer's SEC. The electrical test requirements shall as a minimum follow the requirements of figure 2 and table III herein.

3.8 Marking. The marking shall be in accordance with MIL-M-38510. The altered item drawing number shall be added to the marking by the manufacturer. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.9 Additional line certification requirements. In addition to the requirements of MIL-STD-976, the following documentation shall be provided to the qualifying activity for review approval. This documentation will remain on file for internal Government use only.

- a. Design/layout rules as a manufacturer's controlled document.
- b. A list of the macros in the manufacturer's macrocell library, macrocell performance data and macrocell simulation verification data (see 4.3.2.3). A description of the process used by the manufacturer for adding new macrocells to the library shall also be provided.
- c. Process control monitor design used by the manufacturer for qualification and wafer acceptance (see 4.3.2.1).
- d. Standard evaluation circuit implementation in the form of an AID (see 4.3.2.2 for discussion of this circuit) used by the manufacturer for qualification and quality conformance inspection (SEC design details, test vectors, and all required information will be contained in the AID for each manufacturer's SEC).
- e. JEDEC gate array benchmark set (see appendix A and 4.3.2.4) delay simulation data.
- f. A list of the software packages (including names and current version) used by the manufacturer in the gate array design process.
- g. Design Rule Check (DRC) and Electrical Rule Check (ERC) software verification. The manufacturer's DRC and ERC software shall be run on a design which contains known rule violations; the output shall be presented to the qualifying activity and must show the violations were flagged.
- h. Layout Versus Schematic (LVS) checker. Manufacturer must demonstrate the effectiveness of the LVS software.
- i. Fault simulators, used for qualification.

3.10 Functional delay simulation. To be retained by manufacturer; simulation to be derived from each final application specific electrical design and layout (i.e., post-routed design). Simulation shall be done using actual delays as computed from the placement and layout of the device as it will be fabricated. Actual delays shall include the contribution associated with the delay through the gate, as well as the contribution due to actual metal capacitance and loading on the output(s). Using these actual delays, the application specific designer shall insure that there are no timing violations remaining in the circuit. Such timing violations shall include, but not be limited to, setup, hold, critical delay path and circuit race conditions due to variations in process, temperature and supply voltage. The simulated circuit behavior at the two (fast and slow) worst case extremes of temperature, supply voltage, and process shall be identical states at the specified strobe time (usually at the end of a typical clock cycle where all signals are stable).

3.11 Layout verification. The manufacturer shall retain the results of full, mask level design rule checks, electrical rule checks and connectivity checks for each application specific design. Rule checking will encompass the rules set provided under 3.9a herein. The manufacturer will explain any rules not checked and all error reports produced by the checker. The LVS check will ensure that the layout matches exactly the logic schematic simulated by the application specific integrated circuit (ASIC) designer.

3.12 Power routing simulation 2/. To be retained by organization performing the simulation; derived from each final application specific electrical design and layout. The worst case simulation of power busses shall show that at no time shall the localized bus current density exceed specification for allowable current density of the power bus material as defined in MIL-M-38510. In addition, at no point in the power bus shall voltage levels exceed recommended IR drop values from the respective supply. Power routing simulation must be based upon actual placement of cells within the array. Such a simulation may be driven by Monte Carlo methods, or in conjunction with a digital event driven simulator using the selected set of test vectors.

3.13 Procedure for updating certified software packages. Each manufacturer shall submit to the qualifying activity for review the procedure used for approval of updates and revisions of certified software packages (see 3.9f). This procedure shall outline the method and provide test descriptions regarding the process used to accept/reject updates and revisions to in-house or commercially supplied software packages. This requirement only applies to software packages used by the manufacturer in the gate array design process.

2/ A manufacturer may take an alternate path for qualification of the specific gate array family members without accounting for specific uses of the array. Such a qualification would be a worst case simulation of each gate array family member by populating all cell positions with the worst case power consumption cells (100 percent utilization). Such a simulation must switch all transistors simultaneously at maximum rated frequency and operating voltage. The contribution to the current density from the output buffers should reflect a TTL load capacitance of 50 picofarad, as well as the TTL dc load current and an ECL termination of 50 ohms to minus 2 volts from V_{CC} .

TABLE I. DC electrical performance characteristics. 1/ 2/

Test	Symbol		Conditions	Limits		Unit
				Min	Max	
High level output voltage	V_{OH}	TTL	$I_{OH} = -2 \text{ mA}$	2.4		V
Low level output voltage	V_{OL}	TTL	$I_{OL} = 2.4 \text{ mA}$		0.4	V
High level input voltage	V_{IH}	TTL			0.8	V
Low level input voltage	V_{IL}	TTL		2.0		V
Input current	I_{IN}	TTL	$V_{IN} = V_{CC}$	-1	+1	μA
Three state output leakage current	I_{OZ}	TTL	$V_{IN} = V_{CC}$	-10	+10	μA

1/ This table comprises a core set of performance parameters; all product regardless of manufacturer, shall be within the specified limits.

2/ Limits apply for: $-55^{\circ}\text{C} \leq T_C \leq +125^{\circ}\text{C}$, $V_{CC} = 5 \text{ V} \pm 10\%$.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.1.1 Wafer lot acceptance procedure. Each manufacturer shall submit to the qualifying activity for approval a "Wafer lot acceptance procedure." This procedure shall outline and provide limits regarding the process used to accept/reject a wafer lot. The procedure shall include:

- a. Physical measurements of wafer metallization, glassivation, and gold backing in accordance with method 5007 of MIL-STD-883.
- b. Electrical measurements using the process monitor (PM) (Note: The PM may be dedicated drop-in or a set of structures in the kerf or scribe line).
- c. Visual inspection to include:
 1. High magnification examination on a sample basis.
 2. Optical test structures to insure alignment, etc.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1, 7	1, 7
Final electrical test parameters (method 5004)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, ^{1/} 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group B test requirements (method 5005, subgroup 5)	1, 2, 3, 7, 8, 9, 10, 11	N/A
Group C end-point electrical parameters (method 5005)	N/A	1, 2, 3, 7
Group D end-point electrical parameters (method 5005)	1, 2, 3, 7	1, 2, 3, 7
Additional electrical tests for group C inspection	N/A	N/A

^{1/} PDA applies to subgroups 1 and 7 (see 4.2c).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test (method 1015 of MIL-STD-883).
 1. Test condition A or B, using the circuit configuration shown on figure 1.
 2. $T_A = +125^\circ\text{C}$ minimum.
- b. Interim and final electrical tests shall be as specified in table II herein, except interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.
- c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510 except the PDA for class B shall be 10 percent.
- d. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.3 Qualification inspection.

4.3.1 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510, and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). In addition, the five-phased qualification outlined as follows shall be performed through the use of the identified qualification vehicles.

4.3.1.1 Qualification phase and vehicles.Qualification phase

Process control and stability
 Process reliability
 Macrocell design and simulation
 CAD routing and post routing simulation

Design check software verification

Qualification vehicles

Process monitor (PM)
 Standard evaluation circuit (SEC)
 Macro test chip set
 JEDEC Standard for Gate Array
 Benchmark Set
 Manufacturer test case

Note: Qualification of the Macrocell design and simulation and CAD and post routing simulation will be based on the manufacturer's ability to design, place and route, and manufacture devices where actual measured performance characteristics (i.e., propagation delays, rise and fall times, drive characterization, trigger levels, etc.) are within simulated device performance limits (see 4.3.2.4).

4.3.2.1 Process control and stability. Process control and stability of dc parameters must be demonstrated through the use of the manufacturer's process monitor (PM). The PM (either a dedicated drop-in or structures fabricated in the kerf) shall be designed so that the dc process parameters (ac parameters may be included as a manufacturer's option) may be measured in wafer form or packaged device form. The PM design must be submitted to the qualifying activity for approval prior to use for qualification and must contain as a minimum the following structures:

- a. npn and pnp minimum device.
- b. npn and pnp large device.
- c. Sheet resistance measurement structure.
- d. Metal step coverage structure.
- e. Intermetal oxide integrity structure.
- f. Contact chains (to be of sufficient length to be representative of the contact resistance).
 - (1) Metal 1 to metal 2 (where applicable).
 - (2) Metal 2 to metal 3 (where applicable).
 - (3) Metal to poly (where applicable).
 - (4) Metal to diffusion (where applicable).
 - (5) Gated inverter chains (for ac measurement; may be included as a manufacturer's option).

For qualification, PM's on a minimum of three different lots (minimum of 4 PM's per wafer) shall be measured to insure the establishment of a statistically valid data base on which a decision can be made as to whether the manufacturer's process is stable and under control. Recent lot history data can be used to satisfy this requirement. (For quality conformance inspection, measurement of PM parameters will be required in accordance with method 5007 of MIL-STD-883 for wafer lot acceptance, see 4.1.1.)

4.3.2.2 Process reliability. The process reliability is to be qualified using the manufacturer's SEC. The SEC design shall be submitted to the qualifying activity for approval prior to use in the form of a manufacturer's altered item drawing, and as such shall contain the basic information as detailed in sections 3.2.1 through 3.2.10. It shall be fabricated with the same process that will produce any application specific gate array device under this detail specification. The SEC design shall be configured in such a manner so as to evaluate the reliability of the underlayer designs (diffusions, etc.) and evaluate worst case design rule conditions on the personalization layers. The design should utilize library macrocells as well as test structures which will detect metal to metal shorting or opening, high via resistance and dielectric pinholes during reliability life testing. The SEC shall be implemented on the largest member (i.e., The device type with the largest number of

gates and if applicable with the highest pin count package) of the gate array family. Smaller gate count members of the gate array family in the highest pin count package or in smaller pin count packages may be qualified by extension (see 4.3.3).

The SEC will also be the main qualification vehicle for the electrical testing which follows (see 4.4.1, 4.4.2, 4.4.3 and 4.4.4). Test limits appear in the AID (see table I herein for minimum dc parameters) for each manufacturer's SEC. The electrical test for each subgroup shall be described in table III herein. The SEC shall be suitable for both static and dynamic biased aging, as life testing will be performed on this device (see 4.4.3).

4.3.2.3 Macrocell design and simulation qualification. The macrocell design and simulation qualification shall be accomplished in a two step procedure consisting of parameter verification/ simulation verification and functional verification.

A chip shall be designed to provide access to a set of macrocells to test performance characteristics. These macrocells are a subset of the JEDEC Standard No. 12-X "Bipolar Gate Array Macrocell Standard;" macrocells substitutions are allowable only if the manufacturer does not offer a particular macrocell, and such substitutions must be approved by the qualifying activity. The set of macrocells shall include:

<u>Macrocell(*)</u>	<u>Description</u>
JIV1	Inverter
JND4	4-input NAND
JA012	2-input AND into 3-input NOR
JLDR1	D latch with active low reset
JFJKR1	JK flip-flop with active low reset
JBIT1	TTL input buffer
N/A	ECL input buffer
JB01	Output buffer
JBTB2	3 state I/O buffer with pull-up

(*) JEDEC naming convention

The intent is to get a representative cross section of macrocell types (i.e., combinational, sequential, input, output). Chains shall be formed (when necessary to avoid rise and fall time measurement problems) and actual performance data over the full operating range shall be taken (a provision to extract for multiplexing and I/O buffer delay shall be included). Delay versus metal wire length and fanout for the above macrocells shall be determined. The actual performance data shall be submitted to the qualifying activity along with computer program simulation results. The actual performance data must be within the limits predicted by the simulation. If multipliers are used to extrapolate performance at the temperature extremes, such multipliers shall be verified as well.

In addition, for the above macrocells, a set of pins shall be provided on the test chip for observability. This will enable verification of functionality of the macrocells (inputs and outputs may be multiplexed).

4.3.2.4 CAD routing and post routing simulation. A chip or set of chips incorporating the JEDEC standard for gate array benchmark set shall be used to qualify the manufacturer's ability to perform routing and to accurately predict post routing performance. The manufacturer must submit to the qualifying activity:

- a. The actual measured performance data for each function in the benchmark over temperature and voltage.
- b. The computer simulation performance prediction. The two results will remain on file and the actual measured performance must fall between the two worst case (i.e., fast worse case $V_{CC} = 4.5$ V at -55°C and slow worse case $V_{CC} = 5.5$ V at $+125^{\circ}\text{C}$) simulation performance prediction limits.

4.3.2.5 Design check software verification. The manufacturer shall verify that the DRC, ERC, and LVS software is capable of performing the intended function. This shall be accomplished by running a design with known errors against the design check software and demonstrating that the errors were caught.

4.3.3 Qualification extension. For qualification inspection if a manufacturer qualifies the SEC (i.e., the highest gate count array) in the highest pin count package type, then lower gate count arrays in that package, type, that are manufactured identically (i.e., same line, same process) as the SEC may be part I qualified upon approval of the qualifying activity.

- a. Lower gate count arrays in lower pin count packages that are manufactured identically (i.e., same line, same process) as the SEC may be part I qualified upon the approval of the qualifying activity using another die, provided the gate utilization is 60 percent or greater and by conducting group A electrical tests and any electrical subgroups, if required by qualifying activity on lower pin count packages, added to group C tests in table II herein for the die extension.
- b. Package extension may be achieved by performing subgroups 2, 3, 4, 5, and 7 of group B tests and all group D tests of method 5005 of MIL-STD-883 for the package extension. Data for qualification extension must be submitted in accordance with appendix D of MIL-M-38510.

4.4 Quality conformance inspection. Quality performance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 and 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

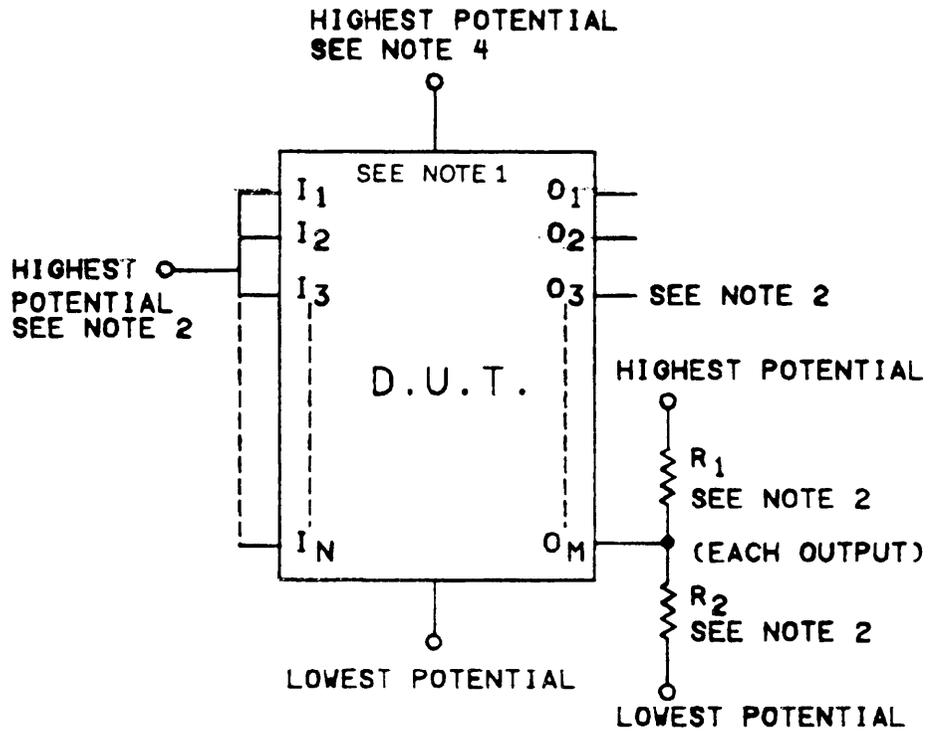
- a. Test requirements shall be specified in table I herein and as follows:
- b. The vehicles to be used for the group A inspection are as follows:
 - (1) Qualification: Standard evaluation circuit.
 - (2) Quality conformance inspection: Actual user device (via the altered item drawing).
- c. Subgroups 4, 5, and 6 of table I of method 5005, of MIL-STD-883 shall be omitted.
- d. AC and functional testing shall be performed using the circuit configuration shown on figure 2 herein or equivalent.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical test requirements shall be as specified in table II herein, and as follows:

- a. The vehicles to be used for the group B inspection are as follows:
 - (1) Qualification: Standard evaluation circuit.
 - (2) Quality conformance inspection: Actual user device (via the altered item drawing).

4.4.3 Group C inspections. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

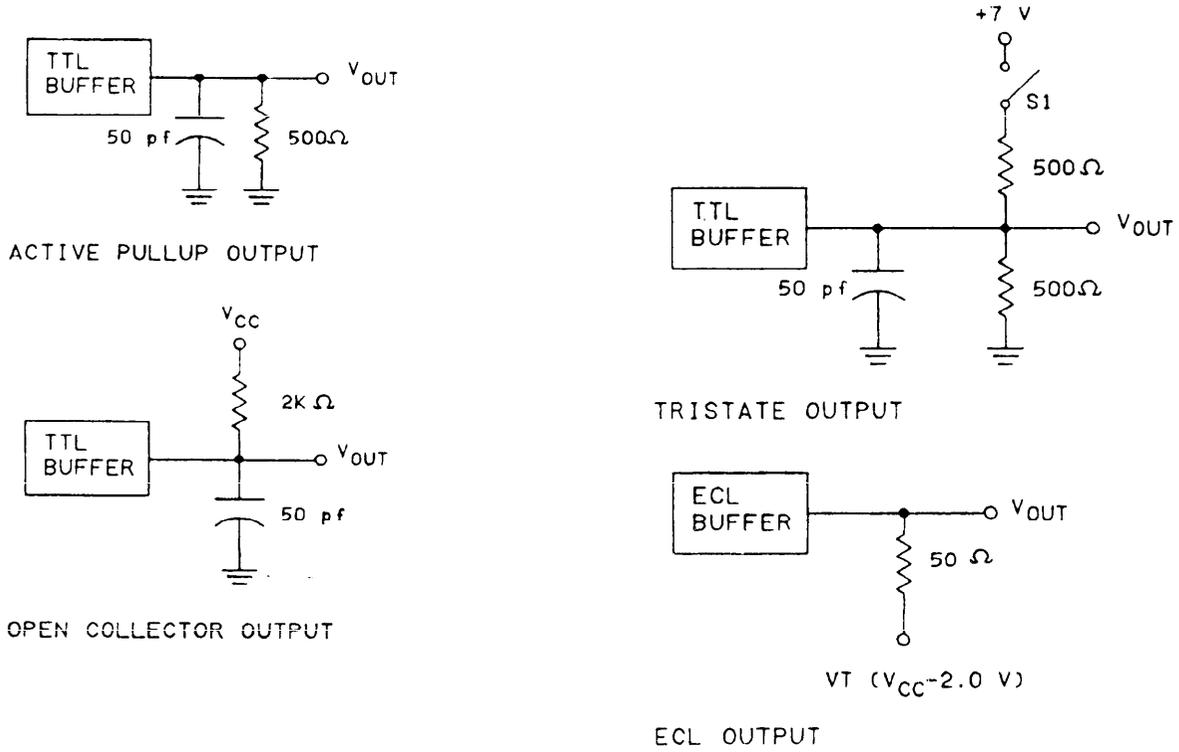
- a. Qualification and quality conformance inspection shall be performed on the manufacturer's SEC.
- b. End point electrical parameters shall be as specified in table II with limits shown in the AID covering the manufacturer's SEC (see table I herein for minimum dc parameters).



NOTES:

1. I = input, O = output, N (M) = highest numbered input (output).
2. For class B, all inputs are connected to the highest potential outputs are connected through load resistors to the highest and lowest potentials. The value of the resistors shall be chosen so as not to overstress the output buffer beyond its current sourcing/sinking.
3. Pin designations determined by customer configuration.
4. In the case of multiple power pins, all connections shall be tied to the appropriate level.

FIGURE 1. Burn-in circuit (device specific).



Test	Switch S_1
t_{PDZH}	Open
t_{PDZL}	Closed
t_{PDHZ}	Open
t_{PDLZ}	Closed
t_{PDLH}	Open
t_{PDHL}	Open

FIGURE 2. AC load circuit configuration.

TABLE III. Group A inspection for all device types. 1/

Subgroup	Test	Symbol	Test No.	MIL-STD-883 method	Conditions	Measured terminal	Limit
1 $T_C = +25^\circ\text{C}$	Input clamp voltage, positive	$V_{IC, POS}$	1	---	$V_{CC} = GND$; 1 mA into terminal	All input terminals	Per manufacturer data
	Input clamp voltage, negative	$V_{IC, NEG}$	2	---	$GND = V_{SS}$; -1 mA into terminal	All input terminals	Per manufacturer data
	Output voltage high, TTL	V_{OH}	3	3006	$V_{CC} = 4.5\text{ V}$	All output terminals	See table I
	Output voltage low, TTL	V_{OL}	5	3007	$V_{CC} = 4.5\text{ V}$	All output terminals	"
	Input current, high	I_{IH}	7	3010	$V_{CC} = 5.5\text{ V}$; input voltage = 5.5 V	All input terminals	"
	Input current, low	I_{IL}	8	3009	$V_{CC} = 5.5\text{ V}$; input voltage = 0.0 V	All input terminals	"
	Static supply current	I_{CCS}	9	3005	$V_{CC} = 5.5\text{ V}$	V_{CC} terminal	Per design
2 $T_C = +125^\circ\text{C}$	Same terminal conditions and limits as above, except $T_C = +125^\circ\text{C}$.						
3 $T_C = -55^\circ\text{C}$	Same terminal conditions and limits as above, except $T_C = -55^\circ\text{C}$.						
7 $T_C = +25^\circ\text{C}$	Functional	---	See figure 3	3014	Design specific, according to AID $V_{CC} = 4.5\text{ V}$		
8	Same as subgroup 7, except $T_C = +125^\circ\text{C}$ and -55°C .						
9 $T_C = +25^\circ\text{C}$	AC switching	---	See figure 3	3003	Design specific, according to AID $V_{CC} = 5.0\text{ V}$		
10 $T_C = +125^\circ\text{C}$	Same as subgroup 9, except $T_C = +125^\circ\text{C}$.						
11 $T_C = -55^\circ\text{C}$	Same as subgroup 9, except $T_C = -55^\circ\text{C}$.						

1/ Static tests shall be conducted as required by table II of this specification; limits and conditions appear in table I herein. Particular terminal(s) to be measured are design specific and must appear in the applicable AID.

2/ Switching tests, comprising subgroups 9, 10, and 11, shall be conducted as required by table II. The test vectors to accomplish the functional and switching verification are design specific, and must be included in the AID. The vector set must meet the criteria as outlined in 3.2.8. Limits appear in the AID.

c. Steady state life test (method 1005 of MIL-STD-883).

- (1) Use life-test condition A or B using the SEC and the circuit configurations shown on figure 1. The life test circuit schematic shall be submitted to the qualifying activity for approval prior to use.
- (2) Test duration 1,000 hours, except as permitted in appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.
- (3) $T_A = +125^\circ\text{C}$ minimum.

d. The following sample plan shall be used in lieu of table III of method 5005 for all group C subgroups: A sample of 10 SEC devices shall be chosen and submitted to test with no failures allowed. If not more than one failure is found in the first sample of 10, a second sample of 10 SEC devices is permitted with no further failures allowed.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End point electrical parameters shall be as specified in table II herein. The SEC shall be used for group D inspection whenever practical; for a smaller package where the SEC cannot be used, another die may be used provided the gate utilization is 60 percent or greater. Group D inspection shall be performed in accordance with MIL-M-38510, 4.5, except as defined below:

- a. If more than one package type within a case outline family is qualified, then the group D inspection shall be rotated between the qualified package types. A different package type shall be tested every three months based on the inspection lot date code.
- b. If a package type is skipped in the rotation due to the absence of production, then the first lot of the skipped type shall receive group D inspection. The successful completion of this package type shall establish a new three month period before the next package type in the rotation is selected for group D inspection.
- c. Failure of a group D subgroup shall discontinue coverage of all package types within the case outline family. Lot by lot inspection shall be initiated until three consecutive lots pass. The package type which failed the subgroup shall not be shippable until that package type has successfully passed the previously failed subgroup.

4.4.5 Constant acceleration. The constant acceleration tests of groups C and D shall be performed using test condition D.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. In addition, all devices shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications (original equipment), design applications, and logistic purposes.

6.2 Ordering data.

6.2.1 Acquisition requirement. Acquisition documents shall specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirements for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.
- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable.
- h. Requirements for "JAN" marking.
- i. Requirements for altered item drawing provided to the manufacturer (see 3.2).

6.4 Logistic support. Lead material and finish (see 3.5), are interchangeable. Unless otherwise specified, microcircuits acquired for government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.5). Longer length leads and lead forming shall not affect the part number.

6.5 Manufacturers' designations. Manufacturers of device types on this specification are designated in table V herein. This does not imply qualification or certification, refer to QPL-38510 for information regarding qualified sources.

TABLE V. Manufacturers' designations.

Device type	A	B
	Honeywell	ATT

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Manufacturer specific generic-industry type</u>
01, 02, and 03	See listed manufacturer data sheets (6.5)

APPENDIX A

Gate Array Benchmark Set

10. SCOPE

10.1 Scope. This appendix contains benchmark description numbers from the JEDEC Standard for Gate Array Benchmark Set as required by 4.3.2.4 CAD routing and post routing simulation herein.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. REQUIREMENTS

30.1 Benchmark number description.

- 1 4 bit ALU, similar to 54S381
- 2 16 bit ALU, similar to 54S381
- 3 4 bit rotater
- 4 16 bit rotater
- 5 8 bit register
- 6 8 bit up/down counter
- 7 3 to 8 decoder, similar to 54S138
- 8 9 bit parity generator, similar to 54S280

Custodians:

Air Force - 17
Navy - EC
Army - ER

Review activities:

Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:

Army - SM
Navy - AS, CG, MC

Preparing activity:

Air Force - 17

Agent:

DLA - ES

(Project 5962-0876)

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(See Instructions - Reverse Side)

1. DOCUMENT NUMBER
MIL-M-38510/600

2. DOCUMENT TITLE MICROCIRCUITS, DIGITAL, BIPOLAR, SEMICUSTOM
(GATE ARRAY) DEVICES, MONOLITHIC SILICON

3. NAME OF SUBMITTING ORGANIZATION

4. TYPE OF ORGANIZATION (Mark one)

VENDOR

USER

MANUFACTURER

OTHER (Specify): _____

5. ADDRESS (Street, City, State, ZIP Code)

5. PROBLEM AREAS

a. Paragraph Number and Wording:

b. Recommended Wording:

c. Reason/Rationale for Recommendation:

5. REMARKS

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b. WORK TELEPHONE NUMBER (Include Area Code) - Optional

c. MAILING ADDRESS (Street, City, State, ZIP Code) - Optional

8. DATE OF SUBMISSION (YYMMDD)