

INCH-POUND

MIL-M-38510/530A
16 September 1994
SUPERSEDING
MIL-M-38510/530(USAF)
10 November 1980

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, N-CHANNEL, SILICON GATE
MONOLITHIC 16-BIT MICROPROCESSOR (FIXED INSTRUCTION)

This specification is approved for use by all Departments and
Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic NMOS, silicon gate microprocessor. Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete Part or Identifying Number (PIN).

1.2 Classification.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit</u>
01	16-bit, fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be as designated in MIL-STD-1835 and as follows:

<u>Letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
Q	GDIP1-T40 or CDIP2-T40	40	dual-in-line package

1.3 Absolute maximum ratings.

V_{CC} supply voltage range ($V_{CC} - GND$)	-1.0 V to +7.0 V
Input voltage range	-1.0 V to +7.0 V
Storage temperature range	-65°C to +150°C
Power dissipation for package	2.5 W
Power dissipation for device type 01:	
$T_C = -55^\circ\text{C}$	2.3 W
$T_C = 125^\circ\text{C}$	1.6 W
Lead temperature (soldering, 5 seconds)	270°C
Maximum junction temperature	150°C
Thermal resistance, junction-to-case (θ_{JC})	13°C/W

1.4 Recommended operating conditions.

Supply voltage Range (V_{CC})	+4.5 V to +5.5 V
High-level input voltage:	
Logic inputs, (V_{IH1})	2.2 V to ($V_{CC} + 0.5$ V)
Clock input, (V_{IH2})	3.9 V to ($V_{CC} + 1.0$ V)

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: DESC-ELD 1507 Wilmington Pike, Dayton, Ohio 45444-5765, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A

FSC 5962

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1.4 Recommended operating conditions. - continued

Low-level input voltage:

Logic inputs, (V _{IL1})	- - - - -	-0.5 V to 0.6 V
Clock input, (V _{IL2})	- - - - -	-0.5 V to 0.6 V
Frequency of operation	- - - - -	2 MHz to 5 MHz
Case operating temperature range	- - - - -	-55°C to +125°C
Clock rise time (from 1.0 V to 3.5 V)	- - - - -	10 ns
Clock fall time (from 3.5 V to 1.0 V)	- - - - -	10 ns

2. APPLICABLE DOCUMENTS

2.1 Issues of documents. The following documents, of the issue in effect on date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, drawings, and publications required by contractors in connection with specific procurement functions should be obtained from the procuring activity or as directed by the contracting officer.)

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be as specified in 1.2.3 herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II.

3.6 Microprocessor instructions. Microprocessor instructions shall be as specified in table III.

3.7 Marking. Marking shall be in accordance with MIL-M-38510.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in a microcircuit group number 107 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. Burn-in test, method 1015 of MIL-STD-883.
 1. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 2. $T_A = +125^\circ\text{C}$, minimum.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

- a. Tests shall be as specified in table II.
- b. Subgroup 4 (C_0 , C_{11} , C_{12} measurement) shall be performed only for initial qualification and after process or design changes which may affect device capacitance. Test 5 devices with zero failures. The measurement shall be made between the indicated terminal and ground at a frequency of 1 MHz.
- c. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- d. Subgroups 7 and 8 functional testing shall include verification of the instruction set, table III.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

- a. Class S steady-state life (accelerated) shall be conducted using test condition D, method 1005 of MIL-STD-883.
- b. End-point electrical parameters shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III, of method 5005 of MIL-STD-883 and as follows:

- a. Steady-state life test, method 1005, of MIL-STD-883.
 - (1). Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
 - (2). $T_A = +125^\circ\text{C}$, minimum.
- b. End-point electrical parameters shall be as specified in table II herein.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C Unless otherwise specified 1/	Group A subgroups	Limits		Unit
				Min	Max	
Output high voltage	V _{OH}	I _{OH} = -400 μA, V _{CC} = 4.5 V See figure 3	1, 2, 3	2.4		V
Output low voltage	V _{OL}	I _{OL} = 2.0 mA, V _{CC} = 4.5 V See figure 3	1, 2, 3		0.45	V
Input low voltage (except CLK, MN/MX)	V _{IL1}	2/	1, 2, 3	-0.5	+0.6	V
Input high voltage (except CLK, MN/MX)	V _{IH1}	2/	1, 2, 3	2.2	V _{CC} +0.5	V
Clock input low voltage	V _{IL2}		1, 2, 3	-0.5	+0.5	V
Clock input high voltage	V _{IH2}		1, 2, 3	3.9	V _{CC} +1.0	V
Power supply current	I _{CC}	V _{CC} = 5.5 V	1, 2, 3		340	mA
Input low current (NMI, INTR, CLK, RESET, READY, TEST, MN/MX)	I _{IL1}	V _{IN} = 0.0 V, V _{CC} = 5.5 V	1, 2, 3	-10	10	μA
Input high current (NMI, INTR, CLK, RESET, READY, TEST, MN/MX)	I _{IH1}	V _{IN} = 5.5 V, V _{CC} = 5.5 V	1, 2, 3	-10	10	μA
Input low current (AD ₀₋₁₅)	I _{IL2}	V _{CC} = 5.5 V, V _{IN} = 0.45 V	1, 2, 3	-10	10	μA
Input high current (AD ₀₋₁₅)	I _{IH2}	V _{CC} = 5.5 V, V _{IN} = 2.4 V	1, 2, 3	-10	10	μA
High impedance state leakage current (A/S, BHE, /S ₇ , RD, DEN (S ₀), DT/R(S ₁), M/IO(S ₂), WR (LOCK))	I _{ZL1}	V _{CC} = 5.5 V, V _O = 0.45 V	1, 2, 3	-10	10	μA
	I _{ZH1}	V _{CC} = 5.5 V, V _O = 2.4 V	1, 2, 3	-10	10	μA
Capacitance of input buffer (all input except AD ₀₋₁₅), RQ/GT	CI ₁	See 4.4.1b	4		15	pF
Capacitance of I/O buffer (AD ₀₋₁₅), RQ/GT	CI ₂	See 4.4.1b	4		15	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics.-continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	MAX	
Capacitance of three state outputs (A/S, BHE/S ₇ , RD, DEN(S ₀), DT/R(S ₁), M/TO(S ₂), WR(LOCK))	C _O	See 4.4.1b	4		15	pF
Functional test		See 4.4.1d	7, 8			
CLK cycle period	t _{CYC}	V _{CC} = 4.5 V See figure 4	9, 10, 11	200	500	ns
CLK low time	t _{PWL1}		9, 10, 11	2/3(t _{CYC})-15		ns
CLK high time	t _{PWH1}		9, 10, 11	1/3(t _{CYC})+2		ns
Data set up time to CLK ↓ EDGE	t _{SZH} t _{SZL}		9, 10, 11	30		ns
Data in hold time from CLK ↓ EDGE	t _{HHZ} t _{HLZ}		9, 10, 11	10		ns
Ready setup time to CLK ↑ EDGE	t _{SLH1}		9, 10, 11	2/3(t _{CYC})-15		ns
Ready hold time to CLK ↑ EDGE	t _{HHL1} t _{HLH1}		9, 10, 11	30		ns
Request (RQ/GT) hold time from CLK ↑ EDGE	t _{HLH2}		9, 10, 11	40		ns
Request (RQ/GT) setup time to CLK ↑ EDGE	t _{SHL2}		9, 10, 11	30		ns
Ready active to status passive. Applies to T3 and WAIT states (S ₀ -S ₂)	t _{PLH1}		9, 10, 11		110	ns
Status active delay from CLK ↑ EDGE (S ₀ -2)	t _{PHL2}		9, 10, 11	10	110	ns
Status inactive delay from CLK ↓ EDGE (S ₀ -2)	t _{PLH2}		9, 10, 11	10	130	ns
Address valid delay from CLK ↓ EDGE (AD ₀ -15, A16/S ₃ - A19/S ₆)	t _{PHL3} t _{PLH3}		9, 10, 11	10	110	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.-continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Control valid delay from CLK ↓ EDGE (BHE/S ₇ , QS ₁ , O LOCK)	t _{PHL4} t _{PLH4}	V _{CC} = 4.5 V See figure 4	9, 10, 11	10	110	ns
Address invalid delay from CLK ↓ EDGE (AD ₀₋₁₅ , A16/S ₃ -A19/S ₆)	t _{PHL5} t _{PLH5}		9, 10, 11	10		ns
$\overline{\text{BHE/S}}_7$ invalid delay from CLK ↓ EDGE	t _{PHL6} t _{PLH6}		9, 10, 11	10		ns
Address float delay from CLK ↓ EDGE	t _{PHZ1} t _{PLZ1}		9, 10, 11	t _{PHL5}	80	ns
Data valid delay from CLK ↓ EDGE (AD ₀₋₁₅)	t _{PHL7} t _{PLH7}		9, 10, 11	10	110	ns
Status valid delay from CLK ↓ EDGE (BHE/S ₇ , A16/S ₃ , A19/S ₆)	t _{PHL8} t _{PLH8}		9, 10, 11	10	110	ns
Data invalid delay from CLK ↑ EDGE (AD ₀₋₁₅)	t _{PHZ2} t _{PLZ2}		9, 10, 11	10	110	ns
Status invalid delay from CLK ↑ EDGE (BHE/S ₇ , A16/S ₃ , A19/S ₆)	t _{PHL9} t _{PLH9}		9, 10, 11	10		ns
Address float to read active	t _{PHL22}		9, 10, 11	0		ns
$\overline{\text{RD}}$ active delay from CLK ↓ EDGE	t _{PHL10}		9, 10, 11	10	165	ns
$\overline{\text{RD}}$ inactive delay from CLK ↓ EDGE	t _{PLH10}		9, 10, 11	10	150	ns
$\overline{\text{RD}}$ inactive to next address active	t _{PZH} t _{PZL}		9, 10, 11	t _{CYC} -45		ns
Grant ($\overline{\text{RQ/GT}}$) active delay from CLK ↓ EDGE	t _{PHL11}		9, 10, 11	0	85	ns
Grant (RQ/GT) inactive delay from CLK ↓ EDGE	t _{PLH11}		9, 10, 11	0	85	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics-continued

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 1/ Unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
$\overline{\text{RD}}$ width	t _{PWL2}	V _{CC} = 4.5 V See figure 4	9, 10, 11	2t _{CYC} -75		ns
$\overline{\text{WR}}$ width	t _{PWL3}		9, 10, 11	2t _{CYC} -60		ns
Hold setup time CLK ↑ EDGE	t _{SHL4} t _{SLH4}		9, 10, 11	35		ns
INTR, NMI, $\overline{\text{TEST}}$ setup time setup req. for asynchronous signal only to CLK ↑ EDGE	t _{SHL4} t _{SLH4}		9, 10, 11	30		ns
ALE width	t _{PWH4}		9, 10, 11	t _{PWL1} -20		ns
ALE active delay from CLK ↓ EDGE	t _{PLH12}		9, 10, 11	0	80	ns
ALE inactive delay from CLK ↑ EDGE	t _{PHL12}		9, 10, 11		85	ns
ALE inactive to AD ₀ -AD ₁₅ inactive (RD cycle)	t _{PHZ3} t _{PLZ3}		9, 10, 11	t _{PWL1} -10		ns
ALE inactive to $\overline{\text{BHE}}/\text{S}_7$, A19/S ₆ - A16/S ₃ inactive	t _{PHL13} t _{PLH13}		9, 10, 11	t _{PWH1} -10		ns
Address valid to ALE low (AD 0-15, A16/S ₃ - A19/S ₆)	t _{PHL14}		9, 10, 11	t _{PWL1} -60		ns
$\overline{\text{BHE}}/\text{S}_7$ valid to ALE low	t _{PHL15}		9, 10, 11	t _{PWL1} -60		ns
Data inactive to WR inactive (AD ₀₋₁₅)	t _{PHZ4} t _{PLZ4}		9, 10, 11	t _{PWL1} -30		ns
$\overline{\text{WR}}$, $\overline{\text{INTA}}$, active delay from CLK ↓ EDGE	t _{PHL16}		9, 10, 11	10	110	ns
$\overline{\text{DT}}/\overline{\text{R}}$, M/IO active delay from CLK ↑ EDGE	t _{PHL17} t _{PLH17}		9, 10, 11	10	110	ns

See footnotes at end of table.

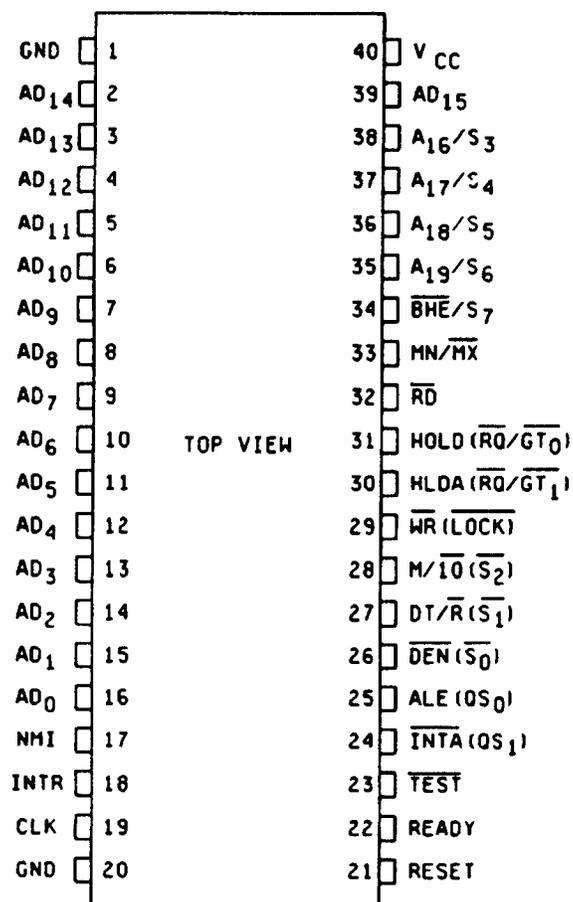
TABLE I. Electrical performance characteristics-continued

Test	Symbol	Conditions 1/ -55°C ≤ T _c ≤ +125°C Unless otherwise specified	Group A Subgroups	Limits		Unit
				Min	Max	
Control inactive delay 1 from CLK ↓ EDGE (DEN, INTA, WR)	t _{PLH23}	V _{CC} = 4.5 V See figure 4	9, 10, 11	10	110	ns
Control inactive delay 3/ from CLK ↑ EDGE (DEN during write cycle)	t _{PLH24}		9, 10, 11	10	110	ns
HLDA valid delay from CLK ↓ EDGE	t _{PHL18} t _{PLH18}		9, 10, 11	10	160	ns
ALE inactive to AD ₀ -AD ₁₅ inactive (WR cycle)	t _{PHL19} t _{PLH19}		9, 10, 11	t _{PWH1} -10		ns
$\overline{\text{DEN}}$ active delay from CLK ↑ EDGE	t _{PHL20}		9, 10, 11	10	110	ns
Address delay 3/ from CLK ↓ EDGE	t _{PLH21} t _{PHL21}		9, 10, 11	t _{PHL5}		ns
Ready inactive setup time to CLK (applies to T2 state only)	t _{SHL1}		9, 10, 11	-8		ns

1/ All tests to be performed using worst case conditions unless otherwise specified.

2/ This parameter is guaranteed but not tested.

3/ This delay is for lines AD₀-AD₁₅, A19/S₆-A16/S₃, S₀-S₂, $\overline{\text{RD}}$, $\overline{\text{LOCK}}$, and $\overline{\text{BHE}}/S_7$ during request/grant and HOLD/HLDA sequences only.

DEVICE TYPE 01

Maximum mode pin functions (e.g; $\overline{\text{LOCK}}$) are shown in parentheses.

FIGURE 1. Terminal connections.

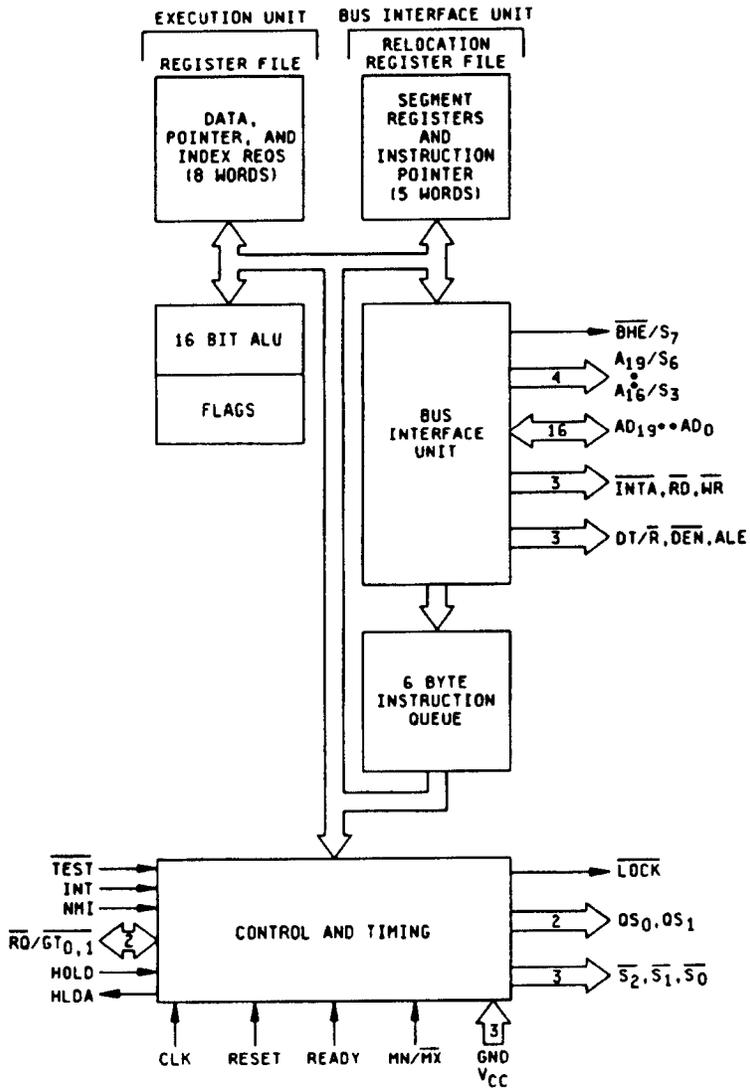


FIGURE 2. Functional block diagram.

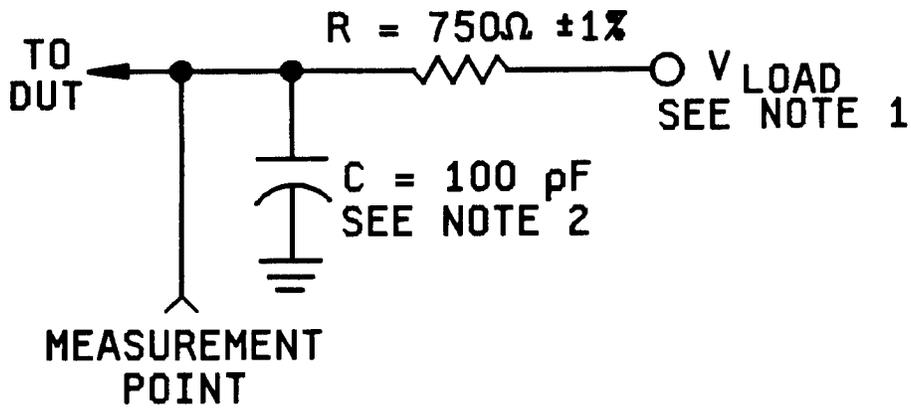
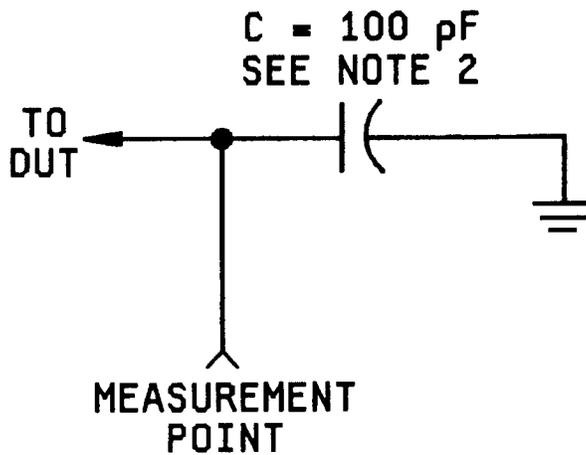


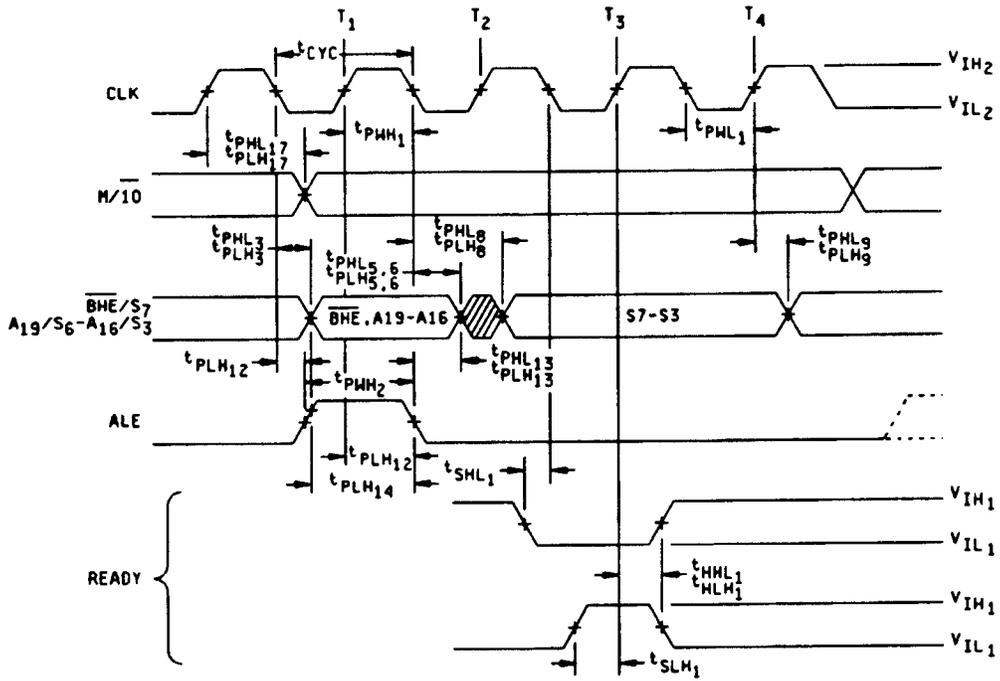
FIGURE 3. D.C. I/O Load.



NOTES:

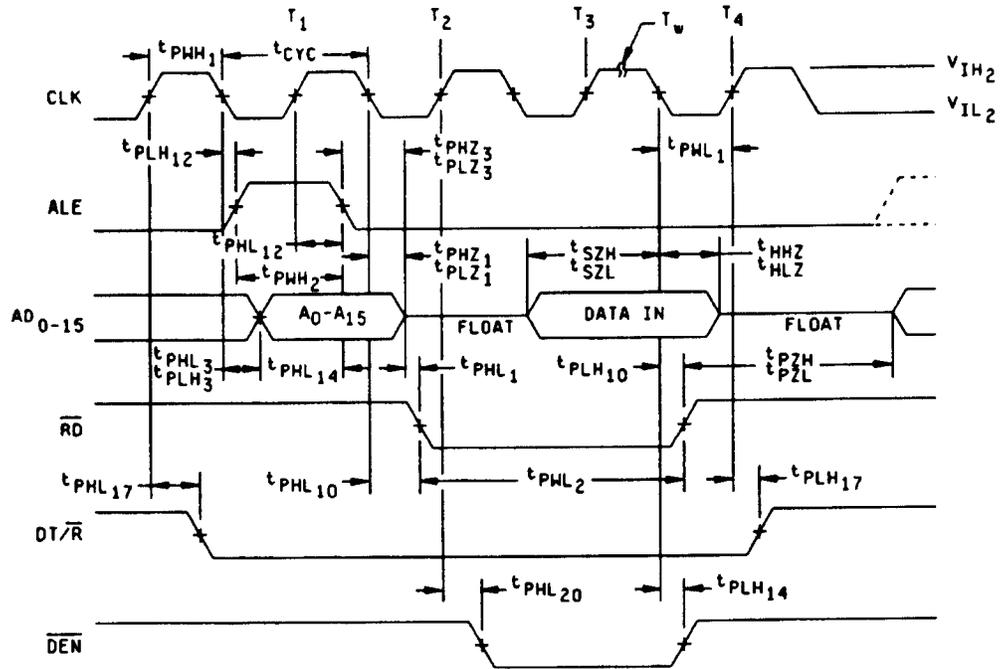
1. Loading used only during V_{OL} , V_{OH} tests. $V_{LOAD} = 0.3$ V for V_{OH} test, and $V_{LOAD} = 1.5$ V for V_{OL} test.
2. C includes tester, wiring and stray capacitance.

FIGURE 4. A.C. Load.



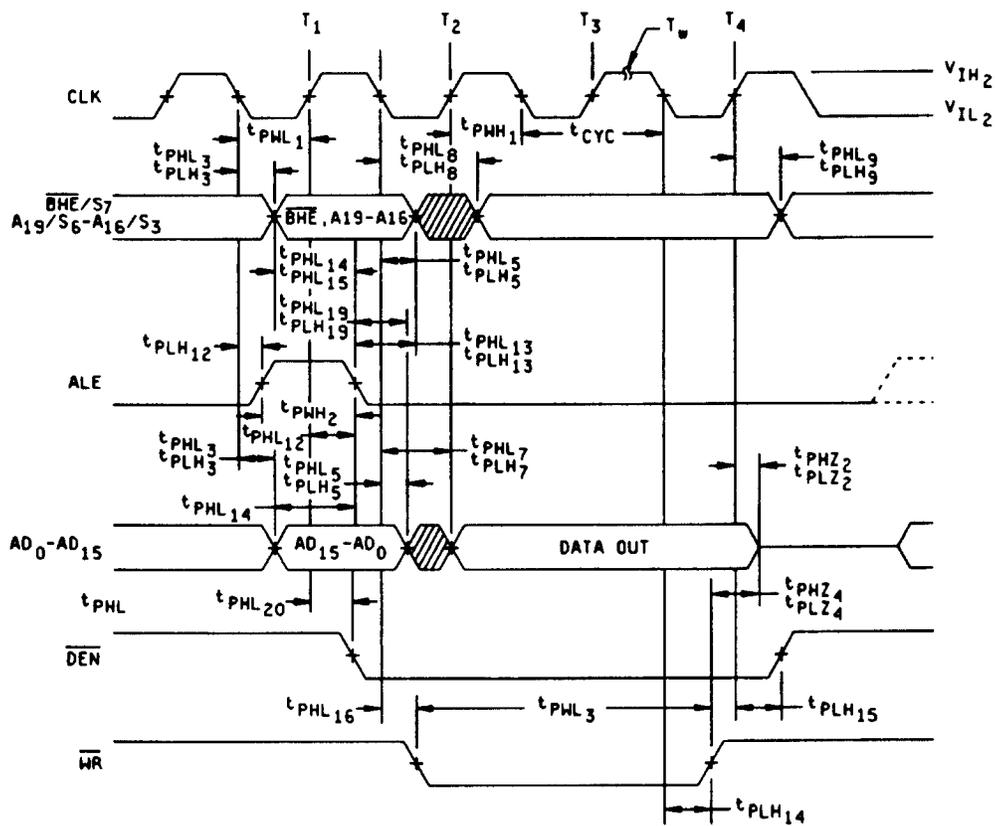
NOTE: All signals in figures 5, 6, 7, 8, 9, 10, 11, 12, and 13 switch between V_{OL} and V_{OH} unless otherwise specified.

FIGURE 5. Bus timing - minimum mode system.



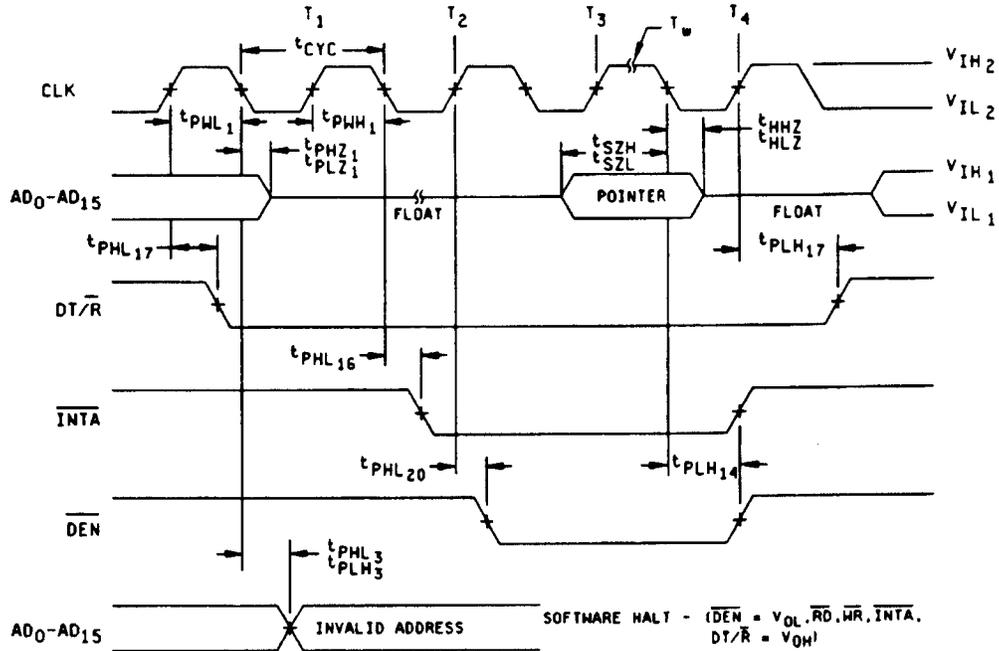
NOTE: \overline{WR} , \overline{INTA} = V_{OH} .

FIGURE 6. Bus timing - minimum mode - read cycle.



NOTE: \overline{RD} , \overline{INTA} , and $DT/\overline{R} = V_{OH}$.

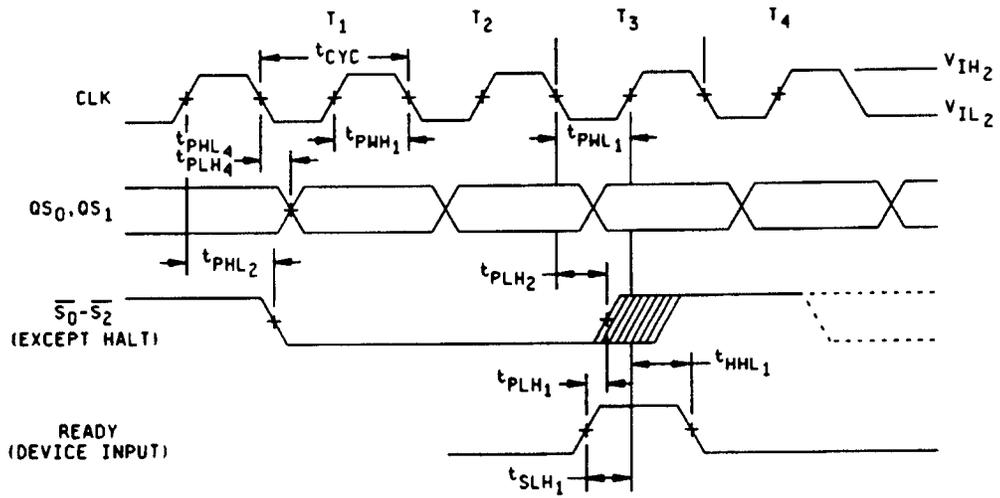
FIGURE 7. Bus timing - minimum mode system - write cycle.



NOTES:

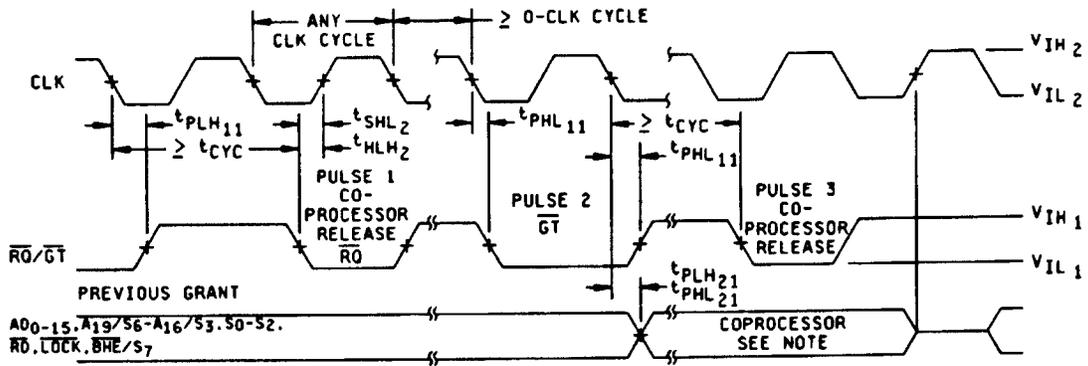
1. $\overline{RD}, \overline{WR} = V_{OH}; \overline{BHE} = V_{OL}$.
2. Two INTA cycles run consecutively. The local ADDR/DATA bus is floating during both cycles. Control signals are shown for second INTA cycle.

FIGURE 8. Bus timing - minimum mode system - interrupt cycle.



NOTE: Status inactive in state just prior to T₄.

FIGURE 9. Bus timing status signals (maximum mode).



NOTE: The coprocessor may not drive the busses outside the region shown without risking contention.

FIGURE 10. Request/grant sequence timing (maximum mode only).

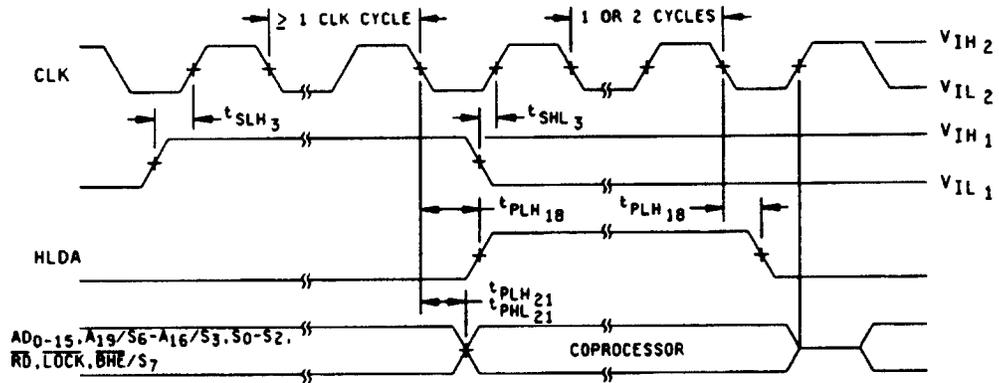
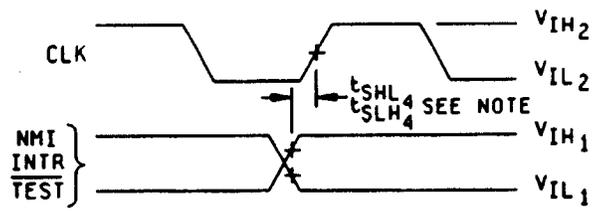


FIGURE 11. Hold/hold acknowledge timing (minimum mode only).



NOTE: Setup requirements for asynchronous signals only to ensure recognition at next CLK.

FIGURE 12. Asynchronous signal recognition.

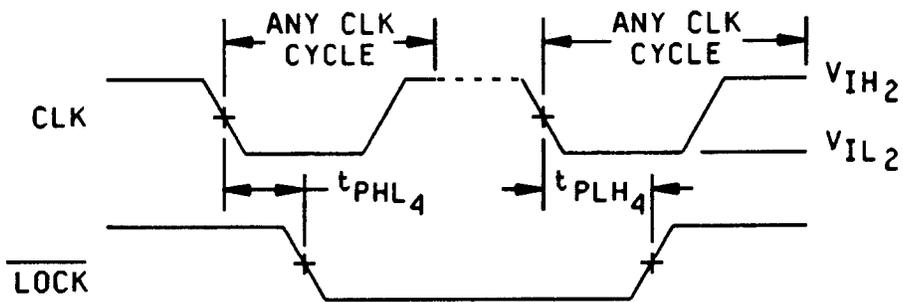


FIGURE 13. Bus lock signal timing (maximum mode only).

Table II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (in accordance with MIL-STD-883, TM 5005, table I.)	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1, 7	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11	1**, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group B (method 5005)	1, 2, 3, 7, 8, 9, 10, 11	None
Group C end-point electrical parameters (method 5005)	None	2, 8A, 10
Group D end-point electrical parameters (method 5005)	1, 2, 3, 7, 8	2, 8A, 10

*PDA applies to subgroups 1 and 7.

**PDA applies to subgroup 1.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate table and as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit ground terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life-test cooldown procedure. When devices are measured at +25°C following application of the operating life or burn-in test condition, they shall be cooled to 35°C prior to removal of the bias.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory).

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Acquisition requirements. The acquisition documents must specify the following:

- a. Title, number, and date of the specification.
- b. Issue of DDDISS to be cited in the solicitation, and if required, the specific issue of individual documents referenced (see 2.1 and 2.2).
- c. Complete PIN.
- d. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- e. Requirements for certificate of compliance, if applicable.
- f. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

MIL-M-38510/530A

- g. Requirements for failure analysis (including required test condition of method 5003 of MI-STD-883), corrective action and reporting of results, if applicable.
- h. Requirements for product assurance and radiation hardness assurance options.
- i. Requirement for carriers, special lead lengths or lead forming, if applicable. These requirements shall not affect the PIN. Unless otherwise specified, these requirements will not apply to direct shipment to the Government.
- j. Requirement for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

- | Pins. | Description |
|----------|--|
| 2-16, 39 | <u>Address data bus:</u> These lines constitute the time multiplexed memory/I/O address (T_1) and data (T_2, T_3, T_W, T_4) bus. A_0 is analogous to BHE for the lower byte of the data bus, pins $D_7 - D_0$. It is LOW during T_1 when a byte is to be transferred on the lower portion of the bus in memory or I/O operations. Eight-bit oriented devices tied to the lower half would normally use A_0 to condition chip select functions. (See BHE). Those lines are active HIGH and float to 3-state OFF during interrupt acknowledge and local bus "hold acknowledge". |
| 35-38 | <u>Address/status:</u> During T_1 these are the four most significant address lines for memory operations. During I/O operations these lines are LOW. During memory and I/O operations, status information is available on these lines during T_2, T_3, T_W , and T_4 . The status of the interrupt enable FLAG bit (S_5) is updated at the beginning of each CLK cycle. A_{17}/S_4 and A_{16}/S_3 are encoded as shown. This information indicates which relocation register is presently being used for data accessing.

These lines float to 3-state OFF during local bus "hold acknowledge." |

A_{17}/S_4	A_{16}/S_3	Characteristics
0 (LOW)	0	Alternate Data Stack Code or none Data
0	1	
1 (HIGH)	0	
1	1	
S_6 is 0 (LOW)		

- 34 Bus high enable/status: During T_1 the bus high enable signal (BHE) should be used to enable data onto the most significant half of the data bus, pins $D_{15}-D_8$.

BHE is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. The S_7 status information is available during T_2, T_3 , and T_4 . The signal is active LOW, and floats to 3-state OFF in "hold". It is LOW during T_1 for the first interrupt acknowledge cycle.

$\overline{\text{BHE}}$	A_0	Characteristics
0	0	Whole word Upper byte from to odd address
0	1	
1	0	Lower byte from to even address
1	1	None

- 32 Read: Read strobe indicates that the processor is performing a memory or I/O read cycle, depending on the state of the S_2 pin. This signal is used to read devices which reside on the local bus. RD is active LOW during T_2, T_3 , and T_W of any read cycle, and is guaranteed to remain HIGH in T_2 until the 8086 local bus has floated. This signal floats to 3-state OFF in "hold acknowledge".

- | <u>Pins</u> | <u>Description</u> |
|-------------|--|
| 22 | <u>Ready:</u> Ready is the acknowledgement from the addressed memory or I/O device that it will complete the data transfer. This signal is active HIGH. The Ready input is not synchronized. |
| 18 | <u>Interrupt request:</u> Interrupt request is a level triggered input which is sampled during the last clock cycle of each instruction to determine if the processor should enter into an interrupt acknowledge operation. It can be internally masked by software resetting the interrupt enable bit. INTR is internally synchronized. This signal is active HIGH. |
| 23 | <u>Test:</u> Test input is examined by the "Wait" instruction. If the TEST input is LOW execution continues, otherwise the processor waits in an "Idle" state. This input is synchronized internally during each clock cycle on the leading edge of CLK. |
| 17 | <u>Non-maskable interrupt:</u> An edge triggered input which causes a type 2 interrupt. A subroutine is vectored to via an interrupt vector lookup table located in system memory. NMI is not maskable internally by software. A transition from a LOW to HIGH initiates the interrupt at the end of the current instruction. This input is internally synchronized. |
| 21 | <u>Reset:</u> Reset causes the processor to immediately terminate its present activity. The signal must be active HIGH for a least four clock cycles. It restarts execution, as described in the Instruction Set description, when RESET returns LOW. Reset is internally synchronized. |
| 19 | <u>Clock:</u> Clock provides the basic timing for the processor and bus controller. It is asymmetric with a 33 percent duty cycle to provide optimized internal timing. |
| 40 | V _{CC} : + 5 V power supply pin. |
| 1,20 | Ground |
| 33 | <u>Minimum/maximum:</u> Indicates what mode the processor is to operate in. The two modes are discussed in the following sections:

Pins 24-31, when operating in maximum mode, perform the following function: |
| 26-28 | <u>Status:</u> Active during T ₄ , T ₁ , and T ₂ and is returned to the passive state (1,1,1) during T ₃ or during T _W when READY is HIGH. This status is used by the Bus Controller to generate all memory and I/O access control signals. Any change by S ₂ , S ₁ , or S ₀ during T ₄ is used to indicate the beginning of a bus cycle, and the return to the passive state in T ₃ or T _W is used to indicate the end of a bus cycle.

These signals float to 3-state OFF in "hold acknowledge". These status lines are encoded as shown. |

$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$	Characteristics
0 (LOW)	0	0	Interrupt Acknowledge
0	0	1	Read I/O PORT
0	1	0	Write I/O Port
0	1	1	Halt
1 (High)	0	0	Code Access
1	0	1	Read memory
1	1	0	Write memory
1	1	1	Passive

Pins	Description
30,31	<p>Request/grant: Pins are used by other local bus masters to force the processor to release the local bus at the end of the processor's current bus cycle. Each pin is bidirectional with RQ/GT₀ having higher priority than RQ/GT₁. RQ/GT has an internal pull-up resistor so may be left unconnected. The request/grant sequence is as follows (see figure 9):</p> <ol style="list-style-type: none"> 1. A pulse of 1 CLK wide from another local bus master indicates a local bus request ("hold") to the (pulse 1). 2. During the CPU's next T₄ or T₁ a pulse 1 CLK wide from the processor to the requesting master (pulse 2), indicates that the processor has allowed the local bus to float and that it will enter the "hold acknowledge" state at the next CLK. The CPU's bus interface unit is disconnected logically from the local bus during "hold acknowledge". 3. A pulse 1 CLK wide from the requesting master indicates to the processor (pulse 3) that the "hold" request is about to end and that the processor can reclaim the local bus at the next CLK. <p>Each master-master exchange of the local bus is a sequence of 3 pulses. There must be one dead CLK cycle after each bus exchange. Pulses are active LOW.</p>
29	<p>LOCK: Output indicates that other system bus masters are not to gain control of the system bus while LOCK is active LOW. The LOCK signal is activated by the "LOCK" prefix instruction and remains active until the completion of the next instruction. This signal is active LOW, and floats to 3-state OFF in "hold acknowledge".</p>
24-25	<p>Queue status: The queue status is valid during the CLK cycle after which the queue operation is performed.</p> <p>QS₁ and QS₀ provide status to allow external tracking of the internal instruction queue.</p> <p>Pins 24-31, when operating in minimum mode, perform the following function:</p>
28	<p>Status line: Logically equivalent to S₂ in the maximum mode. It is used to distinguish a memory access from an I/O access. M/I₀ becomes valid in the T₄ preceding a bus cycle and remains valid until the final T₄ of the cycle (M = HIGH, I₀ = LOW). M/I₀ floats to 3-state OFF in the local bus "hold acknowledge".</p>
29	<p>Write: Indicates that the processor is performing a write memory or write I/O cycle, depending on the state of the M/I₀ signal. WR is active for T₂, T₃, and T₄ of any write cycle. It is active LOW, and floats to 3-state OFF in local bus "hold acknowledge."</p>
24	<p>INTA: Is used as a read strobe for interrupt acknowledge cycles. It is active LOW during T₂, T₃, and T₄ of each interrupt acknowledge cycle.</p>
25	<p>Address latch enable: Provided by the processor to latch the address into the address latch. It is a HIGH pulse active during T₁ of any bus cycle. Note that ALE is never floated.</p>
27	<p>Data transmit/receive: Needed in minimum system that desires to use a data bus transceiver. It is used to control the direction of data flow through the transceiver. It is used to control the direction of data flow through the transceiver. Logically DT/R is equivalent to S₁ in the maximum mode, and its timing is the same as for M/I₀. (T = HIGH, R = LOW). This signal floats to 3-state OFF in local bus "hold acknowledge".</p>

26 Data enable: Provided as an output enable for a minimum system which uses the transceiver. DEN is active LOW during each memory and I/O access and for INTA cycles. For a read or INTA cycle it is active from the middle of T_2 until the middle of T_4 , while for a write cycle it is active from the beginning of T_2 until the middle of T_4 . DEN floats to 3-state OFF in local bus "hold acknowledge".

31 HOLD: Indicates that another master is requesting a local bus "hold". To be acknowledged. HOLD must be active HIGH. The processor receiving the "hold" request will issue HLDA (HIGH) as an acknowledgement in the middle of T_4 or T_1 . Simultaneous with the issuance of HLDA the processor will float the local bus and control lines. After HOLD is detected as being LOW, the processor will LOWER HLDA, and when the processor needs to run another cycle, it will again drive the local bus and control lines.

HOLD is not an asynchronous input. External synchronization should be provided if the system cannot otherwise guarantee the setup time.

6.4 Logistic support. Lead material and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Handling. MOS microprocessors should be handled with certain precautions to avoid damage due to the discharge of accumulated static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage, however, the following handling practices are recommended.

- a. Devices should be handled on benches with conductive and grounded surface.
- b. Ground test equipment and tools.
- c. Handling of devices by the leads should be avoided.
- d. Devices should be stored in conductive carriers.
- e. Avoid uses of plastic, rubber, or silk in MOS areas.

TABLE III. Instruction set summary.

Mnemonic and description	Instruction code			
DATA TRANSFERR				
MOV = Move:	76543210	76543210	76543210	76543210
Register/Memory to/from Register	100010dw	mod reg r/m		
Immediate to Register/Memory	1100011w	mod 000 r/m	data	data if w = 1
Immediate to Register	1011wreg	data	data if w = 1	
Memory to Accumulator	1010000w	addr-low	addr-high	
Accumulator to Memory	1010001w	addr-low	addr-high	
Register/Memory to Segment Register	10001110	mod 0 reg r/m		
Segment Register to Register/Memory	10001100	mod 0 reg r/m		
PUSH = Push:				
Register/Memory	11111111	mod 110 r/m		
Register	01010reg			
Segment Register	000reg110			
POP = Pop:				
Register/Memory	10001111	mod 000 r/m		
Register	01011reg			
Segment Register	000reg111			
XCHG = Exchange:				
Register/Memory with Register	1000011w	mod reg r/m		
Register with Accumulator	10010reg			
IN = Input from:				
Fixed Port	1110010w	port		
Variable Port	1110110w			
OUT = Output to:				
Fixed Port	1110011w	port		
Variable Port	1110111w			
XLAT = Translate Byte to AL	11010111			
LEA = Load EA to Register	10001101	mod reg r/m		
LDS = Load Pointer to DS	11000101	mod reg r/m		
LES = Load Pointer to ES	11000100	mod reg r/m		
LAHF = Load AH with Flags	10011111			
SAHF = Store AH with Flags	10011110			
PUSHF = Push Flags	10011100			

TABLE III. Instruction set summary - Continued.

Mnemonic and description	Instruction code			
	10011101	76543210	76543210	76543210
POPF = Pop Flags	10011101			
ARITHMETIC	76543210	76543210	76543210	76543210
ADD = Add:				
Reg./Memory with Register to Either	00000dw	mod reg r/m		
Immediate to Register/Memory	10000sw	mod 000 r/m	data	data if s:w = 01
Immediate to Accumulator	0000010w	data	data if w = 1	
ADC = Add with Carry:				
Reg./Memory with Register to Either	000100dw	mod reg r/m		
Immediate to Register/Memory	10000sw	mod 010 r/m	data	data if s:w = 01
Immediate to Accumulator	0001010w	data	data if w = 1	
INC = Increment:				
Register/Memory	1111111w	mod 000 r/m		
Register	01000reg			
AAA = ASCII Adjust for Add	00110111			
BAA = Decimal Adjust for Add	00100111			
SUB = Subtract:				
Reg./Memory with Register to Either	001010dw	mod reg r/m		
Immediate from Register/Memory	10000sw	mod 101 r/m	data	data if s w = 01
Immediate from Accumulator	0010110w	data	data if w = 1	
SSB = Subtract with Borrow				
Reg./Memory with Register to Either	000110dw	mod reg r/m		
Immediate from Register/Memory	10000sw	mod 011 r/m	data	data if s w = 01
Immediate from Accumulator	000111w	data	data if w = 1	
DEC = Decrement:				
Register/Memory	1111111w	mod 001 r/m		
Register	01001 reg			
NEG = Change sign	1111011w	mod 011 r/m		
CMP = Compare:				
Register/Memory and Register	001110dw	mod reg r/m		
Immediate with Register/Memory	10000sw	mod 111 r/m	data	data if s w = 01
Immediate with Accumulator	0011110w	data	data if w = 1	
AAS = ASCII Adjust for Subtract	00111111			
DAS = Decimal Adjust for Subtract	00101111			

TABLE III. Instruction set summary - Continued.

Mnemonic and description	Instruction code			
MUL = Multiply (Unsigned)	1111011w	mod 100 r/m		
IMUL = Integer Multiply (Signed)	1111011w	mod 101 r/m		
AAM = ASCII Adjust for Multiply	11010100	00001010		
DIV = Divide (Unsigned)	1111011w	mod 110 r/m		
IDIV = Integer Divide (Signed)	1111011w	mod 111 r/m		
AAD = ASCII Adjust for Divide	11010101	00001010		
CSW = Convert Byte to Word	10011000			
CWD = Convert Word to Double Word	10011001			
LOGIC	76543210	76543210	76543210	76543210
NOT = Invert	1111011w	mod 010 r/m		
SHL/SAL = Shift Logical/Arithmetic Left	110100vw	mod 100 r/m		
SHR = Shift Logical Right	110100vw	mod 101 r/m		
SAR = Shift Arithmetic Right	110100vw	mod 111 r/m		
ROL = Rotate Left	110100vw	mod 000 r/m		
ROR = Rotate Right	110100vw	mod 001 r/m		
RCL = Rotate Through Carry Flag Left	110100vw	mod 010 r/m		
RCR = Rotate Through Carry Right	110100vw	mod 011 r/m		
AND = And:				
Reg./Memory and Register to Either	001000dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 100 r/m	data	data if w = 1
Immediate to Accumulator	0010010w	data	data if w = 1	
TEST = And Function to Flags, No Result:				
Register/Memory and Register	1000010w	mod reg r/m		
Immediate Data and Register/Memory	1111011w	mod 000 r/m	data	data if w = 1
Immediate Data and Accumulator	1010100w	data	data if w = 1	
OR = Or:				
Reg./Memory and Register to Either	000010dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 001 r/m	data	data if w = 1
Immediate to Accumulator	0000110w	data	data if w = 1	
XOR = Exclusive or:				
Reg./Memory and Register to Either	001100dw	mod reg r/m		
Immediate to Register/Memory	1000000w	mod 110 r/m	data	data if w = 1
Immediate to Accumulator	0011010w	data	data if w = 1	

TABLE III. Instruction set summary - Continued.

Mnemonic and description	Instruction code		
STRING MANIPULATION			
REP = Repeat	1111001z		
MOVS = Move Byte/Word	1010010w		
CMPS = Compare Byte/Word	1010011w		
SCAS = Scan Byte/Word	1010111w		
LODS = Load Byte/Wd to AL/AX	1010110w		
STOS = Stor Byte/Wd to AL/A	1010101w		
CONTROL TRANSFER			
CALL = Call:			
Direct within Segment	1110100	disp-low	disp-high
Indirect within Segment	1111111	mod 010 r/m	
Direct Intersegment	10011010	offset-low	offset-high
		seg-low	seg-high
Indirect Intersegment	11111111	mod 011 r/m	
JMP = Unconditional Jump	76543210	76543210	76543210
Direct within Segment	11101001	disp-low	disp-high
Direct within Segment-Short	11101011	disp	
Indirect within Segment	11111111	mod 100 r/m	
Direct Intersegment	11101010	offset-low	offset-high
		seg-low	seg-high
Indirect Intersegment	11111111	mod 101 r/m	
RET = Return from CALL:			
Within Segment	11000011		
Within Seg Adding Immed to SP	11000010	data-low	data-high
Intersegment	11001011		
Intersegment Adding Immed to SP	11001010	data-low	data-high
JE/JZ = Jump on Equal/Zero	01110100	disp	
JL/JNGE = Jump on Less/Not Greater or Equal	01111100	disp	
JLE/JNG = Jump on Less or Equal/Not Greater	01111110	disp	
JB/JNAE = Jump on Below/Not Above or Equal	01110010	disp	
JBE/JNA = Jump on Below or Equal/Not Above	01110110	disp	
JP/JPE = Jump on Parity/Parity Even	01111010	disp	
JO = Jump on Overflow	01110000	disp	
JS = Jump on Sign	01111000	disp	

TABLE III. Instruction set summary - Continued.

Mnemonic and description	Instruction code	
	Binary	Field
JNE/JNZ = Jump on Not Equal/Not Zero	01110101	disp
JNL/JGE = Jump on Not Less/Greater or Equal	01111101	disp
JNLE/JG = Jump on Not Less or Equal/Greater	01111111	disp
JNB/JAE = Jump on Not Below/Above or Equal	01110011	disp
JNBE/JA = Jump on Not Below or Equal/Above	01110111	disp
JNP/JPO = Jump on Not Par/Par Odd	01111011	disp
JNO = Jump on Not Overflow	01110001	disp
JNS = Jump on Not Sign	01111001	disp
LOOP = Loop CX Times	11100010	disp
LOOPZ/LOOPE = Loop While Zero/Equal	11100001	disp
LOOPNZ/LOOPNE = Loop While Not Zero/Equal	11100000	disp
JCXZ = Jump on CX Zero	11100011	disp
INT = Interrupt		
Type Specified	11001101	type
Type 3	11001100	
INTO = Interrupt on Overflow	11001110	
IRET = Interrupt Return	11001111	
PROCESSOR CONTROL		
CLC = Clear Carry	11111000	
CMC = Complement Carry	11110101	
STC = Set Carry	11111001	
CLD = Clear Direction	11111100	
STD = Set Direction	11111101	
CLI = Clear Interrupt	11111010	
STI = Set Interrupt	11111011	
HLT = Halt	11110100	
WAIT = Wait	10011011	
ESC = Escape (to External Device)	11011xxx	mod xxx r/m
LOCK = Bus Lock Prefix	11110000	

See notes at end of table.

TABLE III. Instruction set summary - Continued.

NOTES:

AL = 8-bit accumulator

AX = 16-bit accumulator

CX = Count register

DS = Data segment

ES = Extra segment

Above/below refers to unsigned value

Greater = more positive:

Less = less positive (more negative) signed values

if $d = 1$ then "to" reg: if $d = 0$ then "from" regif $w = 1$ then word instruction: if $w = 0$ then byte instructionif $mod = 11$ then r/m is treated as a REG fieldif $mod = 00$ then $DISP = 0$, disp-low and disp-high are absentif $mod = 01$ then $DISP =$ disp-low sign-extended to 16 bits, disp-high is absentif $mod = 10$ then $DISP =$ disp-high: disp-lowif $r/m = 000$ then $EA = (BX) + (SI) + DISP$ if $r/m = 001$ then $EA = (BX) + (DI) + DISP$ if $r/m = 010$ then $EA = (BP) + (SI) + DISP$ if $r/m = 011$ then $EA = (BP) + (DI) + DISP$ if $r/m = 100$ then $EA = (SI) + DISP$ if $r/m = 101$ then $EA = (DI) + DISP$ *if $r/m = 110$ then $EA = (BP) + DISP$ if $r/m = 111$ then $EA = (BX) + DISP$

DISP follows 2nd byte of instruction (before data if required)

if $sw = 01$ then 16 bits of immediate data form the operandif $sw = 11$ then an immediate data byte is sign extended to form the 16-bits operandif $v = 0$ then "count" = 1: if $v = 1$ then "count" in (CL) x = don't care z is used for string primitive for comparison with ZF FLAG

SEGMENT OVERRIDE PREFIX

001 reg 110

REG is assigned according to the following table:

16-Bit($w = 1$)	8-Bit($w = 0$)	Segment
000 AX	000 AL	00 ES
001 CX	001 CL	01 CS
010 DX	010 DL	10 SS
011 BX	011 BL	11 DS
100 SP	100 AH	
101 BP	101 CH	
110 SI	110 DH	
111 DI	111 BH	

Instructions which reference the flag register file as a 16-bit object use the symbol FLAGS to represent the file:

FLAGS = X:X:X(XOF):(DF):(IF):(TF):(SF):(ZF):X:(AF):X:(PF):X:(CF)

* except if $mod = 00$ and $r/m = 110$ then $EA =$ disp-high; disp-low

MIL-M-38510/530A

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military-device type</u>	<u>Generic-industry type</u>
01	8086

Custodian:
Air Force - 17

Preparing activity:
DLA-ES

Review activities:
Air Force - 11, 19, 85, 99

(Project 5962-F732)