MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, N-CHANNEL, SILICON GATE MONOLITHIC 16-BIT MICROPROCESSOR

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic N-channel, silicon gate microprocessor. One product assurance class (B) and a choice of case outline/lead finish are provided for each type, and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

Device type	Clock frequency	Circuit
01	4.0 MHz	16-bit, fixed instruction microprocessor
02	4.0 MHz	16-bit, fixed instruction microprocessor
03	6.0 MHz	16-bit, fixed instruction microprocessor
04	6.0 MHz	16-bit, fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Letter	Case outline, (see MIL-M-38510, appendix C)
Q	D-5 (40-lead, 9/16" x 2-1/16" dual-in-line package)
X	See figure 1 (48-lead, 9/16" x 2-7/16" dual-in-line package)
Y	C-5 (44-terminal SQ chip carrier, .650" x .650") Option A
Z	C-6 (52-terminal SQ chip carrier, .750" x .750") Option A

1.3 Absolute maximum ratings.

V_{CC} supply voltage range (referenced to GND) -	-0.3 V to +7 V
Voltage on any pin (referenced to ground)- - -	-0.3 V to +7 V
Storage temperature range- - - - - - - - - - -	-65°C to +150°C
Power dissipation per package (all device types) - - - - - - - - - - - - - -	2.5 W
Maximum power dissipation per device (all device types)	
T_C = -55°C - - - - - - - - - - - - - - - - - -	2.3 W
T_C = +125°C - - - - - - - - - - - - - - - - -	1.6 W
Lead temperature (soldering, 5 seconds)- - - -	270°C
Maximum junction temperature (T_J) at T_C = 125°C- - - - - - - - - - - - - - - - -	150°C
Thermal resistance, junction to case (θ_{JC}) (Case Q) -	30°C/W

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RADC (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage	4.5 V min to 5.5 V max
Minimum high-level input voltage (V_{IH})	
Logic inputs	2.4 V
Clock input	V_{CC} -0.4 V
Reset	2.4 V
Maximum low-level input voltage (V_{IL})	
Logic and reset inputs	0.8 V
Clock input	0.45 V
Frequency of operation	
Device types 01 and 02	0.5 to 4.0 MHz
Device types 03 and 04	0.5 to 6.0 MHz
Case operating temperature range	-55°C to +125°C
Clock rise time (t_r)	
Device types 01 and 02	20 ns max
Device types 03 and 04	10 ns max
Clock fall time (t_f)	
Device types 01 and 02	20 ns max
Device types 03 and 04	10 ns max

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification For

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections and pin assignments. The terminal connections and pin assignments shall be as specified on figure 2.

3.2.2 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.3 Functional description, terms, and symbols. The functional description, terms, and symbols shall be as specified in 6.5.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3, herein.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.6).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Figure no. 4/	Reference no. 3/	Device types -01 Min	-01 Max	-02 Min	-02 Max	-03 Min	-03 Max	-04 Min	-04 Max	Limits Min	Limits Max	Unit
Clock input low voltage	V_{IL1}												-0.3	0.45	V
Clock input high voltage	V_{IH1}												V_{CC} -.4	V_{CC} +0.3	"
Input low voltage	V_{IL2}												-0.3	0.8	"
Input high voltage	V_{IH2}												2.4	V_{CC} +0.3	"
$\overline{RESET}$ input high voltage	V_{IH3}												2.4	V_{CC} +0.3	"
Output low voltage	V_{OL}	I_{OL} = 2.0 mA; V_{CC} = 5.5 V												0.4	"
Output high voltage	V_{OH}	I_{OH} = -250 µA; V_{CC} = 4.5 V											2.4		"
Power supply current	I_{CC}	V_{CC} = 5.5 V												350	mA
Input high current (input and bidirectional)	I_{IH}	V_{CC} = 5.5 V; V_{IN} = 2.4 V											-10	+10	µA
Input low current (input and bidirectional)	I_{IL}	V_{CC} = 5.5 V; V_{IN} = 0.4 V											-10	+10	"
Tristate output high leakage current (in float)	I_{ZH}	V_{CC} = 5.5 V; V_{IN} = 2.4 V											-10	+10	"
Tristate output low leakage current (in float)	I_{ZL}	V_{CC} = 5.5 V; V_{IN} = 0.4 V											-10	+10	"
Input clock capacitance	C_{I1}													50	pF
Input capacitance	C_{I2}													10	"
Input capacitance-bidirectional inputs	C_{I3}													25	"
Output capacitance, all other outputs	C_O													15	"
Maximum clock frequency	f_{MAX}	4.5 V ≤ V_{CC} ≤ 5.5 V C_L = 130 pF ±10%			4.0		4.0		6.0		6.0				MHz
Clock cycle time	t_{cyc}	-55°C ≤ T_C ≤ +125°C V_{CC} = 5.0 V ±10% C_L = 130 pF ±10%	6	1	250	2,000	250	2,000	165	2,000	165	2,000			ns
Clock width (high)	t_{PWH1}	"	"	2	105	1,895	105	1,895	70	1,930	70	1,930			"
Clock width (low)	t_{PWL1}	"	"	3	105	1,895	105	1,895	70	1,930	70	1,930			"
$\overline{MREQ}$ width (high)	t_{PWH7}	"	"	19	210 5/		210 5/		135 5/		135 5/				"
$\overline{AS}$ width (low)	t_{PWL2}	"	"	29	85 5/		85 5/		55 5/		55 5/				"
$\overline{DS}$ (read) width (low)	t_{PWL3}	"	"	38	275 5/		275 5/		185 5/		185 5/				"
$\overline{DS}$ (write) width (low)	t_{PWL4}	"	"	40	185 5/		185 5/		110 5/		110 5/				"
$\overline{DS}$ (I/O) width (low)	t_{PWL5}	"	"	43	410 5/		410 5/		255 5/		255 5/				"
$\overline{NMI}$ width (low)	t_{PWL6}	"	"	51	100		100		70		70				"

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Figure no. 4/	Reference no. 3/	Device types -01 Min	-01 Max	-02 Min	-02 Max	-03 Min	-03 Max	-04 Min	-04 Max	Limits Min	Limits Max	Unit
Data in to clock ↓ setup	t_{SLH1} t_{SHL1}	$-55°C \leq T_C \leq +125°C$ V_{CC} = 5.0 V ±10% C_L = 130 pF ±10%	6	12	50		50		20		20				ns
$\overline{RESET}$ to clock ↑ setup	t_{SLH2} t_{SHL2}	"	"	49	180		180		70		70				"
$\overline{VI}$, $\overline{NVI}$ to clock ↑ setup	t_{SLH3} t_{SHL3}	"	"	53	110		110		50		50				"
$\overline{SEGT}$ to clock ↑ setup 1/	t_{SLH4} t_{SHL4}	"	"	55	70				55						"
$\overline{MI}$ to clock ↑ setup	t_{SLH5} t_{SHL5}	"	"	57	180		180		140		140				"
$\overline{STOP}$ to clock ↓ setup	t_{SLH6} t_{SHL6}	"	"	60	140		140		100		100				"
$\overline{WAIT}$ to clock ↓ setup	t_{SLH7} t_{SHL7}	"	"	62	50		50		30		30				"
$\overline{BUSRQ}$ to clock ↑ setup	t_{SLH8} t_{SHL8}	"	"	64	90		90		80		80				"
$\overline{NMI}$ to clock ↑ setup	t_{SHL9}	"	"	52	140		140		70		70				"
Data in to $\overline{DS}$ ↑ hold	t_{HLZ1} t_{HHZ1}	"	"	15	0		0		0		0				"
$\overline{RESET}$ to clock ↑ hold	t_{HLH1} t_{HHL1}	"	"	50	0		0		0		0				"
$\overline{VI}$, $\overline{NMI}$ to clock ↑ hold	t_{HLH2} t_{HHL2}	"	"	54	20		20		20		20				"
$\overline{SEGT}$ to clock ↑ hold 1/	t_{HLH3} t_{HHL3}	"	"	56	0				0						"
$\overline{MI}$ to clock ↑ hold	t_{HLH4} t_{HHL4}	"	"	58	0		0		0		0				"
$\overline{STOP}$ to clock ↓ hold	t_{HLH5} t_{HHL5}	"	"	61	0		0		0		0				"
$\overline{WAIT}$ to clock ↓ hold	t_{HLH6} t_{HHL6}	"	"	63	10		10		10		10				"
$\overline{BUSRQ}$ to clock ↑ hold	t_{HLH7} t_{HHL7}	"	"	65	10		10		10		10				"
Clock ↑ to segment number valid 1/	2/ t_{PLH1} t_{PHL1}	"	"	6		130				110					"
Clock ↑ to segment number not valid 1/	2/ t_{PLH2} t_{PHL2}	"	"	7	20				10						"
Clock ↑ to address valid	2/ t_{PLH3} t_{PHL3}	"	"	9		100		100		75		75			"

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Figure no. 4/	Reference no. 3/	Device types -01 Min	-01 Max	-02 Min	-02 Max	-03 Min	-03 Max	-04 Min	-04 Max	Limits Min	Limits Max	Unit
Address valid to data in required valid	t_{PLH4} 2/ t_{PHL4} "	C_L = 130 pF ±10%	6	11	455 5/		455 5/		305 5/		305 5/				ns
$\overline{DS}$ ↑ to address active	t_{PZL1} " t_{PZH1} "	"	"	13	80 5/		80 5/		40 5/		40 5/				"
$\overline{MREQ}$ ↓ to address not active	t_{PLZ1} " t_{PHZ1} "	"	"	20	70 5/		70 5/		35 5/		35 5/				"
$\overline{AS}$ ↑ to address not active	t_{PLZ2} " t_{PHZ2} "	"	"	30	60 5/		60 5/		30 5/		30 5/				"
Clock ↑ to address float	t_{PLZ3} " t_{PHZ3} "	"	"	10		90		90		75		75			"
Clock ↑ to bus float	t_{PLZ4} " t_{PHZ4} "	"	"	8		90		90		75		75			"
$\overline{MREQ}$ ↓ to data In required valid	t_{PLH5} " t_{PHL5} "	"	"	22	350 5/		350 5/		225 5/		225 5/				"
$\overline{AS}$ ↑ to data In required valid	t_{PLH6} " t_{PHL6} "	"	"	27	340 5/		340 5/		215 5/		215 5/				"
$\overline{DS}$ (read) ↓ to data In required valid	t_{PLH7} " t_{PHL7} "	"	"	33	185 5/		185 5/		130 5/		130 5/				"
$\overline{DS}$ (input) ↓ to data In required valid	t_{PLH8} " t_{PHL8} "	"	"	41	320 5/		320 5/		200 5/		200 5/				"
$\overline{DS}$ (Ack) ↓ to data in required valid	t_{PLH9} " t_{PHL9} "	"	"	46	435 5/		435 5/		295 5/		295 5/				"
Clock ↑ to data out valid	t_{PLH10} " t_{PHL10} "	"	"	14		100		100		75		75			"
$\overline{DS}$ ↑ to data out not valid	t_{PLH11} " t_{PHL11} "	"	"	35	75 5/		75 5/		45 5/		45 5/				"
Clock ↑ to status valid delay	t_{PLH12} " t_{PHL12} "	"	"	47		110		110		85		85			"
Clock ↑ to $\overline{MO}$ delay	t_{PLH13} " t_{PHL13} "	"	"	59		120		120		85		85			"
Data out valid to $\overline{DS}$ ↑ delay	t_{PLH14} "	"	"	16	295 5/		295 5/		195 5/		195 5/				"
Data out valid to $\overline{DS}$ ↓ (write) delay	t_{PHL14} "	"	"	21	55 5/		55 5/		35 5/		35 5/				"
Address float to $\overline{DS}$ ↓ (read) delay	t_{PHL15} "	"	"	31	0		0		0		0				"
$\overline{AS}$ ↑ to $\overline{DS}$ ↓ (read) delay	t_{PHL16} "	"	"	32	70 5/		70 5/		35 5/		35 5/				"
Clock ↓ to $\overline{DS}$ ↑ delay	t_{PLH28} "	"	"	34		70		70		65		65			"
Address valid to $\overline{DS}$ ↓ (read) delay	t_{PHL17} "	"	"	36	180 5/		180 5/		110 5/		110 5/				"

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions (T_C = -55°C to +125°C; V_{CC} = 5.0 V ±10% unless otherwise specified)	Figure no. 4/	Reference no. 3/	Device types -01 Min	-01 Max	-02 Min	-02 Max	-03 Min	-03 Max	-04 Min	-04 Max	Limits Min	Limits Max	Unit
Clock ↑ to $\overline{DS}$ ↓ (read) delay	t_{PHL18} 2/	C_L = 130 pF ±10%	6	37		120		120		85		85			ns
Clock ↑ to $\overline{DS}$ ↓ (write) delay	t_{PHL19} "	"	"	39		95		95		80		80			"
Clock to $\overline{DS}$ (I/O) delay	t_{PHL20} "	"	"	42		120		120		100		100			"
$\overline{AS}$ ↓ to $\overline{DS}$ ↓ (Ack) delay	t_{PHL21} "	"	"	44	1,065 5/		1,065 5/		690 5/		690 5/				"
Clock ↑ to $\overline{DS}$ ↓ (Ack) delay	t_{PHL22} "	"	"	45		120		120		85		85			"
Address valid to $\overline{MREQ}$ ↓ delay	t_{PHL23} "	"	"	17	55 5/		55 5/		35 5/		35 5/				"
Clock ↓ to $\overline{MREQ}$ ↓ delay	t_{PHL24} "	"	"	18		80		80		70		70			"
Clock ↓ to $\overline{MREQ}$ ↑ delay	t_{PLH24} "	"	"	23		80		80		60		60			"
Clock ↑ to $\overline{AS}$ ↓ delay	t_{PHL25} "	"	"	24		80		80		60		60			"
Address valid to $\overline{AS}$ ↑ delay	t_{PLH29} "	"	"	25	55 5/		55 5/		35 5/		35 5/				"
Clock ↓ to $\overline{AS}$ ↑ delay	t_{PLH30} "	"	"	26		90		90		80		80			"
$\overline{DS}$ ↑ to $\overline{AS}$ ↓ delay	t_{PHL26} "	"	"	28	70 5/		70 5/		35 5/		35 5/				"
Status valid to $\overline{AS}$ ↑ delay	t_{PLH31} "	"	"	48	60 5/		60 5/		30 5/		30 5/				"
Clock ↑ to $\overline{BUSAK}$ ↓ delay	t_{PLH27} "	"	"	66		100		100		75		75			"
Clock ↑ to $\overline{BUSAK}$ ↓ delay	t_{PHL27} "	"	"	67		100		100		75		75			"

1/ These parameters apply to the -01 and -03 parts only.
2/ Propagation delays and pulse widths are specified with load of figure 5 attached to output pins.
3/ The reference number refers to the position where the parameter being tested appears on figure 6.
4/ Figure 6 represents the electrical performance characteristics associated with the ac limits shown in table I.
5/ These reference number parameters are dependent upon clock high or clock low or clock cycle time. The limits provided are at maximum frequency. To determine the limits at other frequencies use the following equations (see next page).

5/ - Continued.

Reference	Symbol	Device types 01 and 02	Device types 03 and 04
11	t_{PLH4} t_{PHL4}	2 t_{cyc} + t_{PWH1} - 150 ns	2 t_{cyc} + t_{PWH1} - 95 ns
13	t_{PZL1} t_{PZH1}	t_{PWL1} - 25 ns	t_{PWL1} - 30 ns
16	t_{PLH14}	t_{cyc} + t_{PWH1} - 60 ns	t_{cyc} + t_{PWL1} - 40 ns
17	t_{PHL23}	t_{PWH1} - 50 ns	t_{PWH1} - 35 ns
19	t_{PWH7}	t_{cyc} - 40 ns	t_{cyc} - 30 ns
20	t_{PLZ1} t_{PHZ1}	t_{PWL1} - 35 ns	t_{PWL1} - 35 ns
21	t_{PHL14}	t_{PWH1} - 50 ns	t_{PWH1} - 35 ns
22	t_{PLH5} t_{PHL5}	2 t_{cyc} - 150 ns	2 t_{cyc} - 105 ns
25	t_{PLH29}	t_{PWH1} - 50 ns	t_{PWH1} - 35 ns
27	t_{PLH6} t_{PHL6}	2 t_{cyc} - 160 ns	2 t_{cyc} - 115 ns
28	t_{PHL26}	t_{PWL1} - 35 ns	t_{PWL1} - 35 ns
29	t_{PWL2}	t_{PWH1} - 20 ns	t_{PWH1} - 15 ns
30	t_{PLZ2} t_{PHZ2}	t_{PWL1} - 45 ns	t_{PWL1} - 40 ns
32	t_{PHL16}	t_{PWL1} - 35 ns	t_{PWL1} - 35 ns
33	t_{PLH7} t_{PHL7}	t_{cyc} + t_{PWH1} - 170 ns	t_{cyc} + t_{PWH1} - 105 ns
35	t_{PLH11} t_{PHL11}	t_{PWL1} - 30 ns	t_{PWL1} - 25 ns
36	t_{PHL17}	t_{cyc} - 70 ns	t_{cyc} - 55 ns
38	t_{PWL3}	t_{cyc} + t_{PWH1} - 80 ns	t_{cyc} + t_{PWH1} - 50 ns
40	t_{PWL4}	t_{cyc} - 65 ns	t_{cyc} - 55 ns
41	t_{PLH8} t_{PHL8}	2 t_{cyc} - 180 ns	2 t_{cyc} - 130 ns
43	t_{PWL5}	2 t_{cyc} - 90 ns	2 t_{cyc} - 75 ns
44	t_{PHL21}	4 t_{cyc} + t_{PWL1} - 40 ns	4 t_{cyc} + t_{PWL1} - 40 ns
46	t_{PLH9} t_{PHL9}	2 t_{cyc} + t_{PWH1} - 170 ns	2 t_{cyc} + t_{PWL1} - 105 ns
48	t_{PLH31}	t_{PWH1} - 55 ns	t_{PWH1} - 40 ns

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and on figure 6, and unless otherwise specified, apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III, table V, and figure 6.

3.6 Microprocessor instructions. The microprocessor instructions shall be as specified in table VI.

3.7 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in a microcircuit group number 107 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (see table III)
	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	1,7
Final electrical test parameters (method 5004)	*1,2,3,*7,8,**9 10,11
Group A test requirements (method 5005)	1,2,3,4,7,8,**9 10,11,12
Group C end-point electrical parameters (method 5005)	1,2,3,7,8
Group D end-point electrical parameters (method 5005)	1,2,3,7,8

*PDA applies to subgroups 1 and 7 (see 4.2c).
**Subgroup 9 is run concurrently with subgroup 7 with a combined LTPD of 5.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E, using the circuit shown on figure 4, or equivalent.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameters test prior to burn-in, is at the discretion of the manufacturer.

c. The percent defective allowable (PDA) is specified as 10 percent for class B devices based on failures from group A, subgroups 1 and 7 tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA.

If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for the lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

d. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3).

4.3.1 Qualification extension. For qualification inspection, if a manufacturer qualifies to a higher frequency device type which is designed and manufactured identically to a lower frequency device type on this specification, then the lower frequency device type may be part I qualified by conducting only group A electrical tests and electricals specified as additional group C subgroups in table II (when authorized by the qualifying activity) and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3).

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II, herein.

b. Subgroup 4 (C_0, C_{I1}, C_{I2}, and C_{I3} measurements) shall be performed only for initial qualification and after process or design changes which may affect device capacitance. Tests 88-132 for device types 01 and 03 and tests 72-108 for device types 02 and 04 shall be performed on 5 devices. Test 10 additional devices with the exception that one test be chosen from the following test group and performed as representative of the test group. The representative tests that are chosen will be the worst case high measured values taken on the previous 5 units. The test groups are tests 98-113 for device types 01 and 03 and tests 81-96 for device types 02 and 04."

c. Subgroup 12 shall be added to group A inspection requirements for class B devices using an LTPD of 10 and consist of the procedures, test conditions, and limits specified in table III. This subgroup shall be used for initial qualification only and variables data shall be submitted.

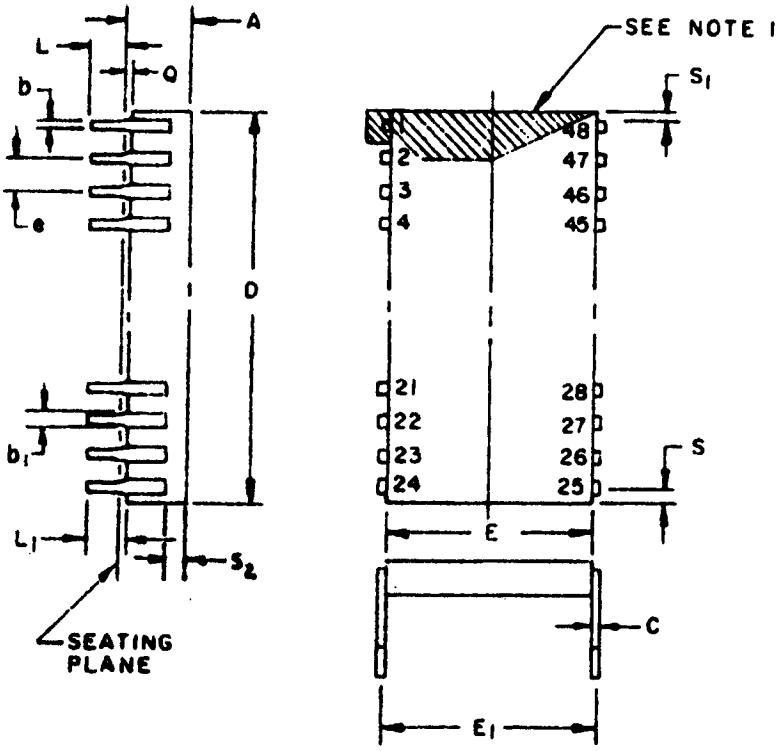
d. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883, and as follows: A special subgroup shall be added to the group B inspection requirements for class B. This subgroup shall consist of the test, conditions, and limits specified in 4.5.2. The LTPD for this subgroup shall be 15.

4.4.3 Groups C and D inspections. Groups C and D inspections shall consist of the test subgroups and LTPD values shown in tables III and IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II, herein.

TEXT CONTINUES ON PAGE 75.



NOTES:

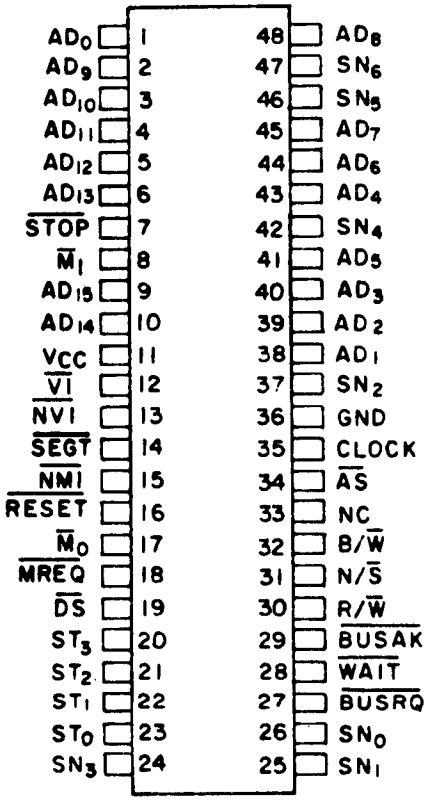
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The minmum limit for dimension b_1 may be .020 (.51 mm) for leads number 1, 24, 25, and 48 only.
3. Dimension Q shall be measured from the seating plane to the base plane.
4. The basic pin spacing is .100 (2.54 mm) between centerlines. Each pin centerline shall be located within ±.010 (.25 mm) of its exact longitudinal position relative to pins 1 and 48.
5. Applies to all four corners (leads number 1, 24, 25, and 48), and 40.5 shall apply.
6. Leads center when α is 0°. E_1 shall be measured at the centerline of the leads (see 40.4 of appendix C of MIL-M-38510).
7. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
8. Forty six spaces.
9. The top edge of lead shall not extend above the brazed pad top surface.

FIGURE 1. Case outline X (48-lead, 9/16" x 2-7/16" dual-in-line package).

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	---	.225	---	5.72	
b	.014	.023	.36	.58	7
b_1	.030	.070	.76	1.78	2,7
c	.008	.015	.20	.28	7
D	---	2.480	---	63.00	
E	.510	.620	12.95	15.75	
E_1	.520	.620	13.21	15.75	6
e	.100 BSC		2.54 BSC		4,8
L	.120	.200	3.05	5.08	
L_1	.150	---	3.81	---	
Q	.020	.060	.51	1.52	3
S	---	.098	---	2.49	5
S_1	.005	---	.13	---	5
S_2	.005	---	.13	---	9

FIGURE 1. Case outline X (48-lead, 9/16" x 2-7/16" dual-in-line package) - Continued.

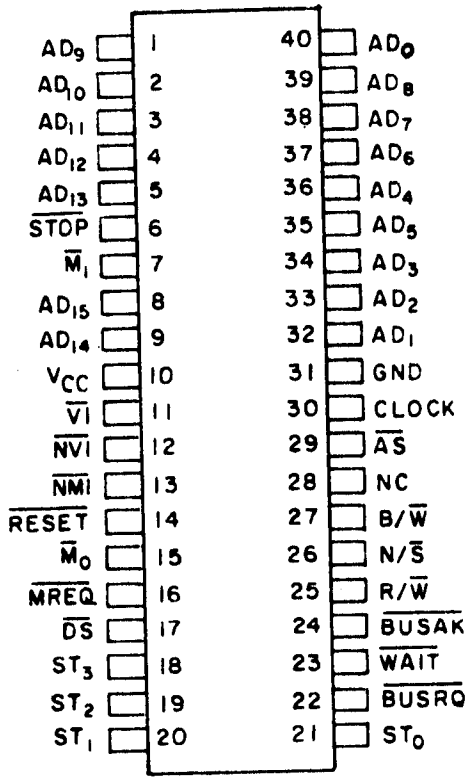
Device types 01 and 03



CASE X

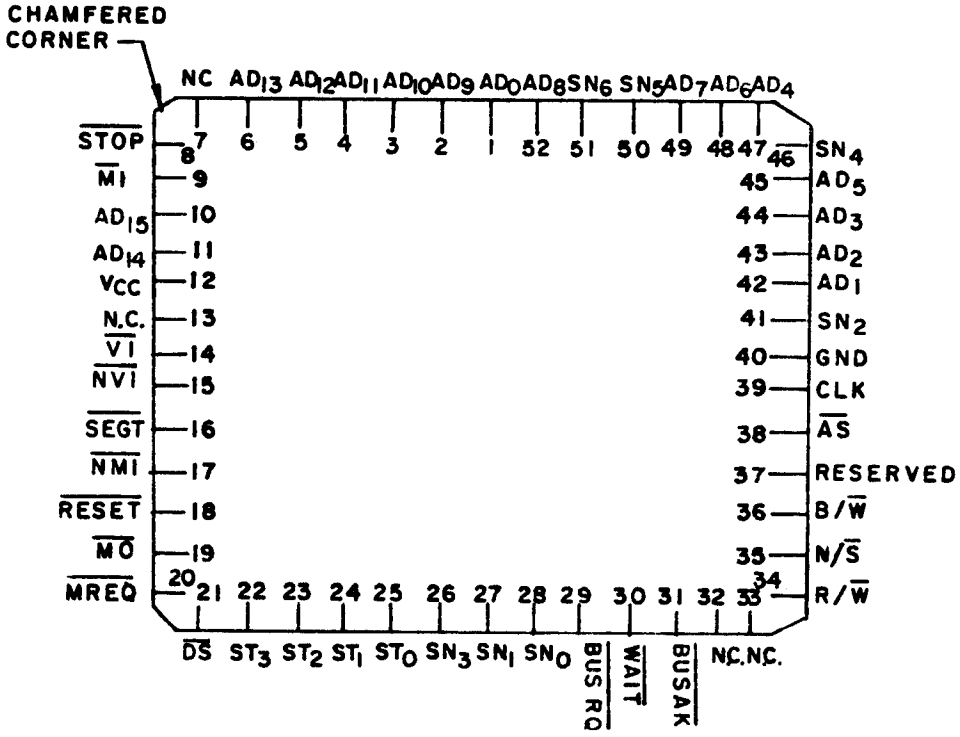
FIGURE 2. Terminal connections and pin assignments.

Device types 02 and 04



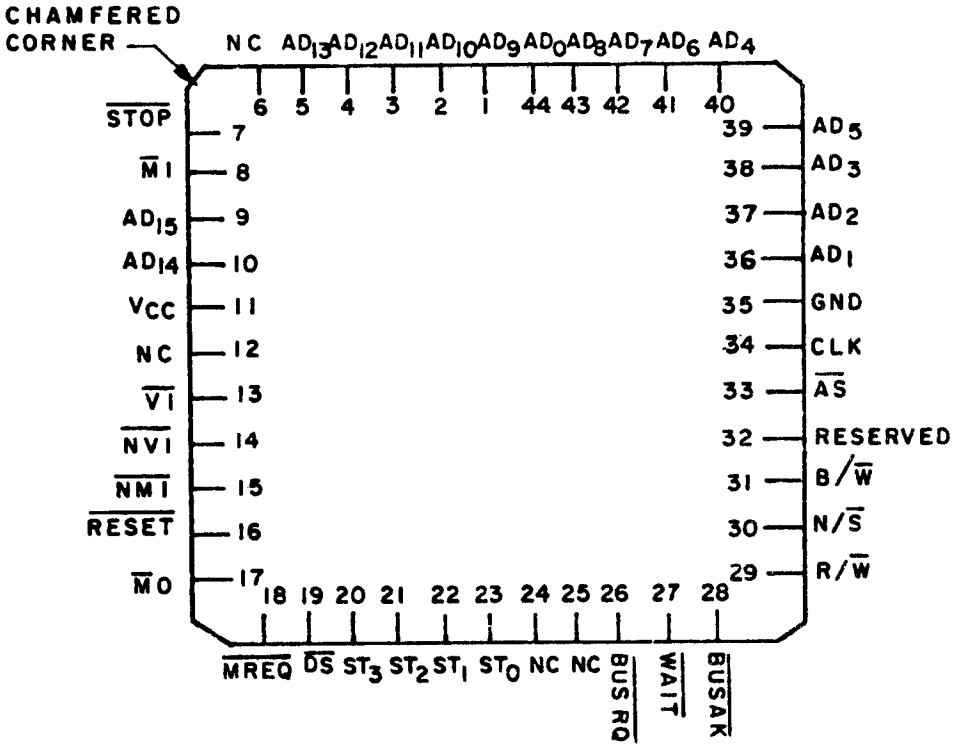
CASE Q

FIGURE 2. Terminal connections and pin assignments - Continued.



DEVICE TYPES 01 AND 03
N.C.=NO CONNECTION

FIGURE 2. Terminal connections (case outline Z, 52- terminal SQ chip carrier) - Continued.



DEVICE TYPES 02 AND 04
NC = NO CONNECTION

FIGURE 2. Terminal connections (case outline Y, 44- terminal SQ chip carrier) - Continued.

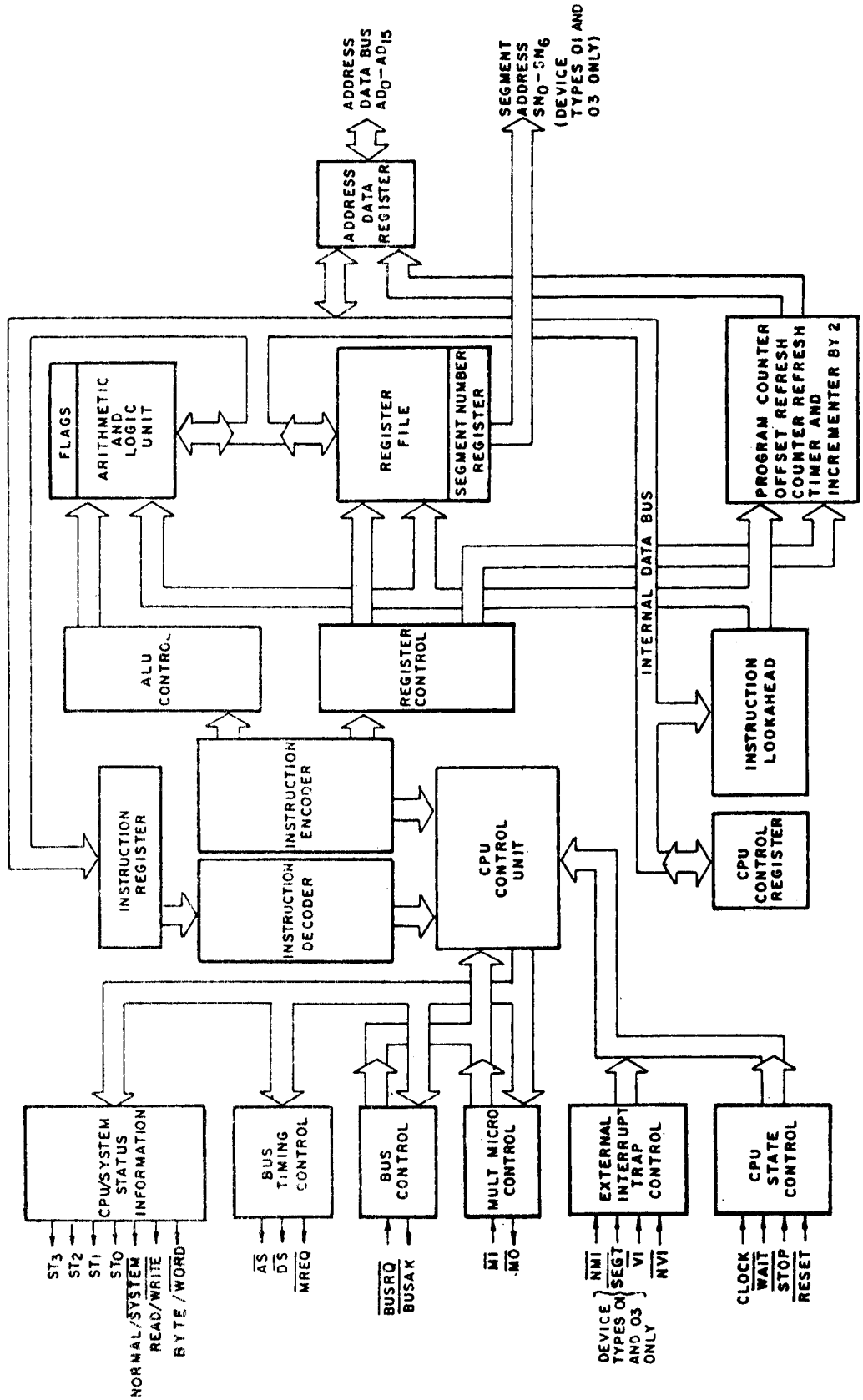
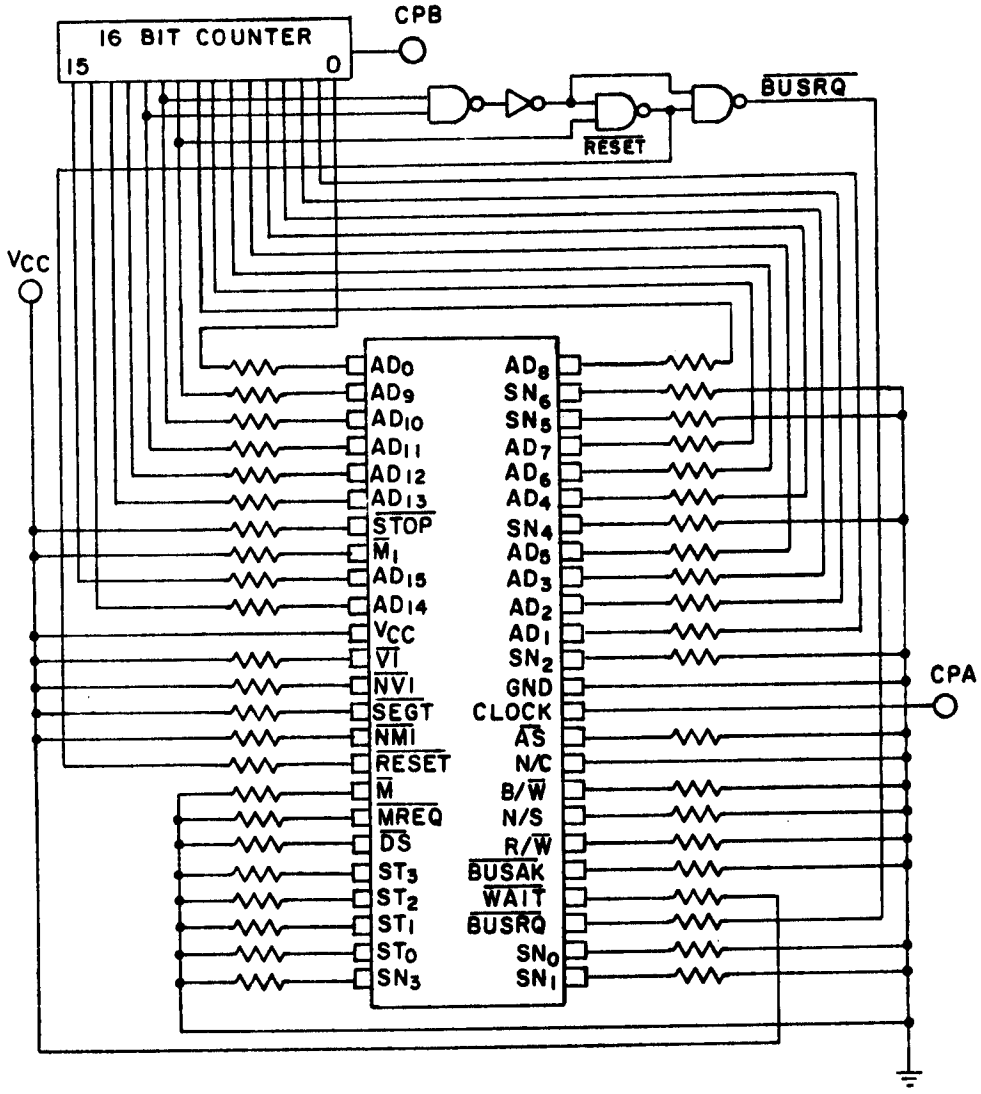


FIGURE 3. Functional block diagram.

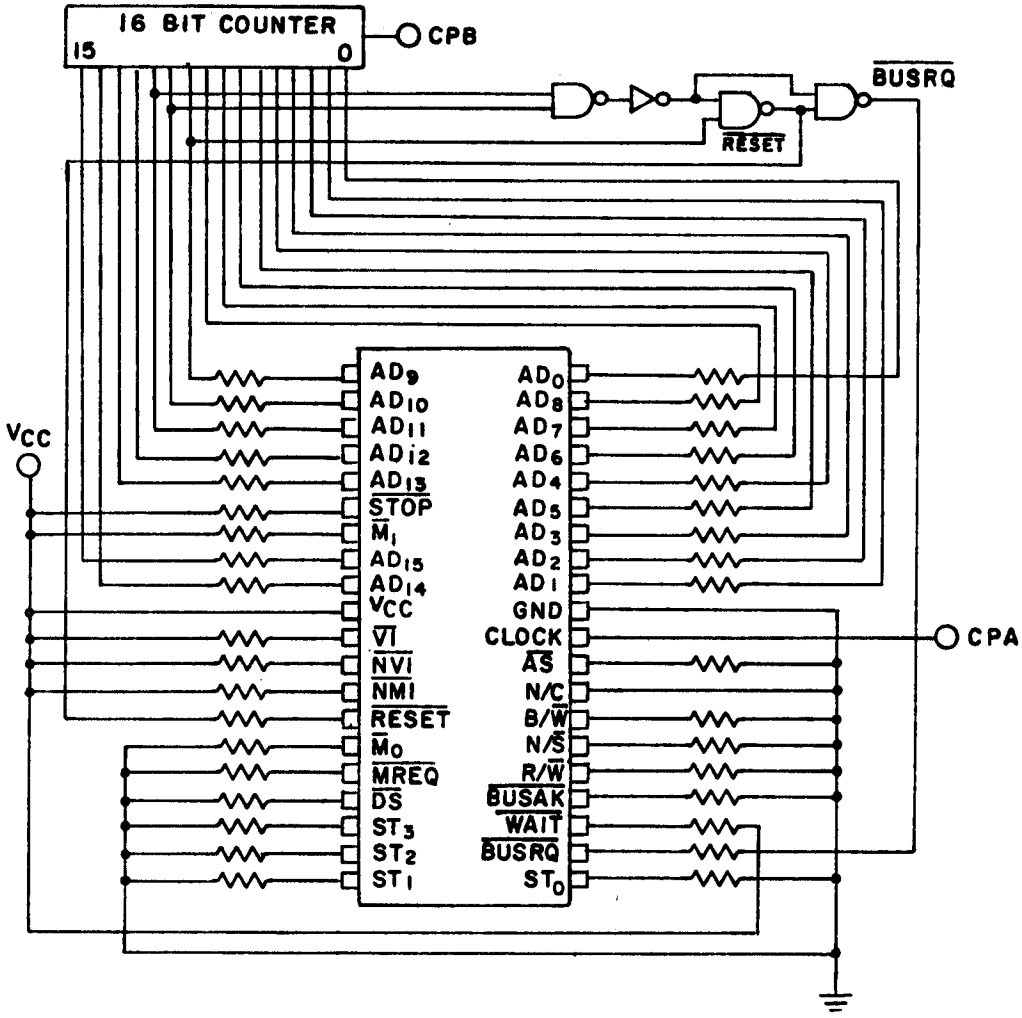
Device types 01 and 03



NOTES:
1. CPA = 250 kHz ±10% square wave; 50% duty cycle.
2. V_{CC} shall be no less than 4.5 V at device terminal.
   V_{CC} shall be no more than 5.5 V at device terminal.
3. V_{IL} shall be no more than 0.5 V at device terminal.
   V_{IH} shall be no less than V_{CC} -0.4 V at device terminal.
4. All resistors shall be 10 kΩ ±10% 1/4 W minimum.
5. CPB = 0.1 Hz ±10% square wave; 50% duty cycle.

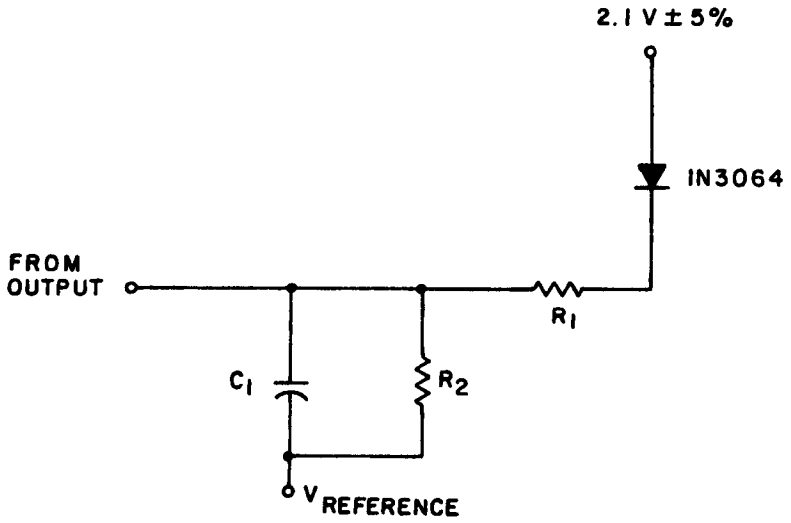
FIGURE 4. Dynamic burn-in and life test.

Device types 02 and 04



NOTES:
1. CPA = 250 kHz ±10% square wave; 50% duty cycle.
2. V_{CC} shall be no less than 4.5 V at device terminal.
   V_{CC} shall be no more than 5.5 V at device terminal.
3. V_{IL} shall be no more than 0.5 V at device terminal.
   V_{IH} shall be no less than V_{CC} -0.4 V at device terminal.
4. All resistors shall be 10 kΩ ±10% 1/4 W minimum.
5. CPB = 0.1 Hz ±10% square wave; 50% duty cycle.

FIGURE 4. Dynamic burn-in and life test - Continued.



NOTES:
1. R1 = 550Ω ±5%.
2. R2 = 9.6 kΩ ±5%.
3. C1 = 130 pF ±20%.
4. $V_{REFERENCE}$ = GND except for tests 145 and 146 for device types 01 and 03, and tests 121 and 122 for device types 02 and 04 during which $V_{REFERENCE}$ = -10 V.
5. During tests 145 and 146 (device types 01 and 03) and tests 121 and 122 (device types 02 and 04) testing proceeds as follows:
   a. Search actual V_{OH} and V_{OL} levels during output data drive time of DUT.
   b. Set tester output comparators to:
      V_{OH} (1 level) = Search value - 0.050 volts
      V_{OL} (0 level) = Search value + 0.050 volts
   c. Search with appropriate timing generator for data out not valid (tri-state).
   d. Compare search value < limits -- force error if not true.

FIGURE 5. Output load circuit for functional and ac testing.

TABLE III. Group A inspection for device types 01 and 03.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883-method	Test no.	1 AD_0	2 AD_9	3 AD_{10}	4 AD_{11}	5 AD_{12}	6 AD_{13}	7 $\overline{STOP}$	8 $\overline{RI}$	9 AD_{15}	10 AD_{14}	11 V_{CC}	12 $\overline{VI}$	13 $\overline{NVI}$	14 $\overline{SEGT}$	15 $\overline{NMI}$	16 $\overline{RESET}$	17 $\overline{MO}$	18 $\overline{NREQ}$	19 $\overline{DS}$	20 ST_3	21 ST_2	22 ST_1	23 ST_0	24 SN_3
1 $T_C = 25°C$	I_{CC}	3005	1							2.4 V	2.4 V			5.5 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V								
	I_{IH} 1/		2	2.4 V						"	"			"	"	"	"	"	"								
			3		2.4 V					"	"			"	"	"	"	"	"								
			4			2.4 V				"	"			"	"	"	"	"	"								
			5				2.4 V			"	"			"	"	"	"	"	"								
			6					2.4 V		"	"			"	"	"	"	"	"								
			7						2.4 V	"	"			"	"	"	"	"	"								
			8							"	"	2.4 V		"	"	"	"	"	"								
			9							"	"		2.4 V	"	"	"	"	"	"								
			10							"	"			"	"	"	"	"	"								
			11							"	"			"	"	"	"	"	"								
			12							"	"			"	"	"	"	"	"								
			13							"	"			"	"	"	"	"	"								
			14							"	"			"	"	"	"	"	"								
			15							"	"			"	"	"	"	"	"								
			16							"	"			"	"	"	"	"	"								
			17							"	"			"	"	"	"	"	"								
	I_{ZH} 1/		18							"	"			"	"	"	"	"	"				2.4 V				
			19							"	"			"	"	"	"	"	"					2.4 V			
			20							"	"			"	"	"	"	"	"						2.4 V		
			21							"	"			"	"	"	"	"	"							2.4 V	
			22							"	"			"	"	"	"	"	"								2.4 V
			23							"	"			"	"	"	"	"	"								
			24							"	"			"	"	"	"	"	"								
			25							"	"			"	"	"	"	"	"								
			26							"	"			"	"	"	"	"	"								
			27							"	"			"	"	"	"	"	"								
			28							"	"			"	"	"	"	"	"		2.4 V						
			29							"	"			"	"	"	"	"	"								
			30							"	"			"	"	"	"	"	"								
			31							"	"			"	"	"	"	"	"								
			32							"	"			"	"	"	"	"	"			2.4 V					
			33							"	"			"	"	"	"	"	"								
			34							"	"			"	"	"	"	"	"								
	I_{IH}		35							"	"			"	"	"	"	"	"								
			36							"	"			"	"	"	"	"	"								
			37							"	"			"	"	"	"	"	"								
			38							"	"			"	"	"	"	"	"								
			39							"	"			"	"	"	"	"	"								
			40							"	"			"	"	"	"	"	"								
			41							"	"			"	"	"	"	"	"								
			42							"	"			"	"	"	"	"	"								
			43							"	"			"	"	"	"	"	"								
			44							"	"			"	"	"	"	"	"								
	I_{IL} 1/		45	0.4 V						"	"			"	"	"	"	"	"								
			46		0.4 V					"	"			"	"	"	"	"	"								
			47			0.4 V				"	"			"	"	"	"	"	"								
			48				0.4 V			"	"			"	"	"	"	"	"								
			49					0.4 V		"	"			"	"	"	"	"	"								
			50						0.4 V	"	"			"	"	"	"	"	"								
			51							"	"	0.4 V		"	"	"	"	"	"								
			52							"	"		0.4 V	"	"	"	"	"	"								
			53							"	"			"	"	"	"	"	"								
			54							"	"			"	"	"	"	"	"								
			55							"	"			"	"	"	"	"	"								
			56							"	"			"	"	"	"	"	"								
			57							"	"			"	"	"	"	"	"								
			58							"	"			"	"	"	"	"	"								
			59							"	"			"	"	"	"	"	"								
			60							"	"			"	"	"	"	"	"								

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.	25 SM_1	26 SM_0	27 $\overline{BUSRQ}$	28 $\overline{WAIT}$	29 $\overline{BUSAK}$	30 $R/\overline{W}$	31 $N/\overline{S}$	32 $B/\overline{W}$	33 NC	34 $\overline{AS}$	35 CLK	36 GND	37 SM_2	38 AD_1	39 AD_2	40 AD_3	41 AD_5	42 SM_4	43 AD_4	44 AD_6	45 AD_7	46 SM_5	47 SM_6	48 AD_8	Measured terminal	Test Limits Min	Test Limits Max	Unit
1			0.8 V	2.4 V							5.1 V	GND													V_{CC}		275	mA
2			"	"							"	"													AD_0	-10	+10	µA
3			"	"							"	"													AD_9	"	"	"
4			"	"							"	"													AD_{10}	"	"	"
5			"	"							"	"													AD_{11}	"	"	"
6			"	"							"	"													AD_{12}	"	"	"
7			"	"							"	"													AD_{13}	"	"	"
8			"	"							"	"													AD_{15}	"	"	"
9			"	"							"	"													AD_{14}	"	"	"
10			"	"							"	"		2.4 V											AD_1	"	"	"
11			"	"							"	"			2.4 V										AD_2	"	"	"
12			"	"							"	"				2.4 V									AD_3	"	"	"
13			"	"							"	"					2.4 V								AD_5	"	"	"
14			"	"							"	"							2.4 V						AD_4	"	"	"
15			"	"							"	"								2.4 V					AD_6	"	"	"
16			"	"							"	"									2.4 V				AD_7	"	"	"
17			"	"							"	"												2.4 V	AD_8	"	"	"
18			"	"							"	"													ST_3	"	"	"
19			"	"							"	"													ST_2	"	"	"
20			"	"							"	"													ST_1	"	"	"
21			"	"							"	"													ST_0	"	"	"
22			"	"							"	"													SM_3	"	"	"
23	2.4 V		"	"							"	"													SM_1	"	"	"
24		2.4 V	"	"							"	"													SM_0	"	"	"
25			"	"							"	"													SM_2	"	"	"
26			"	"							"	"						2.4 V							SM_4	"	"	"
27			"	"							"	"										2.4 V			SM_5	"	"	"
28			"	"							"	"											2.4 V		SM_6	"	"	"
29			"	"							"	"													$\overline{MREQ}$	"	"	"
30			"	"		2.4 V					"	"													$R/\overline{W}$	"	"	"
31			"	"			2.4 V				"	"													$N/\overline{S}$	"	"	"
32			"	"				2.4 V			"	"													$B/\overline{W}$	"	"	"
33			"	"							"	"													$\overline{DS}$	"	"	"
34			"	"						2.4 V	"	"													$\overline{AS}$	"	"	"
35			"	"							"	"													$\overline{STOP}$	"	"	"
36			"	"							"	"													$\overline{M1}$	"	"	"
37			"	"							"	"													$\overline{VT}$	"	"	"
38			"	"							"	"													$\overline{NVI}$	"	"	"
39			"	"							"	"													$\overline{SEGT}$	"	"	"
40			"	"							"	"													$\overline{NMI}$	"	"	"
41			"	"							"	"													$\overline{RESET}$	"	"	"
42			"	"							"	"													$\overline{WAIT}$	"	"	"
43			"	"							2.4 V	"													CLK	"	"	"
44			2.4 V	"							5.1 V	"													$\overline{BUSRQ}$	"	"	"
45			0.8 V	"							"	"													AD_0	"	"	"
46			"	"							"	"													AD_9	"	"	"
47			"	"							"	"													AD_{10}	"	"	"
48			"	"							"	"													AD_{11}	"	"	"
49			"	"							"	"													AD_{12}	"	"	"
50			"	"							"	"													AD_{13}	"	"	"
51			"	"							"	"													AD_{15}	"	"	"
52			"	"							"	"													AD_{14}	"	"	"
53			"	"							"	"		0.4 V											AD_1	"	"	"
54			"	"							"	"			0.4 V										AD_2	"	"	"
55			"	"							"	"				0.4 V									AD_3	"	"	"
56			"	"							"	"					0.4 V								AD_5	"	"	"
57			"	"							"	"							0.4 V						AD_4	"	"	"
58			"	"							"	"								0.4 V					AD_6	"	"	"
59			"	"							"	"									0.4 V				AD_7	"	"	"
60			"	"							"	"												0.4 V	AD_8	"	"	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883-method	Test no.	1 AD_0	2 AD_9	3 AD_{10}	4 AD_{11}	5 AD_{12}	6 AD_{13}	7 $\overline{STOP}$	8 $\overline{MI}$	9 AD_{15}	10 AD_{14}	11 V_{CC}	12 $\overline{VI}$	13 $\overline{NVI}$	14 $\overline{SEGT}$	15 $\overline{NMI}$	16 $\overline{RESET}$	17 $\overline{MO}$	18 $\overline{MREQ}$	19 $\overline{DS}$	20 ST_3	21 ST_2	22 ST_1	23 ST_0	24 SN_3
1 $T_C = 25°C$	I_{IL} 1/		61							2.4 V	2.4 V	0.4 V		5.5 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V				0.4 V				
			62							"	"		0.4 V	"	"	"	"	"	"					0.4 V			
			63							"	"			"	"	"	"	"	"						0.4 V		
			64							"	"			"	"	"	"	"	"								0.4 V
			65							"	"			"	"	"	"	"	"								
			66							"	"			"	"	"	"	"	"								
			67							"	"			"	"	"	"	"	"								
			68							"	"			"	"	"	"	"	"								
			69							"	"			"	"	"	"	"	"								
			70							"	"			"	"	"	"	"	"								
			71							"	"			"	"	"	"	"	"		0.4 V						
			72							"	"			"	"	"	"	"	"								
			73							"	"			"	"	"	"	"	"								
			74							"	"			"	"	"	"	"	"								
			75							"	"			"	"	"	"	"	"			0.4 V					
			76							"	"			"	"	"	"	"	"								
			77							"	"			"	"	"	"	"	"								
	I_{IL} 1/		78							0.4 V				"	"	"	"	"	"								
			79							2.4 V	0.4 V			"	"	"	"	"	"								
			80							"	2.4 V			"	0.4 V		"	"	"								
			81							"	"			"	2.4 V	0.4 V	0.4 V	"	"								
			82							"	"			"	"	2.4 V	2.4 V	0.4 V	"								
			83							"	"			"	"	"	"	2.4 V	0.4 V								
			84							"	"			"	"	"	"	"	2.4 V								
			85							"	"			"	"	"	"	"	"								
			86							"	"			"	"	"	"	"	"								
			87							"	"			"	"	"	"	"	"								
	V_{OL}		88	2.0 mA						"	"			4.5 V	"	"	"	"	"								
			89		2.0 mA					"	"			"	"	"	"	"	"								
			90			2.0 mA				"	"			"	"	"	"	"	"								
			91				2.0 mA			"	"			"	"	"	"	"	"								
			92					2.0 mA		"	"			"	"	"	"	"	"								
			93						2.0 mA	"	"			"	"	"	"	"	"								
			94							"	"	2.0 mA		"	"	"	"	"	"								
			95							"	"		2.0 mA	"	"	"	"	"	"								
			96							"	"			"	"	"	"	"	"								
			97							"	"			"	"	"	"	"	"								
			98							"	"			"	"	"	"	"	"								
			99							"	"			"	"	"	"	"	"								
			100							"	"			"	"	"	"	"	"								
			101							"	"			"	"	"	"	"	"								
			102							"	"			"	"	"	"	"	"				2.0 mA				
			103							"	"			"	"	"	"	"	"					2.0 mA			
			104							"	"			"	"	"	"	"	"						2.0 mA		
			105							"	"			"	"	"	"	"	"							2.0 mA	
			106							"	"			"	"	"	"	"	"								2.0 mA
			107							"	"			"	"	"	"	"	"								
			108							"	"			"	"	"	"	"	"								
			109							"	"			"	"	"	"	"	"								
			110							"	"			"	"	"	"	"	"								
			111							"	"			"	"	"	"	"	"								
			112							"	"			"	"	"	"	"	"								
			113							"	"			"	"	"	"	"	"								
			114							"	"			"	"	"	"	"	"	2.0 mA							
			115							"	"			"	"	"	"	"	"		2.0 mA						
			116							"	"			"	"	"	"	"	"			2.0 mA					
			117							"	"			"	"	"	"	"	"								
			118							"	"			"	"	"	"	"	"								
			119							"	"			"	"	"	"	"	"								
			120							"	"			"	"	"	"	"	"								
			121							"	"			"	"	"	"	"	"								
			122							"	"			"	"	"	"	"	"								

See footnotes at end of device types 01 and 03

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.	25 SN_1	26 SN_0	27 BUSRQ	28 WAIT	29 BUSAK	30 R/W	31 N/S	32 B/W	33 NC	34 AS	35 CLK	36 GND	37 SN_2	38 AD_1	39 AD_2	40 AD_3	41 AD_5	42 SN_4	43 AD_4	44 AD_6	45 AD_7	46 SN_5	47 SN_6	48 AD_8	Measured terminal	Test Limits Min	Test Limits Max	Unit
61			0.8 V	2.4 V							5.1 V	GND													ST_3	-10	10	μA
62			"	"							"	"													ST_2	"	"	"
63			"	"							"	"													ST_1	"	"	"
64			"	"							"	"													ST_0	"	"	"
65			"	"							"	"													SN_3	"	"	"
66	0.4 V		"	"							"	"													SN_1	"	"	"
67		0.4 V	"	"							"	"													SN_0	"	"	"
68			"	"							"	"	0.4 V												SN_2	"	"	"
69			"	"							"	"						0.4 V							SN_4	"	"	"
70			"	"							"	"										0.4 V			SN_5	"	"	"
71			"	"							"	"											0.4 V		SN_6	"	"	"
72			"	"							"	"													$\overline{MREQ}$	"	"	"
73			"	"		0.4 V					"	"													R/W	"	"	"
74			"	"			0.4 V				"	"													N/S	"	"	"
75			"	"				0.4 V			"	"													B/W	"	"	"
76			"	"							"	"													$\overline{DS}$	"	"	"
77			"	"						0.4 V	"	"													AS	"	"	"
78			"	"							"	"													$\overline{STOP}$	"	"	"
79			"	"							"	"													$\overline{MI}$	"	"	"
80			"	"							"	"													$\overline{VI}$	"	"	"
81			"	"							"	"													$\overline{NVI}$	"	"	"
82			"	"							"	"													$\overline{SEGT}$	"	"	"
83			"	"							"	"													$\overline{NMI}$	"	"	"
84			"	"							"	"													$\overline{RESET}$	"	"	"
85			"	0.4 V							"	"													WAIT	"	"	"
86			"	2.4 V							0.4 V	"													CLK	"	"	"
87			0.4 V	"							5.1 V	"													$\overline{BUSRQ}$	"	"	"
88			2.4 V	"							4.1 V	0V													AD_0		0.4	V
89			"	"							"	"													AD_9		"	"
90			"	"							"	"													AD_{10}		"	"
91			"	"							"	"													AD_{11}		"	"
92			"	"							"	"													AD_{12}		"	"
93			"	"							"	"													AD_{13}		"	"
94			"	"							"	"													AD_{15}		"	"
95			"	"							"	"													AD_{14}		"	"
96			"	"							"	"		2.0 mA											AD_1		"	"
97			"	"							"	"			2.0 mA										AD_2		"	"
98			"	"							"	"				2.0 mA									AD_3		"	"
99			"	"							"	"					2.0 mA								AD_5		"	"
100			"	"							"	"							2.0 mA						AD_4		"	"
101			"	"							"	"								2.0 mA					AD_6		"	"
102			"	"							"	"									2.0 mA				AD_7		"	"
103			"	"							"	"												2.0 mA	AD_8		"	"
104			"	"							"	"													ST_3		"	"
105			"	"							"	"													ST_2		"	"
106			"	"							"	"													ST_1		"	"
107			"	"							"	"													ST_0		"	"
108			"	"							"	"													SN_3		"	"
109	2.0 mA		"	"							"	"													SN_1		"	"
110		2.0 mA	"	"							"	"													SN_0		"	"
111			"	"							"	"	2.0 mA												SN_2		"	"
112			"	"							"	"						2.0 mA							SN_4		"	"
113			"	"							"	"										2.0 mA			SN_5		"	"
114			"	"							"	"											2.0 mA		SN_6		"	"
115			"	"							"	"													$\overline{RD}$		"	"
116			"	"							"	"													$\overline{MREQ}$		"	"
117			"	"							"	"													$\overline{DS}$		"	"
118			"	"		2.0 mA					"	"													R/W		"	"
119			"	"			2.0 mA				"	"													N/S		"	"
120			"	"				2.0 mA			"	"													B/W		"	"
121			"	"						2.0 mA	"	"													$\overline{AS}$		"	"
122			"	"	2.0 mA						"	"													$\overline{BUSAK}$		"	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883-method	Test no.	1 AD_0	2 AD_9	3 AD_{10}	4 AD_{11}	5 AD_{12}	6 AD_{13}	7 STOP	8 MI	9 AD_{15}	10 AD_{14}	11 V_{CC}	12 VI	13 NVI	14 SEGT	15 NMI	16 RESET	17 MO	18 MREQ	19 DS	20 ST_3	21 ST_2	22 ST_1	23 ST_0	24 SM_3
1 T_C = 25°C	V_{OH}		123	-250 μA						2.4 V	2.4 V			4.5 V	2.4 V	2.4 V	2.4 V	2.4 V	2.4 V								
			124		-250 μA					"	"			"	"	"	"	"	"								
			125			-250 μA				"	"			"	"	"	"	"	"								
			126				-250 μA			"	"			"	"	"	"	"	"								
			127					-250 μA		"	"			"	"	"	"	"	"								
			128						-250 μA	"	"			"	"	"	"	"	"								
			129							"	"	-250 μA		"	"	"	"	"	"								
			130							"	"		-250 μA	"	"	"	"	"	"								
			131							"	"			"	"	"	"	"	"								
			132							"	"			"	"	"	"	"	"								
			133							"	"			"	"	"	"	"	"								
			134							"	"			"	"	"	"	"	"								
			135							"	"			"	"	"	"	"	"								
			136							"	"			"	"	"	"	"	"								
			137							"	"			"	"	"	"	"	"								
			138							"	"			"	"	"	"	"	"				-250 μA				
			139							"	"			"	"	"	"	"	"					-250 μA			
			140							"	"			"	"	"	"	"	"						-250 μA		
			141							"	"			"	"	"	"	"	"							-250 μA	
			142							"	"			"	"	"	"	"	"								-250 μA
			143							"	"			"	"	"	"	"	"								
			144							"	"			"	"	"	"	"	"								
			145							"	"			"	"	"	"	"	"								
			146							"	"			"	"	"	"	"	"								
			147							"	"			"	"	"	"	"	"								
			148							"	"			"	"	"	"	"	"								
			149							"	"			"	"	"	"	"	"	-250 μA							
			150							"	"			"	"	"	"	"	"		-250 μA						
			151							"	"			"	"	"	"	"	"			-250 μA					
			152							"	"			"	"	"	"	"	"								
			153							"	"			"	"	"	"	"	"								
			154							"	"			"	"	"	"	"	"								
			155							"	"			"	"	"	"	"	"								
			156							"	"			"	"	"	"	"	"								
			157							"	"			"	"	"	"	"	"								
2	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C and I_{CC} = 220 mA.																										
3	Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C and I_{CC} = 350 mA.																										
4 T_C = 25°C	C_{I1}		158	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	"	"	"	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.8 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V
	C_{I2}		159	"	"	"	"	"	"	2/	0.0 V	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"
			160	"	"	"	"	"	"	0.0 V	2/	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"
			161	"	"	"	"	"	"	"	0.0 V	"	"	"	2/	"	"	"	"	"	"	"	"	"	"	"	"
			162	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"
			163	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"
			164	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"
			165	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"
			166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"	"	"	"	"	"
			167	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_{I3}		168	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			169	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			171	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			172	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			173	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			175	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			176	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			177	"	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			178	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			179	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			180	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			181	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			182	"	"	"	"	"	0.0 V	"	"	"	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			183	"	"	"	"	"	0.0 V	"	"	2/	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.	25 SN_1	26 SN_0	27 BUSRQ	28 WAIT	29 BUSAK	30 R/W	31 M/S	32 B/W	33 NC	34 AS	35 CLK	36 GND	37 SN_2	38 AD_1	39 AD_2	40 AD_3	41 AD_5	42 SN_4	43 AD_4	44 AD_6	45 AD_7	46 SN_5	47 SN_6	48 AD_8	Measured terminal	Test Limits Min	Test Limits Max	Unit
123			2.4 V	2.4 V							4.1 V	0.0 V													AD_0	2.4		V
124			"	"							"	"													AD_9	"		"
125			"	"							"	"													AD_{10}	"		"
126			"	"							"	"													AD_{11}	"		"
127			"	"							"	"													AD_{12}	"		"
128			"	"							"	"													AD_{13}	"		"
129			"	"							"	"													AD_{15}	"		"
130			"	"							"	"													AD_{14}	"		"
131			"	"							"	"		-250 μA											AD_1	"		"
132			"	"							"	"			-250 μA										AD_2	"		"
133			"	"							"	"				-250 μA									AD_3	"		"
134			"	"							"	"					-250 μA								AD_5	"		"
135			"	"							"	"							-250 μA						AD_4	"		"
136			"	"							"	"								-250 μA					AD_6	"		"
137			"	"							"	"									-250 μA				AD_7	"		"
138			"	"							"	"												-250 μA	AD_8	"		"
139			"	"							"	"													ST_3	"		"
140			"	"							"	"													ST_2	"		"
141			"	"							"	"													ST_1	"		"
142			"	"							"	"													ST_0	"		"
143	-250 μA		"	"							"	"													SM_3	"		"
144		-250 μA	"	"							"	"													SM_1	"		"
145			"	"							"	"	-250 μA												SM_0	"		"
146			"	"							"	"						-250 μA							SM_2	"		"
147			"	"							"	"										-250 μA			SM_4	"		"
148			"	"							"	"											-250 μA		SM_5	"		"
149			"	"							"	"													SM_6	"		"
150			"	"							"	"													$\overline{MO}$	"		"
151			"	"							"	"													$\overline{MREQ}$	"		"
152			"	"		-250 μA					"	"													$\overline{DS}$	"		"
153			"	"			-250 μA				"	"													$R/\overline{W}$	"		"
154			"	"				-250 μA			"	"													$M/\overline{S}$	"		"
155			"	"						-250 μA	"	"													$B/\overline{W}$	"		"
156			"	"	-250 μA						"	"													$\overline{AS}$	"		"
157																									$\overline{BUSAK}$	"		"
158	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	2/	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	CLK		50	pF
159	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{SIOP}$		10	"
160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{MI}$		"	"
161	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{VI}$		"	"
162	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{NVI}$		"	"
163	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{SEGT}$		"	"
164	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{NMI}$		"	"
165	"	"	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{RESET}$		"	"
166	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{BUSRQ}$		"	"
167																									$\overline{WAIT}$			
168	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_0		25	"
169	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	"	"	"	"	"	"	"	"	"	"	AD_1		"	"
170	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	AD_2		"	"
171	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	AD_3		"	"
172	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	2/	"	"	"	"	"	AD_4		"	"
173	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	"	0.0 V	"	"	"	"	"	AD_5		"	"
174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	2/	"	"	"	"	AD_6		"	"
175	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	AD_7		"	"
176	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	2/	AD_8		"	"
177	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	AD_9		"	"
178	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{10}		"	"
179	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{11}		"	"
180	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{12}		"	"
181	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{13}		"	"
182	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{14}		"	"
183	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{15}		"	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883-method	Test no.	1 AD_0	2 A_{D9}	3 AD_{10}	4 AD_{11}	5 AD_{12}	6 AD_{13}	7 $\overline{STOP}$	8 $\overline{MI}$	9 AD_{15}	10 AD_{14}	11 V_{CC}	12 $\overline{VI}$	13 $\overline{NVI}$	14 $\overline{SEGT}$	15 $\overline{NMI}$	16 $\overline{RESET}$	17 $\overline{MO}$	18 $\overline{MREQ}$	19 $\overline{DS}$	20 ST_3	21 ST_2	22 ST_1	23 ST_0	24 SN_3
4 $T_C = 25°C$	C_0		184	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.8 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V
			185	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			186	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/
			187	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V
			188	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			189	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	"
			190	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	0.0 V	"
			191	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			192	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	0.0 V	"	"
			193	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"
			194	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			195	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			196	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			197	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			198	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			199	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	"	"	"	"	"	"	"
			200	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"
			201	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	0.0 V	2/	"	"	"	"	"
			202	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
7	3/ 3A/	3014	See 6.2 and table V.																								
8	Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C and T_C = -55°C 3/ 3A/																										
9	3/ 3A/ 4/ 5/																										
10	3/ 3A/ 4/ 5/																										
11	3/ 3A/ 4/ 5/																										

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 - Continued.
Terminal conditions (pins not designated are open)

Test no.	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	Measured terminal	Test Limits Min	Test Limits Max	Unit
	SN_1	SN_0	BUSRQ	WAIT	BUSAK	R/W	M/S	B/W	NC	AS	CLK	GND	SN_2	AD_1	AD_2	AD_3	AD_5	SN_4	AD_4	AD_6	AD_7	SN_5	SN_6	AD_8				
184	0.0 V	2/	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	SN_0		15	pF
185	2/	0.0 V	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	SN_1		"	"
186	0.0 V	"	"	"	"	"	"	"	"	"	"	"	2/	"	"	"	"	"	"	"	"	"	"	"	SN_2		"	"
187	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	SN_3		"	"
188	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	"	"	"	"	"	"	SN_4		"	"
189	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"	2/	"	"	SN_5		"	"
190	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	SN_6		"	"
191	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	ST_0		"	"
192	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	ST_1		"	"
193	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	ST_2		"	"
194	"	"	"	"	"	"	"	"	"	"	"	"								"	"	"	"	"	ST_3		"	"
195	"	"	"	"	2/	"	"	"	"	"	"	"								"	"	"	"	"	$\overline{BUSAK}$		"	"
196	"	"	"	"	0.0 V	2/	"	"	"	"	"	"								"	"	"	"	"	R/$\overline{W}$		"	"
197	"	"	"	"	"	0.0 V	2/	"	"	"	"	"								"	"	"	"	"	M/$\overline{S}$		"	"
198	"	"	"	"	"	"	0.0 V	2/	"	"	"	"								"	"	"	"	"	B/$\overline{W}$		"	"
199	"	"	"	"	"	"	"	0.0 V	"	2/	"	"								"	"	"	"	"	$\overline{AS}$		"	"
200	"	"	"	"	"	"	"	"	"	0.0 V	"	"								"	"	"	"	"	$\overline{MO}$		"	"
201	"	"	"	"	"	"	"	"	"	"	"	"								"	"	"	"	"	$\overline{MREQ}$		"	"
202	"	"	"	"	"	"	"	"	"	"	"	"								"	"	"	"	"	$\overline{DS}$		"	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-01		-03		Unit
	Symbol	Terminal			Min	Max	Min	Max	
203 8/	t_{PWH7}	$\overline{MREQ}$	6	19	210		135		ns
204 8/	t_{PWL2}	$\overline{AS}$	"	29	85		55		"
205 8/	t_{PWL3}	$\overline{DS}$	"	38	275		185		"
206 8/	t_{PWL4}	$\overline{DS}$	"	40	185		110		"
207 8/	t_{PWL5}	$\overline{DS}$	"	43	410		255		"
208 6/	t_{PLH1} t_{PHL1}	SN_0 - SN_6	"	6		130		110	"
209 6/	t_{PLH2} t_{PHL2}	SN_0 - SN_6	"	7	20		10		"
210 6/	t_{PLH3} t_{PHL3}	AD_0 - AD_{15}	"	9		100		75	"
211 6/ 8/	t_{PLH4} t_{PHL4}	AD_0 - AD_{15}	"	11	455		305		"
212 6/ 8/	t_{PZL1} t_{PZH1}	AD_0 - AD_{15}	"	13	80		40		"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-01		-03		Unit
	Symbol	Terminal			Min	Max	Min	Max	
213 6/ 8/	t_{PLZ1} t_{PHZ1}	AD_0 - AD_{15}	6	20	70		35		ns
214 6/ 8/	t_{PLZ2} t_{PHZ2}	AD_0 - AD_{15}	"	30	60		30		"
215 6/	t_{PLZ3} t_{PHZ3}	AD_0 - AD_{15}	"	10		90		75	"
216	t_{PLZ4} t_{PHZ4}	$\overline{AS}$, SN_0 - SN_6, $\overline{DS}$, B/$\overline{W}$, AD_0 - AD_{15}, R/$\overline{W}$, N/$\overline{S}$, $\overline{MREQ}$, ST_0 - ST_3	"	8		90		75	"
217 6/ 8/	t_{PLH5} t_{PHL5}	AD_0 - AD_{15}	"	22	350		225		"
218 6/ 8/	t_{PLH6} t_{PHL6}	AD_0 - AD_{15}	"	27	340		215		"
219 6/ 8/	t_{PLH7} t_{PHL7}	AD_0 - AD_{15}	"	33	185		130		"
220 6/ 8/	t_{PLH8} t_{PHL8}	AD_0 - AD_{15}	"	41	320		200		"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-01		-03		Unit
	Symbol	Terminal			Min	Max	Min	Max	
221 6/ 8/	t_{PLH9} t_{PHL9}	AD_0 - AD_{15}	6	46	435		295		ns
222 6/	t_{PLH10} t_{PHL10}	AD_0 - AD_{15}	"	14		100		75	"
223 6/ 8/	t_{PLH11} t_{PHL11}	AD_0 - AD_{15}	"	35	75		45		"
224	t_{PLH12} t_{PHL12}	$R/\overline{W}$, $B/\overline{W}$, ST_0 - ST_3, $N/\overline{S}$	"	47		110		85	"
225	t_{PLH13} t_{PHL13}	$\overline{MO}$	"	59		120		85	"
226 8/	t_{PLH14}	$\overline{DS}$	"	16	295		195		"
227 8/	t_{PHL14}	$\overline{DS}$	"	21	55		35		"
228	t_{PHL15}	$\overline{DS}$	"	31	0		0		"
229 8/	t_{PHL16}	$\overline{DS}$	"	32	70		35		"
230	t_{PLH28}	$\overline{DS}$	"	34		70		65	"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-01		-03		Unit
	Symbol	Terminal			Min	Max	Min	Max	
231 8/	t_{PHL17}	$\overline{DS}$	6	36	180		110		ns
232	t_{PHL18}	$\overline{DS}$	"	37		120		85	"
233	t_{PHL19}	$\overline{DS}$	"	39		95		80	"
234	t_{PHL20}	$\overline{DS}$	"	42		120		100	"
235 8/	t_{PHL21}	$\overline{DS}$	"	44	1,065		690		"
236	t_{PHL22}	$\overline{DS}$	"	45		120		85	"
237 8/	t_{PHL23}	$\overline{MREQ}$	"	17	55		35		"
238	t_{PHL24}	$\overline{MREQ}$	"	18		80		70	"
239	t_{PLH24}	$\overline{MREQ}$	"	23		80		60	"
240	t_{PHL25}	$\overline{AS}$	"	24		80		60	"
241 8/	t_{PLH29}	$\overline{AS}$	"	25	55		35		"

See footnotes at end of device types 01 and 03.

TABLE III. Group A inspection for device types 01 and 03 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-01		-03		Unit
	Symbol	Terminal			Min	Max	Min	Max	
242	t_{PLH30}	$\overline{AS}$	6	26		90		80	ns
243 8/	t_{PHL26}	$\overline{AS}$	"	28	70		35		"
244 8/	t_{PLH31}	$\overline{AS}$	"	48	60		30		"
245	t_{PLH27}	$\overline{BUSAK}$	"	66		100		75	"
246	t_{PHL27}	$\overline{BUSAK}$	"	67		100		75	"

1/ Apply input conditions and pulse CLK until $\overline{BUSAK}$ is low.

2/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

3/ For subgroups 7, 8, 9, 10, 11, and 12 tests input conditions A, B, C, D, E, F, G, and H appear in table IV (see footnotes 7 and 10).

3A/ For subgroups 7, 8, 9, 10, and 11 tests output conditions AO, BO, CO, DO, EO, FO, GO, and HO appear in table IV.

4/ Figure 6 represents the timing diagrams associated with subgroups 7, 8, 9, 10, 11, and 12.

5/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.

6/ Where propagation delay tests for subgroup 12 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst case delay requires recording. In some cases this will be a minimum reading, while in others it will be a maximum as indicated in the table.

7/ For subgroup 12 input conditions A-D will each be individually used when making measurements for device type 01. Input conditions E-H will each be individually used for device type 03.

8/ These reference number parameters are dependent upon clock high or clock low or clock cycle time. The limits provided are at maximum frequency. To determine the limits at other frequencies use the equations in footnote 5 of table I herein.

9/ The reference number refers to the position where the parameter being measured appears on figure 6.

10/ Subgroup 12 tests are the only tests for which an ac data value is actually recorded. Subgroups 7, 8, 9, 10, and 11 are pass/fail tests and shall be checked by an automated tester controlled by the test software represented in table V using input and output conditions of table IV.

11/ Limits shown for subgroup 12 are from f_{MAX} input conditions A, B, E, and F of table IV. The limits for f_{MIN} input conditions C, D, G, and H are not shown.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				AD_9	AD_{10}	AD_{11}	AD_{12}	AD_{13}	$\overline{STOP}$	$\overline{MI}$	AD_{15}	AD_{14}	V_{CC}	$\overline{VI}$	$\overline{NVI}$	$\overline{NMI}$	$\overline{RESET}$	$\overline{MO}$	$\overline{MREQ}$	$\overline{DS}$	ST_3	ST_2	ST_1
1 $T_C = 25°C$	I_{CC}	3005	1						2.0 V	2.0 V			5.5 V	2.0 V	2.0 V	2.0 V	2.0 V						
	I_{IH} 1/		2	2.4 V					"	"			"	"	"	"	"						
			3		2.4 V				"	"			"	"	"	"	"						
			4			2.4 V			"	"			"	"	"	"	"						
			5				2.4 V		"	"			"	"	"	"	"						
			6					2.4 V	"	"			"	"	"	"	"						
			7						"	"	2.4 V		"	"	"	"	"						
			8						"	"			"	"	"	"	"						
			9						"	"		2.4 V	"	"	"	"	"						
			10						"	"			"	"	"	"	"						
			11						"	"			"	"	"	"	"						
			12						"	"			"	"	"	"	"						
			13						"	"			"	"	"	"	"						
			14						"	"			"	"	"	"	"						
			15						"	"			"	"	"	"	"						
			16						"	"			"	"	"	"	"						
			17						"	"			"	"	"	"	"						
	I_{ZH}		18						"	"			"	"	"	"	"				2.4 V		
			19						"	"			"	"	"	"	"					2.4 V	
			20						"	"			"	"	"	"	"						2.4 V
			21						"	"			"	"	"	"	"						
			22						"	"			"	"	"	"	"		2.4 V				
			23						"	"			"	"	"	"	"						
			24						"	"			"	"	"	"	"						
			25						"	"			"	"	"	"	"						
			26						"	"			"	"	"	"	"			2.4 V			
			27						"	"			"	"	"	"	"						
	I_{IH}		28						2.4 V				"	"	"	"	"						
			29						2.4 V	2.4 V			"	"	"	"	"						
			30							2.4 V			"	2.4 V	"	"	"						
			31										"	"	2.4 V	"	"						
			32										"	"	"	2.4 V	"						
			33										"	"	"	"	2.4 V						
			34										"	"	"	"	"						
			35										"	"	"	"	"						
			36										"	"	"	"	"						
	I_{IL}		37	0.4 V									"	"	"	"	"						
			38		0.4 V								"	"	"	"	"						
			39			0.4 V							"	"	"	"	"						
			40				0.4 V						"	"	"	"	"						
			41					0.4 V					"	"	"	"	"						
			42								0.4 V		"	"	"	"	"						
			43									0.4 V	"	"	"	"	"						
			44										"	"	"	"	"						
			45										"	"	"	"	"						
			46										"	"	"	"	"						
			47										"	"	"	"	"						
			48										"	"	"	"	"						
			49										"	"	"	"	"						
			50										"	"	"	"	"						
			51										"	"	"	"	"						
			52										"	"	"	"	"						

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Min	Test limits Max	Unit
	ST_0	$\overline{BUSRQ}$	$\overline{WAIT}$	$\overline{BUSAK}$	R/$\overline{W}$	N/$\overline{S}$	B/$\overline{W}$	NC	$\overline{AS}$	CLK	GND	AD_1	AD_2	AD_3	AD_5	AD_4	AD_6	AD_7	AD_8	AD_0				
1		0.8 V	2.0 V							5.1 V	GND										V_{CC}			mA
2		"	"							"	"										AD_9	-10	10	μA
3		"	"							"	"										AD_{10}	"	"	"
4		"	"							"	"										AD_{11}	"	"	"
5		"	"							"	"										AD_{12}	"	"	"
6		"	"							"	"										AD_{13}	"	"	"
7		"	"							"	"										AD_{15}	"	"	"
8		"	"							"	"										AD_{14}	"	"	"
9		"	"							"	"	2.4 V									AD_1	"	"	"
10		"	"							"	"		2.4 V								AD_2	"	"	"
11		"	"							"	"			2.4 V							AD_3	"	"	"
12		"	"							"	"				2.4 V						AD_5	"	"	"
13		"	"							"	"					2.4 V					AD_4	"	"	"
14		"	"							"	"						2.4 V				AD_6	"	"	"
15		"	"							"	"							2.4 V			AD_7	"	"	"
16		"	"							"	"								2.4 V		AD_8	"	"	"
17		"	"							"	"									2.4 V	AD_0	"	"	"
18		"	"							"	"										ST_3	"	"	"
19		"	"							"	"										ST_2	"	"	"
20		"	"							"	"										ST_1	"	"	"
21	2.4 V	"	"							"	"										ST_0	"	"	"
22		"	"							"	"										$\overline{MREQ}$	"	"	"
23		"	"		2.4 V					"	"										R/$\overline{W}$	"	"	"
24		"	"			2.4 V				"	"										N/$\overline{S}$	"	"	"
25		"	"				2.4 V			"	"										B/$\overline{W}$	"	"	"
26		"	"							"	"										$\overline{DS}$	"	"	"
27		"	"						2.4 V	"	"										$\overline{AS}$	"	"	"
28		"	"							"	"										$\overline{STOP}$	"	"	"
29		"	"							"	"										$\overline{MI}$	"	"	"
30		"	"							"	"										$\overline{VI}$	"	"	"
31		"	"							"	"										$\overline{NVI}$	"	"	"
32		"	"							"	"										$\overline{NMI}$	"	"	"
33		"	"							"	"										$\overline{RESET}$	"	"	"
34		"	2.4 V							"	"										$\overline{WAIT}$	"	"	"
35		"	"							2.4 V	"										CLK	"	"	"
36		2.4 V	"							5.1 V	"										$\overline{BUSRQ}$	"	"	"
37		0.8 V	"							"	"										AD_9	"	"	"
38		"	"							"	"										AD_{10}	"	"	"
39		"	"							"	"										AD_{11}	"	"	"
40		"	"							"	"										AD_{12}	"	"	"
41		"	"							"	"										AD_{13}	"	"	"
42		"	"							"	"										AD_{15}	"	"	"
43		"	"							"	"										AD_{14}	"	"	"
44		"	"							"	"	0.4 V									AD_1	"	"	"
45		"	"							"	"		0.4 V								AD_2	"	"	"
46		"	"							"	"			0.4 V							AD_3	"	"	"
47		"	"							"	"				0.4 V						AD_5	"	"	"
48		"	"							"	"					0.4 V					AD_4	"	"	"
49		"	"							"	"						0.4 V				AD_6	"	"	"
50		"	"							"	"							0.4 V			AD_7	"	"	"
51		"	"							"	"								0.4 V		AD_8	"	"	"
52		"	"							"	"									0.4 V	AD_0	"	"	"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				AD_9	AD_{10}	AD_{11}	AD_{12}	AD_{13}	$\overline{STOP}$	$\overline{MI}$	AD_{15}	AD_{14}	V_{CC}	$\overline{VI}$	$\overline{NVI}$	$\overline{NMI}$	$\overline{RESET}$	$\overline{MO}$	$\overline{MREQ}$	$\overline{DS}$	ST_3	ST_2	ST_1
1 T_C = 25°C	I_{ZL}		53						2.4 V	2.4 V			5.5 V	2.4 V	2.4 V	2.4 V	2.4 V				0.4 V		
			54						"	"			"	"	"	"	"					0.4 V	
			55						"	"			"	"	"	"	"						0.4 V
			56						"	"			"	"	"	"	"						
			57						"	"			"	"	"	"	"		0.4 V				
			58						"	"			"	"	"	"	"						
			59						"	"			"	"	"	"	"						
			60						"	"			"	"	"	"	"						
			61						"	"			"	"	"	"	"						
			62						"	"			"	"	"	"	"			0.4 V			
	I_{IL}		63						0.4 V	"			"	"	"	"	"						
			64						2.4 V	0.4 V			"	"	"	"	"						
			65						"	2.4 V			"	0.4 V	"	"	"						
			66						"	"			"	2.4 V	0.4 V	"	"						
			67						"	"			"	"	2.4 V	0.4 V	"						
			68						"	"			"	"	"	2.4 V	0.4 V						
			69						"	"			"	"	"	"	2.4 V						
			70						"	"			"	"	"	"	"						
			71						"	"			"	"	"	"	"						
	V_{OL}		72	2.0 mA					"	"			4.5 V	"	"	"	"						
			73		2.0 mA				"	"			"	"	"	"	"						
			74			2.0 mA			"	"			"	"	"	"	"						
			75				2.0 mA		"	"			"	"	"	"	"						
			76					2.0 mA	"	"			"	"	"	"	"						
			77						"	"	2.0 mA		"	"	"	"	"						
			78						"	"		2.0 mA	"	"	"	"	"						
			79						"	"			"	"	"	"	"						
			80						"	"			"	"	"	"	"						
			81						"	"			"	"	"	"	"						
			82						"	"			"	"	"	"	"						
			83						"	"			"	"	"	"	"						
			84						"	"			"	"	"	"	"						
			85						"	"			"	"	"	"	"						
			86						"	"			"	"	"	"	"						
			87						"	"			"	"	"	"	"						
			88						"	"			"	"	"	"	"				2.0 mA		
			89						"	"			"	"	"	"	"					2.0 mA	
			90						"	"			"	"	"	"	"						2.0 mA
			91						"	"			"	"	"	"	"						
			92						"	"			"	"	"	"	"		2.0 mA				
			93						"	"			"	"	"	"	"						
			94						"	"			"	"	"	"	"						
			95						"	"			"	"	"	"	"						
			96						"	"			"	"	"	"	"			2.0 mA			
			97						"	"			"	"	"	"	"						
			98						"	"			"	"	"	"	"	2.0 mA					
			99						"	"			"	"	"	"	"						
	V_{OH}		100	-250 μA					"	"			"	"	"	"	"						
			101		-250 μA				"	"			"	"	"	"	"						
			102			-250 μA			"	"			"	"	"	"	"						
			103				-250 μA		"	"			"	"	"	"	"						
			104					-250 μA	"	"			"	"	"	"	"						
			105						"	"	-250 μA		"	"	"	"	"						
			106						"	"		-250 μA	"	"	"	"	"						
			107						"	"			"	"	"	"	"						
			108						"	"			"	"	"	"	"						
			109						"	"			"	"	"	"	"						
			110						"	"			"	"	"	"	"						

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Min	Test limits Max	Unit
	ST_0	$\overline{BUSRQ}$	$\overline{WAIT}$	$\overline{BUSAK}$	R/W	N/$\overline{S}$	B/$\overline{W}$	NC	$\overline{AS}$	CLK	GND	AD_1	AD_2	AD_3	AD_5	AD_4	AD_6	AD_7	AD_8	AD_0				
53		0.8 V	2.4 V							5.1 V	GND										ST_3	-10	10	μA
54		"								"	"										ST_2	"	"	"
55		"								"	"										ST_1	"	"	"
56	0.4 V	"								"	"										ST_0	"	"	"
57		"								"	"										$\overline{MREQ}$	"	"	"
58		"			0.4 V					"	"										R/$\overline{W}$	"	"	"
59		"				0.4 V				"	"										N/$\overline{S}$	"	"	"
60		"					0.4 V			"	"										B/$\overline{W}$	"	"	"
61		"								"	"										$\overline{DS}$	"	"	"
62		"							0.4 V	"	"										$\overline{AS}$	"	"	"
63		"								"	"										$\overline{STOP}$	"	"	"
64		"								"	"										$\overline{MI}$	"	"	"
65		"								"	"										$\overline{VI}$	"	"	"
66		"								"	"										$\overline{NVI}$	"	"	"
67		"								"	"										$\overline{NMI}$	"	"	"
68		"								"	"										$\overline{RESET}$	"	"	"
69		"	0.4 V							"	"										$\overline{WAIT}$	"	"	"
70		"	2.4 V							0.4 V	"										CLK	"	"	"
71		0.4 V	2.4 V							5.1 V	"										$\overline{BUSRQ}$	"	"	"
72		2.4 V	"							4.1 V	0.0 V										AD_9		0.4	V
73		"	"							"	"										AD_{10}		"	"
74		"	"							"	"										AD_{11}		"	"
75		"	"							"	"										AD_{12}		"	"
76		"	"							"	"										AD_{13}		"	"
77		"	"							"	"										AD_{14}		"	"
78		"	"							"	"										AD_{15}		"	"
79		"	"							"	"	2.0 mA									AD_1		"	"
80		"	"							"	"		2.0 mA								AD_2		"	"
81		"	"							"	"			2.0 mA							AD_3		"	"
82		"	"							"	"				2.0 mA						AD_5		"	"
83		"	"							"	"					2.0 mA					AD_4		"	"
84		"	"							"	"						2.0 mA				AD_6		"	"
85		"	"							"	"							2.0 mA			AD_7		"	"
86		"	"							"	"								2.0 mA		AD_8		"	"
87		"	"							"	"									2.0 mA	AD_0		"	"
88		"	"							"	"										ST_3		"	"
89		"	"							"	"										ST_2		"	"
90		"	"							"	"										ST_1		"	"
91	2.0 mA	"	"							"	"										ST_0		"	"
92		"	"							"	"										$\overline{MREQ}$		"	"
93		"	"		2.0 mA					"	"										R/$\overline{W}$		"	"
94		"	"			2.0 mA				"	"										N/$\overline{S}$		"	"
95		"	"				2.0 mA			"	"										B/$\overline{W}$		"	"
96		"	"							"	"										$\overline{DS}$		"	"
97		"	"					2.0 mA		"	"										$\overline{AS}$		"	"
98		"	"							"	"										$\overline{MO}$		"	"
99		0.8 V	"	2.0 mA						"	"										$\overline{BUSAK}$		"	"
100		"	"							"	"										AD_9	2.4		"
101		"	"							"	"										AD_{10}	"		"
102		"	"							"	"										AD_{11}	"		"
103		"	"							"	"										AD_{12}	"		"
104		"	"							"	"										AD_{13}	"		"
105		"	"							"	"										AD_{15}	"		"
106		"	"							"	"										AD_{14}	"		"
107		"	"							"	"	-250 μA									AD_1	"		"
108		"	"							"	"		-250 μA								AD_2	"		"
109		"	"							"	"			-250 μA							AD_3	"		"
110		"	"							"	"				-250 μA						AD_5	"		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				AD_9	AD_{10}	AD_{11}	AD_{12}	AD_{13}	$\overline{STOP}$	$\overline{MI}$	AD_{15}	AD_{14}	V_{CC}	$\overline{VI}$	$\overline{NVI}$	$\overline{NMI}$	$\overline{RESET}$	$\overline{MO}$	$\overline{MREQ}$	$\overline{DS}$	ST_3	ST_2	ST_1
1 T_C = 25°C	V_{OH}		111						2.4 V	2.4 V			4.5 V	2.4 V	2.4 V	2.4 V	2.4 V						
			112						"	"			"	"	"	"	"						
			113						"	"			"	"	"	"	"						
			114						"	"			"	"	"	"	"						
			115						"	"			"	"	"	"	"						
			116						"	"			"	"	"	"	"				-250 μA		
			117						"	"			"	"	"	"	"					-250 μA	
			118						"	"			"	"	"	"	"						-250 μA
			119						"	"			"	"	"	"	"						
			120						"	"			"	"	"	"	"		-250 μA				
			121						"	"			"	"	"	"	"						
			122						"	"			"	"	"	"	"						
			123						"	"			"	"	"	"	"						
			124						"	"			"	"	"	"	"			-250 μA			
			125						"	"			"	"	"	"	"						
			126						"	"			"	"	"	"	"	-250 μA					
			127						"	"			"	"	"	"	"						
2			Same tests, terminal conditions, and limits as for subgroup 1, except T_C = +125°C, and I_{CC} = 220 mA.																				
3			Same tests, terminal conditions, and limits as for subgroup 1, except T_C = -55°C, and I_{CC} = 350 mA.																				
4 T_C = 25°C	C_{I1}		128	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V
	C_{I2}		129	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			130	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			131	"	"	"	"	"	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			132	"	"	"	"	"	0.0 V	2/	"	"	"	2/	"	"	"	"	"	"	"	"	"
			133	"	"	"	"	"	"	0.0 V	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"
			134	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"
			135	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"
			136	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"
	C_{I3}		137	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	"	"	"	"
			138	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			139	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			140	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			141	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			142	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			143	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			144	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			145	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			146	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			147	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			148	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			149	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			150	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			151	"	"	"	"	0.0 V	"	"	"	2/	"	"	"	"	"	"	"	"	"	"	"
			152	"	"	"	"	"	"	"	2/	0.0 V	"	"	"	"	"	"	"	"	"	"	"
	C_0		153	"	"	"	"	"	"	"	0.0 V	"	"	"	"	"	2/	"	"	"	"	"	"
			154	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	2/	"	"	"	"
			155	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	0.0 V	2/	"	"	"
			156	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"
			157	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"
			158	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/
			159	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V
			160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			161	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			162	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			163	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			164	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Min	Test limits Max	Unit
	ST_0	$\overline{BUSRQ}$	$\overline{WAIT}$	$\overline{BUSAK}$	R/$\overline{W}$	N/$\overline{S}$	B/$\overline{W}$	NC	$\overline{AS}$	CLK	GND	AD_1	AD_2	AD_3	AD_5	AD_4	AD_6	AD_7	AD_8	AD_0				
111		2.4 V	2.4 V	2.0 mA						4.1 V	0.0 V					-250 μA					AD_4	2.4		V
112		"	"	"						"	"						-250 μA				AD_6	"		"
113		"	"	"						"	"							-250 μA			AD_7	"		"
114		"	"	"						"	"								-250 μA		AD_8	"		"
115		"	"	"						"	"									-250 μA	AD_0	"		"
116		"	"	"						"	"										ST_3	"		"
117		"	"	"						"	"										ST_2	"		"
118		"	"	"						"	"										ST_1	"		"
119	-250 μA	"	"	"						"	"										ST_0	"		"
120		"	"	"						"	"										MREQ	"		"
121		"	"	"	-250 μA					"	"										R/W	"		"
122		"	"	"		-250 μA				"	"										N/S	"		"
123		"	"	"			-250 μA			"	"										B/W	"		"
124		"	"	"						"	"										DS	"		"
125		"	"	"					-250 μA	"	"										AS	"		"
126		"	"	"						"	"										MO	"		"
127		"	"	-250 μA						"	"										BUSAK	"		"
128	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	2/	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	CLK		50	pF
129	"	0.0 V	2/	"	"	"	"	"	"	0.0 V	"	"	"	"	"	"	"	"	"	"	$\overline{WAIT}$		10	"
130	"	2/	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{BUSRQ}$		"	"
131	"	0.0 V	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{STOP}$		"	"
132	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{MI}$		"	"
133	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{VI}$		"	"
134	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{NVI}$		"	"
135	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{NMI}$		"	"
136	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{RESET}$		"	"
137	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	AD_0		25	"
138	"	"	"	"	"	"	"	"	"	"	"	2/	"	"	"	"	"	"	"	0.0 V	AD_1		"	"
139	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	AD_2		"	"
140	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	AD_3		"	"
141	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	2/	"	"	"	"	AD_4		"	"
142	"	"	"	"	"	"	"	"	"	"	"	"	"	"	2/	0.0 V	"	"	"	"	AD_5		"	"
143	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	2/	"	"	"	AD_6		"	"
144	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	"	AD_7		"	"
145	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	2/	"	AD_8		"	"
146	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	0.0 V	"	AD_9		"	"
147	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{10}		"	"
148	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{11}		"	"
149	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{12}		"	"
150	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{13}		"	"
151	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{14}		"	"
152	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	AD_{15}		"	"
153	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{MO}$		15	"
154	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{MREQ}$		"	"
155	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	$\overline{DS}$		"	"
156	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	ST_3		"	"
157	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	ST_2		"	"
158	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	ST_1		"	"
159	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	ST_0		"	"
160	0.0 V	"	"	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	BUSAK		"	"
161	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	R/$\overline{W}$		"	"
162	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	"	N/$\overline{S}$		"	"
163	"	"	"	"	"	0.0 V	2/	"	"	"	"	"	"	"	"	"	"	"	"	"	B/$\overline{W}$		"	"
164	"	"	"	"	"	0.0 V	0.0 V	"	2/	"	"	"	"	"	"	"	"	"	"	"	$\overline{AS}$		"	"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04.
Terminal conditions (pins not designated are open).

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				AD_9	AD_{10}	AD_{11}	AD_{12}	AD_{13}	$\overline{STOP}$	$\overline{MI}$	AD_{15}	AD_{14}	V_{CC}	$\overline{VI}$	$\overline{NVI}$	$\overline{NMI}$	$\overline{RESET}$	$\overline{MO}$	$\overline{MREQ}$	$\overline{DS}$	ST_3	ST_2	ST_1
7	3/ 3A/	3014		See 6.2 and table VI.																			
8	3/ 3A/		Same tests, terminal conditions, and limits as for subgroup 7, except T_C = +125°C, and T_C = -55°C.																				
9	3/ 3A/ 4/ 5/																						
10	3/ 3A/ 4/ 5/		Repeat subgroup 9 at T_C = +125°C.																				
11	3/ 3A/ 4/ 5/		Repeat subgroup 9 at T_C = -55°C.																				

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 - Continued.
Terminal conditions (pins not designated are open).

Test no.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits		Unit
	ST_0	$\overline{BUSRQ}$	$\overline{WAIT}$	$\overline{BUSAK}$	R/$\overline{W}$	N/$\overline{S}$	B/$\overline{W}$	NC	$\overline{AS}$	CLK	GND	AD_1	AD_2	AD_3	AD_5	AD_4	AD_6	AD_7	AD_8	AD_0		Min	Max	

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-02		-04		Unit
	Symbol	Terminal			Min	Max	Min	Max	
165 8/	t_{PWH7}	$\overline{MREQ}$	6	19	210		135		ns
166 8/	t_{PWL2}	$\overline{AS}$	"	29	85		55		"
167 8/	t_{PWL3}	$\overline{DS}$	"	38	275		185		"
168 8/	t_{PWL4}	$\overline{DS}$	"	40	185		110		"
169 8/	t_{PWL5}	$\overline{DS}$	"	43	410		255		"
170 6/	t_{PLH3} t_{PHL3}	AD_0 - AD_{15}	"	9		100		75	"
171 6/ 8/	t_{PLH4} t_{PHL4}	AD_0 - AD_{15}	"	11	455		305		"
172 6/ 8/	t_{PZL1} t_{PZH1}	AD_0 - AD_{15}	"	13	80		40		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-02		-04		Unit
	Symbol	Terminal			Min	Max	Min	Max	
173 6/ 8/	t_{PLZ1} t_{PHZ1}	AD_0 - AD_{15}	6	20	70		35		ns
174 6/ 8/	t_{PLZ2} t_{PHZ2}	AD_0 - AD_{15}	"	30	60		30		"
175 6/	t_{PLZ3} t_{PHZ3}	AD_0 - AD_{15}	"	10		90		75	"
176	t_{PLZ4} t_{PHZ4}	$\overline{AS}$, SN_0 - SN_6, $\overline{DS}$, $B/\overline{W}$, AD_0 - AD_{15}, $R/\overline{W}$, $N/\overline{S}$, $\overline{MREQ}$, ST_0 - ST_3	"	8		90		75	"
177 6/ 8/	t_{PLH5} t_{PHL5}	AD_0 - AD_{15}	"	22	350		225		"
178 6/ 8/	t_{PLH6} t_{PHL6}	AD_0 - AD_{15}	"	27	340		215		"
179 6/ 8/	t_{PLH7} t_{PHL7}	AD_0 - AD_{15}	"	33	185		130		"
180 6/ 8/	t_{PLH8} t_{PHL8}	AD_0 - AD_{15}	"	41	320		200		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25°C and +125°C		Figure number 4/	Reference number 9/	-02		-04		Unit
	Symbol	Terminal			Min	Max	Min	Max	
181 6/ 8/	t_{PLH9} t_{PHL9}	AD_0 - AD_{15}	6	46	435		295		ns
182 6/	t_{PLH10} t_{PHL10}	AD_0 - AD_{15}	"	14		100		75	"
183 6/ 8/	t_{PLH11} t_{PHL11}	A_{D0} - AD_{15}	"	35	75		45		"
184	t_{PLH12} t_{PHL12}	R/$\overline{W}$, B/$\overline{W}$, ST_0 - ST_3, N/$\overline{S}$	"	47		110		85	"
185	t_{PLH13} t_{PHL13}	$\overline{MO}$	"	59		120		85	"
186 8/	t_{PLH14}	$\overline{DS}$	"	16	295		195		"
187 8/	t_{PHL14}	$\overline{DS}$	"	21	55		35		"
188	t_{PHL15}	$\overline{DS}$	"	31	0		0		"
189 8/	t_{PHL16}	$\overline{DS}$	"	32	70		35		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25° and +125°C		Figure number 4/	Reference number 9/	-02		-04		Unit
	Symbol	Terminal			Min	Max	Min	Max	
190	t_{PLH28}	$\overline{DS}$	6	34		70		65	ns
191 8/	t_{PHL17}	$\overline{DS}$	"	36	180		110		"
192	t_{PHL18}	$\overline{DS}$	"	37		120		85	"
193	t_{PHL19}	$\overline{DS}$	"	39		95		80	"
194	t_{PHL20}	$\overline{DS}$	"	42		120		100	"
195 8/	t_{PHL21}	$\overline{DS}$	"	44	1065		690		"
196	t_{PHL22}	$\overline{DS}$	"	45		120		85	"
197 8/	t_{PHL23}	$\overline{MREQ}$	"	17	55		35		"
198	t_{PHL24}	$\overline{MREQ}$	"	18		80		70	"
199	t_{PLH24}	$\overline{MREQ}$	"	23		80		60	"
200	t_{PHL25}	$\overline{AS}$	"	24		80		60	"
201 8/	t_{PLH29}	$\overline{AS}$	"	25	55		35		"

See footnotes at end of device types 02 and 04.

TABLE III. Group A inspection for device types 02 and 04 3/ - Continued.

Test number	10/ 11/ Subgroup 12, T_C = 25° and +125°C		Figure number 4/	Reference number 9/	-02		-04		Unit
	Symbol	Terminal			Min	Max	Min	Max	
202	t_{PLH30}	$\overline{AS}$	6	26		90		80	ns
203 8/	t_{PHL26}	$\overline{AS}$	"	28	70		35		"
204 8/	t_{PLH31}	$\overline{AS}$	"	48	60		30		"
205	t_{PLH27}	$\overline{BUSAK}$	"	66		100		75	"
206	t_{PHL27}	$\overline{BUSAK}$	"	67		100		75	"

See footnotes at end of device types 02 and 04.

1/ Apply input conditions and pulse CLK until BUSAK is low.

2/ The capacitance measurements shall be made between the indicated terminal and ground at a frequency of 1 MHz. The dc bias of the measuring instrument shall be less than ±0.1 V. The ac signal amplitude shall be less than 50 mV rms.

3/ For subgroups 7, 8, 9, 10, 11 and 12 tests input condiions A, B, C, D, E, F, G and H appear in table IV (see footnotes 7 and 10).

3A/ For subgroups 7, 8, 9, 10, and 11 tests output conditions AO, BO, CO, DO, EO, FO, GO, and HO appear in table IV.

4/ Figure 6 represents the timing diagrams associated with subgroups 7, 8, 9, 10, 11, and 12.

5/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.

6/ Where propagation delay tests for subgroup 12 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst case delay requires recording. In some cases this will be a minimum reading, while for others it will be a maximum as indicated in the table.

7/ For subgroup 12 input conditions A-D will each be individually used when making measurements for device type 02. Input conditions E-H will each be individually used for device type 04.

8/ These reference number parameters are dependent upon clock high or clock low or clock cycle time. The limits provided are at maximum frequency. To determine the limits at other frequencies use the equations in footnote 5 of table I herein.

9/ The reference number refers to the position where the parameter being measured appears on figure 6.

10/ Subgroup 12 tests are the only test for which an ac data value is actually recorded. Subgroups 7, 8, 9, 10, and 11 are pass/fail tests and shall be checked by an automated tester controlled by the test software represented in table V using input and output conditions in table IV.

11/ Limits shown in subgroup 12 are from f_{MAX} input conditions A, B, E, and F of table IV. The limits for f_{MIN} input conditions C, D, G, and H are not shown.

TABLE IV. Input conditions for device types 01 and 02 functional tests.

Symbol	Reference 2/	Terminal(s)	A 5/	B 5/	C 5/	D 5/	Unit
V_{CC}		V_{CC}	5.5	4.5	4.5	4.5	V
V_{IH2}		Logic inputs	2.4	2.4	2.4	2.4	V
V_{IL2}		Logic inputs	0.8	0.8	0.8	0.8	V
V_{IH1}		CLK	5.1	4.1	4.1	4.1	V
V_{IL1}		CLK	0.45	0.45	0.45	0.45	V
t_{cyc}	1	CLK	250	250	2,000	2,000	ns
t_{PWH1} 4/	2	CLK	105		105		ns
t_{PWL1} 4/	3	CLK		105		105	ns
t_{PWL6}	51	$\overline{NMI}$	100	100	100	100	ns
t_{SLH1}, t_{SHL1}	12	AD_0-AD_{15}	50	50	50	50	ns
t_{SLH2}, t_{SHL2}	49	$\overline{RESET}$	180	180	180	180	ns
t_{SLH3}, t_{SHL3}	53	$\overline{VI}$, $\overline{NVI}$	110	110	110	110	ns
t_{SLH5}, t_{SHL5}	57	$\overline{MI}$	180	180	180	180	ns
t_{SLH6}, t_{SHL6}	60	$\overline{STOP}$	140	140	140	140	ns
t_{SLH7}, t_{SHL7}	62	$\overline{WAIT}$	50	50	50	50	ns
t_{SLH8}, t_{SHL8}	64	$\overline{BUSRQ}$	90	90	90	90	ns
t_{SLH9}	52	$\overline{NMI}$	140	140	140	140	ns
t_{SLH4}, t_{SHL4} 3/	55	$\overline{SEGT}$	70	70	70	70	ns
t_{HLH3}, t_{HHL3} 3/	56	$\overline{SEGT}$	0	0	0	0	ns

See footnotes at end of device types 01 and 02.

TABLE IV. Input conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	A 5/	B 5/	C 5/	D 5/	Unit 5/
t_{HLZ1}, t_{HHZ1}	15	AD_0-AD_{15}	0	0	0	0	ns
t_{HLH1}, t_{HHL1}	50	$\overline{RESET}$	0	0	0	0	ns
t_{HLH2}, t_{HHL2}	54	$\overline{VI}$,$\overline{NVI}$	20	20	20	20	ns
t_{HLH4}, t_{HHL4}	58	$\overline{MI}$	0	0	0	0	ns
t_{HLH5}, t_{HHL5}	61	$\overline{STOP}$	0	0	0	0	ns
t_{HLH6}, t_{HHL6}	63	$\overline{WAIT}$	10	10	10	10	ns
t_{HLH7}, t_{HHL7}	65	$\overline{BUSRQ}$	10	10	10	10	ns

See footnotes at end of device types 01 and 02.

TABLE IV. Output conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	A0 6/	B0 6/	C0 6/	D0 6/	Unit 6/
V_{OH}		Outputs	2.0	2.0	2.0	2.0	V
V_{OL}		Outputs	0.8	0.8	0.8	0.8	V
t_{PWL2} 1/	29	$\overline{AS}$	85	85			ns
t_{PWL3} 1/	38	$\overline{DS}$	275	275			ns
t_{PWL4} 1/	40	$\overline{DS}$	185	185			ns
t_{PWL5} 1/	43	$\overline{DS}$	410	410			ns
t_{PWH7} 1/	19	$\overline{MREQ}$	210	210			ns
t_{PLH1}, t_{PHL1} 3/	6	SN_0-SN_6	130	130	130	130	ns
t_{PZL1}, t_{PZH1} 1/	13	AD_0-AD_{15}	80	80			ns
t_{PLZ1}, t_{PHZ1} 1/	20	AD_0-AD_{15}	70	70			ns
t_{PLH2}, t_{PHL2} 3/	7	SN_0-SN_6	20	20	20	20	ns
t_{PLZ2}, t_{PHZ2} 1/	30	AD_0-AD_{15}	60	60			ns
t_{PLH3}, t_{PHL3}	9	AD_0-AD_{15}	100	100	100	100	ns
t_{PLZ3}, t_{PHZ3} 1/	10	AD_0-AD_{15}	90	90	90	90	ns
t_{PLH4}, t_{PHL4} 1/	11	AD_0-AD_{15}	455	455			ns
t_{PLZ4}, t_{PHZ4} 1/ 3/	8	AD_0-AD_{15}, $\overline{AS}$, $\overline{DS}$, B/$\overline{W}$, R/$\overline{W}$, N/$\overline{S}$, $\overline{MREQ}$, ST_0-ST_3, SN_0-SN_6	90	90	90	90	ns
t_{PLH5}, t_{PHL5} 1/	22	AD_0-AD_{15}	350	350			ns
t_{PLH6}, t_{PHL6} 1/	27	AD_0-AD_{15}	340	340			ns
t_{PLH7}, t_{PHL7} 1/	33	AD_0-AD_{15}	185	185			ns

See footnotes at end of device types 01 and 02.

TABLE IV. Output conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	A0 6/	B0 6/	C0 6/	D0 6/	Unit
t_{PLH8} 1/ t_{PHL8}	41	AD_0-AD_{15}	320	320			ns
t_{PLH9} 1/ t_{PHL9}	46	AD_0-AD_{15}	435	435			ns
t_{PLH10} t_{PHL10}	14	AD_0-AD_{15}	100	100	100	100	ns
t_{PLH11} 1/ t_{PHL11}	35	AD_0 - AD_{15}	75	75			ns
t_{PLH12} t_{PHL12}	47	ST^0-ST_3	110	110	110	110	ns
t_{PLH13} t_{PHL13}	59	$\overline{MO}$	120	120	120	120	ns
t_{PLH14} 1/	16	$\overline{DS}$	295	295			ns
t_{PHL14} 1/	21	$\overline{DS}$	55	55			ns
t_{PHL15}	31	DS	0	0	0	0	ns
t_{PHL16} 1/	32	$\overline{DS}$	70	70			ns
t_{PHL17} 1/	36	$\overline{DS}$	180	180			ns
t_{PHL18}	37	$\overline{DS}$	120	120	120	120	ns
t_{PHL19}	39	$\overline{DS}$	95	95	95	95	ns
t_{PHL20}	42	$\overline{DS}$	120	120	120	120	ns
t_{PLH20}	66	$\overline{BUSAK}$	100	100	100	100	ns
t_{PHL21} 1/	44	$\overline{DS}$	1,065	1,065			ns
t_{PHL22}	45	$\overline{DS}$	120	120	120	120	ns
t_{PHL23} 1/	17	$\overline{MREQ}$	55	55			ns
t_{PHL24}	18	$\overline{MREQ}$	80	80	80	80	ns
t_{PLH24}	23	$\overline{MREQ}$	80	80	80	80	ns
t_{PHL25}	24	$\overline{AS}$	80	80	80	80	ns
t_{PLH28}	34	$\overline{DS}$	70	70	70	70	ns
t_{PLH29} 1/	25	$\overline{AS}$	55	55			ns

TABLE IV. Output conditions for device types 01 and 02 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	A0 6/	B0 6/	C0 6/	D0 6/	Unit
t_{PLH30}	26	$\overline{AS}$	90	90	90	90	ns
t_{PHL26} 1/	28	$\overline{AS}$	70	70			ns
t_{PHL27}	67	$\overline{BUSAK}$	100	100	100	100	ns
t_{PLH31} 1/	48	$\overline{AS}$	60	60			ns

1/ Limits for output conditions C and D are calculated using footnote 5 of table I herein. (These parameters are dependent upon the clock high, clock low or clock cycle time).

2/ The reference number refers to the position where the parameter being measured appears on figure 6.

3/ For device type 01 only.

4/ Clock input high or low or cycle times for device types 01 and 02 shall be 20 ns maximum.

5/ Input conditions A and B are at f_{MAX}, input conditions C and D are at f_{MIN}.

6/ Output conditions A0 and B0 are at f_{MAX}, output conditions C0 and D0 are at f_{MIN}.

TABLE IV. Input conditions for device types 03 and 04 functional tests.

Symbol	Reference 2/	Terminal(s)	E 5/	F 5/	G 5/	H 5/	Unit
V_{CC}		V_{CC}	5.5	4.5	4.5	4.5	V
V_{IH2}		Logic inputs	2.4	2.4	2.4	2.4	V
V_{IL2}		Logic inputs	0.8	0.8	0.8	0.8	V
V_{IH1}		CLK	5.1	4.1	4.1	4.1	V
V_{IL1}		CLK	0.45	0.45	0.45	0.45	V
t_{cyc}	1	CLK	165	165	2,000	2,000	ns
t_{PWH1} 4/	2	CLK	70		70		ns
t_{PWL1} 4/	3	CLK		70		70	ns
t_{PWL6}	51	$\overline{NMI}$	70	70	70	70	ns
t_{SLH1}, t_{SHL1}	12	AD_0-AD_{15}	20	20	20	20	ns
t_{SLH2}, t_{SHL2}	49	$\overline{RESET}$	70	70	70	70	ns
t_{SLH3}, t_{SHL3}	53	$\overline{VI}$, $\overline{NVI}$	50	50	50	50	ns
t_{SLH5}, t_{SHL5}	57	$\overline{MI}$	140	140	140	140	ns
t_{SLH6}, t_{SHL6}	60	$\overline{STOP}$	100	100	100	100	ns
t_{SLH7}, t_{SHL7}	62	$\overline{WAIT}$	30	30	30	30	ns
t_{SLH8}, t_{SHL8}	64	$\overline{BUSRQ}$	80	80	80	80	ns
t_{SLH9}	52	$\overline{NMI}$	70	70	70	70	ns
t_{SLH4}, t_{SHL4} 3/	55	$\overline{SEGT}$	55	55	55	55	ns
t_{HLH3}, t_{HHL3} 3/	56	$\overline{SEGT}$	0	0	0	0	ns
t_{HLZ1}, t_{HHZ1}	15	AD_0-AD_{15}	0	0	0	0	ns

See footnotes at end of device types 03 and 04.

TABLE IV. Input conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E 5/	F 5/	G 5/	H 5/	Unit
t_{HLH1} t_{HHL1}	50	$\overline{RESET}$	0	0	0	0	ns
t_{HLH2} t_{HHL2}	54	$\overline{VI}$, $\overline{NVI}$	20	20	20	20	ns
t_{HLH4} t_{HHL4}	58	$\overline{MI}$	0	0	0	0	ns
t_{HLH5} t_{HHL5}	61	$\overline{STOP}$	0	0	0	0	ns
t_{HLH6} t_{HHL6}	63	$\overline{WAIT}$	10	10	10	10	ns
t_{HLH7} t_{HHL7}	65	$\overline{BUSRQ}$	10	10	10	10	ns

See footnotes at end of device types 03 and 04.

TABLE IV. Output conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E0 6/	F0 6/	G0 6/	H0 6/	Unit
V_{OH}		Outputs	2.0	2.0	2.0	2.0	V
V_{OL}		Outputs	0.8	0.8	0.8	0.8	V
t_{PWL2} 1/	29	$\overline{AS}$	55	55			ns
t_{PWL3} 1/	38	$\overline{DS}$	185	185			ns
t_{PWL4} 1/	40	$\overline{DS}$	110	110			ns
t_{PWL5} 1/	43	$\overline{DS}$	255	255			ns
t_{PWH7} 1/	19	$\overline{MREQ}$	135	135			ns
t_{PLH1}, t_{PHL1} 3/	6	SN_0-SN_6	110	110	110	110	ns
t_{PZL1}, t_{PZH1} 1/	13	AD_0-AD_{15}	40	40			ns
t_{PLZ1}, t_{PHZ1} 1/	20	AD_0-AD_{15}	35	35			ns
t_{PLH2}, t_{PHL2} 3/	7	SN_0-SN_6	10	10	10	10	ns
t_{PLZ2}, t_{PHZ2} 1/	30	AD_0-AD_{15}	30	30			ns
t_{PLH3}, t_{PHL3}	9	AD_0-AD_{15}	75	75	75	75	ns
t_{PLZ3}, t_{PHZ3}	10	AD_0-AD_{15}	75	75	75	75	ns
t_{PLH4}, t_{PHL4} 1/	11	AD_0-AD_{15}	305	305			ns
t_{PLZ4}, t_{PHZ4}	8	AD_0-AD_{15}, $\overline{AS}$, $\overline{DS}$, B/$\overline{W}$, R/$\overline{W}$, N/$\overline{S}$, $\overline{MREQ}$, ST_0-ST_3, SN_0-SN_6	75	75	75	75	ns
t_{PLH5}, t_{PHL5} 1/	22	AD_0-AD_{15}	225	225			ns
t_{PLH6}, t_{PHL6} 1/	27	AD_0-AD_{15}	215	215			ns

See footnotes at end of device types 03 and 04.

TABLE IV. Output conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	E0 6/	F0 6/	G0 6/	H0 6/	Unit
t_{PLH7} 1/ t_{PHL7}	33	AD_0-AD_{15}	130	130			ns
t_{PLH8} 1/ t_{PHL8}	41	AD_0-AD_{15}	200	200			ns
t_{PLH9} 1/ t_{PHL9}	46	AD_0-AD_{15}	295	295			ns
t_{PLH10} t_{PHL10}	14	AD_0-AD_{15}	75	75	75	75	ns
t_{PLH11} 1/ t_{PHL11}	35	AD_0-AD_{15}	45	45			ns
t_{PLH12} t_{PHL12}	47	ST_0-ST_3	85	85	85	85	ns
t_{PLH13} t_{PHL13}	59	$\overline{MO}$	85	85	85	85	ns
t_{PLH14} 1/	16	$\overline{DS}$	195	195			ns
t_{PHL14} 1/	21	$\overline{DS}$	35	35			ns
t_{PHL15}	31	$\overline{DS}$	0	0	0	0	ns
t_{PHL16} 1/	32	$\overline{DS}$	35	35			ns
t_{PHL17} 1/	36	$\overline{DS}$	110	110			ns
t_{PHL18}	37	$\overline{DS}$	85	85	85	85	ns
t_{PHL19}	39	$\overline{DS}$	80	80	80	80	ns
t_{PLH20}	66	$\overline{BUSAK}$	75	75	75	75	ns
t_{PHL20}	42	$\overline{DS}$	100	100	100	100	ns
t_{PHL21} 1/	44	$\overline{DS}$	690	690			ns
t_{PHL22}	45	$\overline{DS}$	85	85	85	85	ns
t_{PHL23} 1/	17	$\overline{MREQ}$	35	35			ns
t_{PHL24}	18	$\overline{MREQ}$	70	70	70	70	ns
t_{PLH24}	23	$\overline{MREQ}$	60	60	60	60	ns

TABLE IV. Output conditions for device types 03 and 04 functional tests - Continued.

Symbol	Reference 2/	Terminal(s)	EO 6/	FO 6/	GO 6/	HO 6/	Unit
t_{PHL25}	24	$\overline{AS}$	60	60	60	60	ns
t_{PLH28}	34	$\overline{DS}$	65	65	65	65	ns
t_{PLH29} 1/	25	$\overline{AS}$	35	35			ns
t_{PLH30}	26	$\overline{AS}$	80	80	80	80	ns
t_{PHL26} 1/	28	$\overline{AS}$	35	35			ns
t_{PHL27}	67	$\overline{BUSAK}$	75	75	75	75	ns
t_{PLH31} 1/	48	$\overline{AS}$	30	30			ns

1/ Limits for output conditions G and H are calculated using footnote 5 of table I herein. (These parameters are dependent upon the clock high or clock low).

2/ The reference number refers to the position where the parameter being measured appears on figure 6.

3/ For device type 03 only.

4/ Clock input high or low or cycle times for device types 03 and 04 shall be 10 ns maximum

5/ Input conditions E and F are at f_{MAX}, input conditions G and H are at f_{MIN}.

6/ Output conditions EO and FO are at f_{MAX}, output conditions GO and HO are at f_{MIN}.

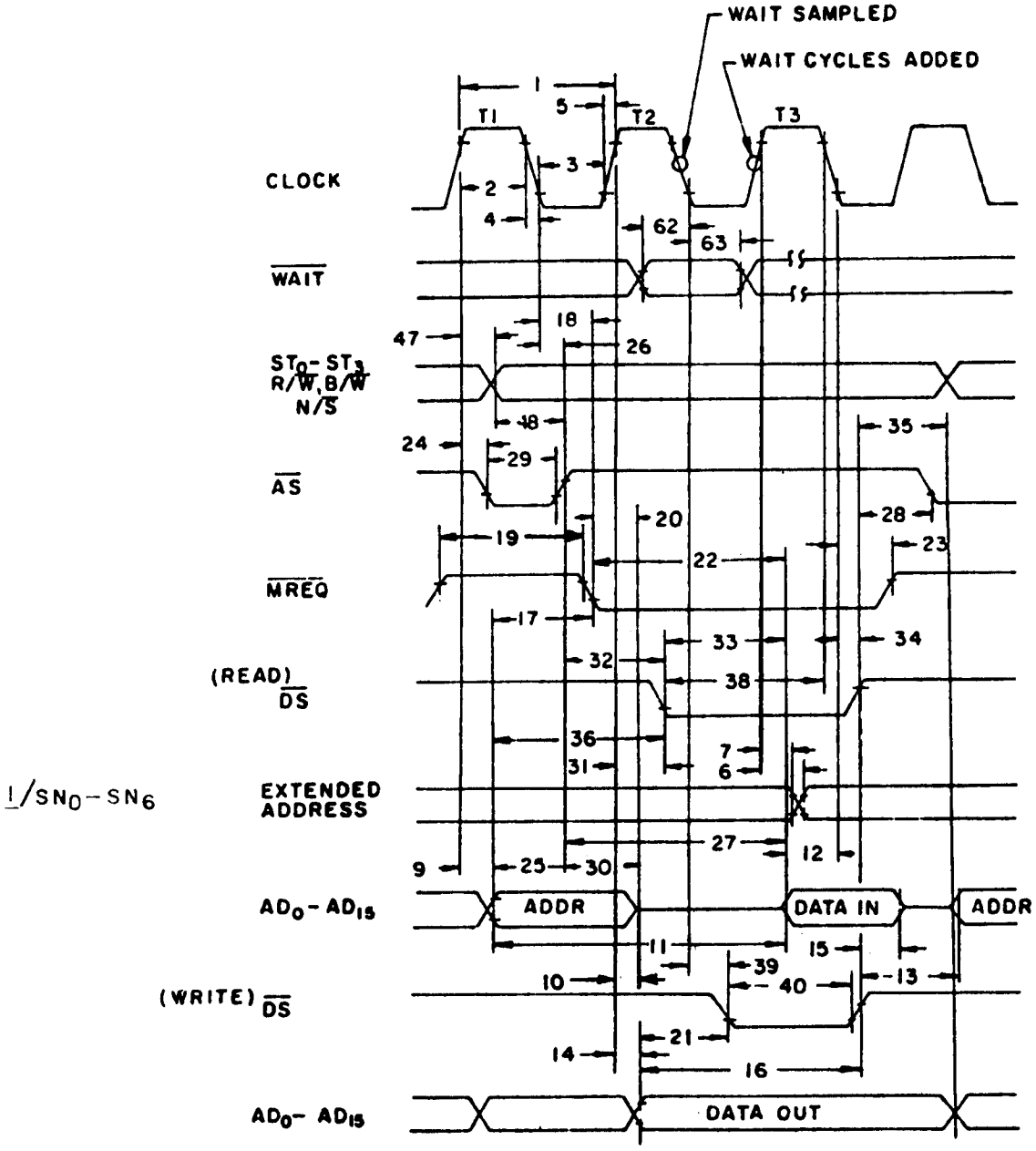


FIGURE 6. AC timing diagram (memory read/write timing).

1/ THESE SIGNALS APPLY TO DEVICE TYPES 01 AND 03 ONLY.

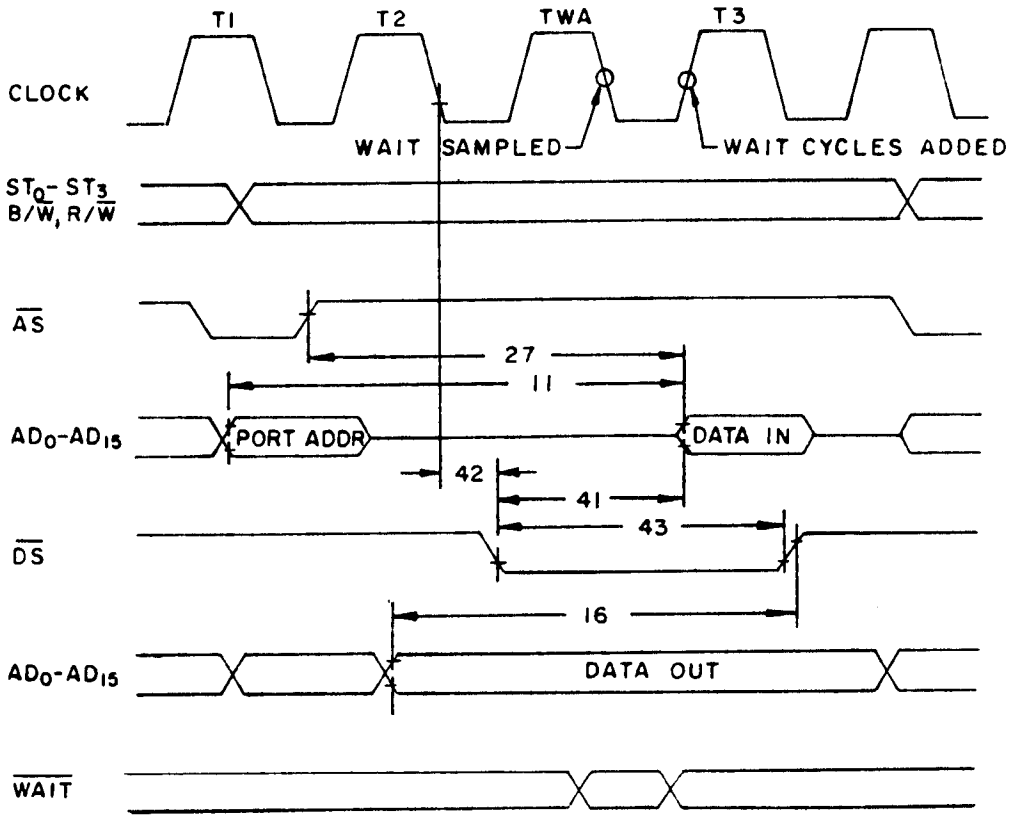


FIGURE 6. AC timing diagram (input/output timing) - Continued.

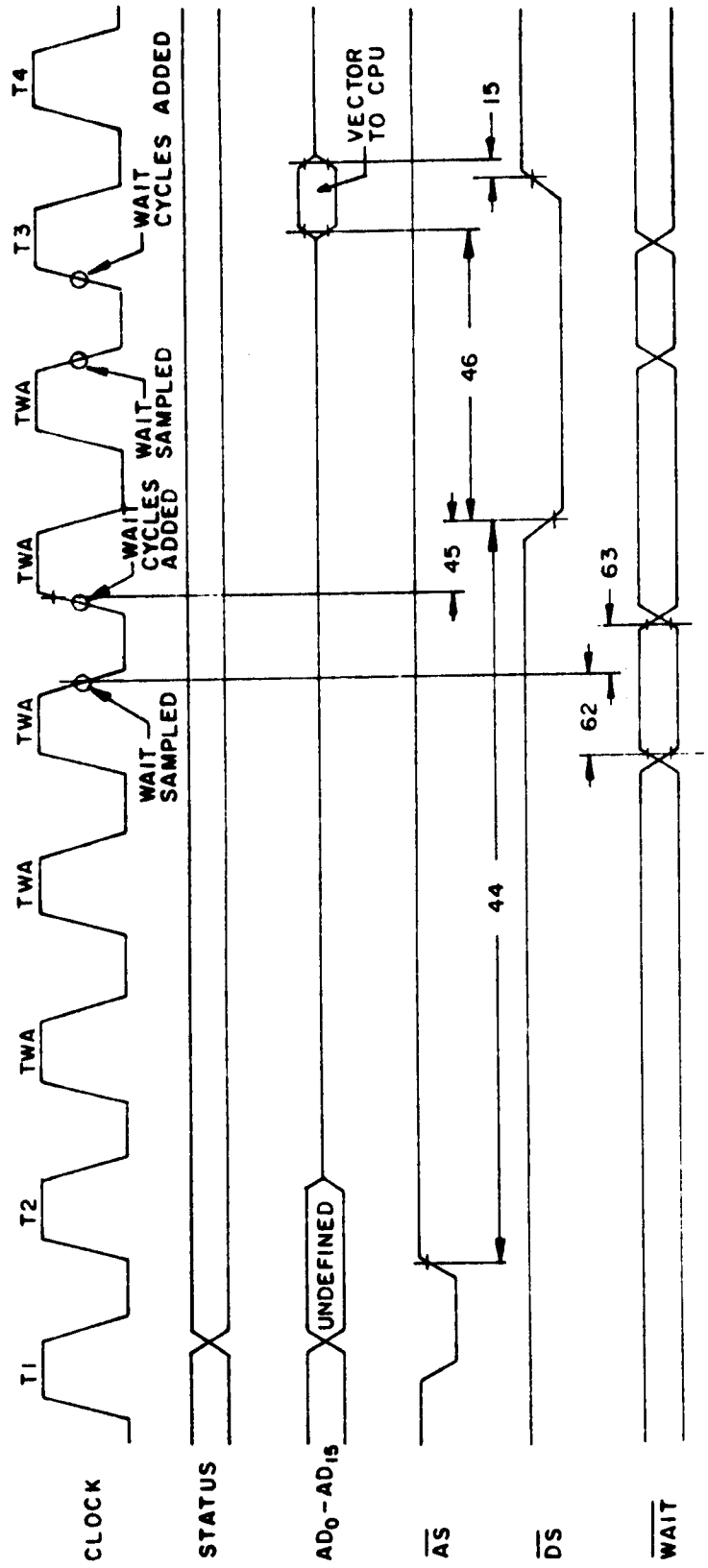
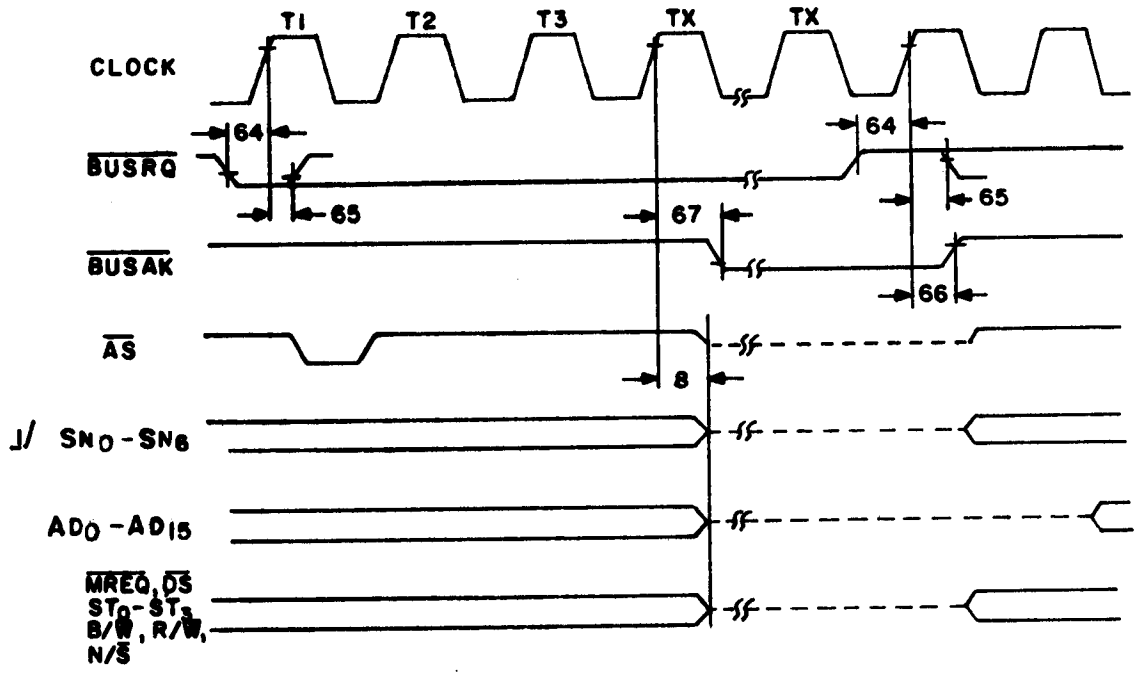
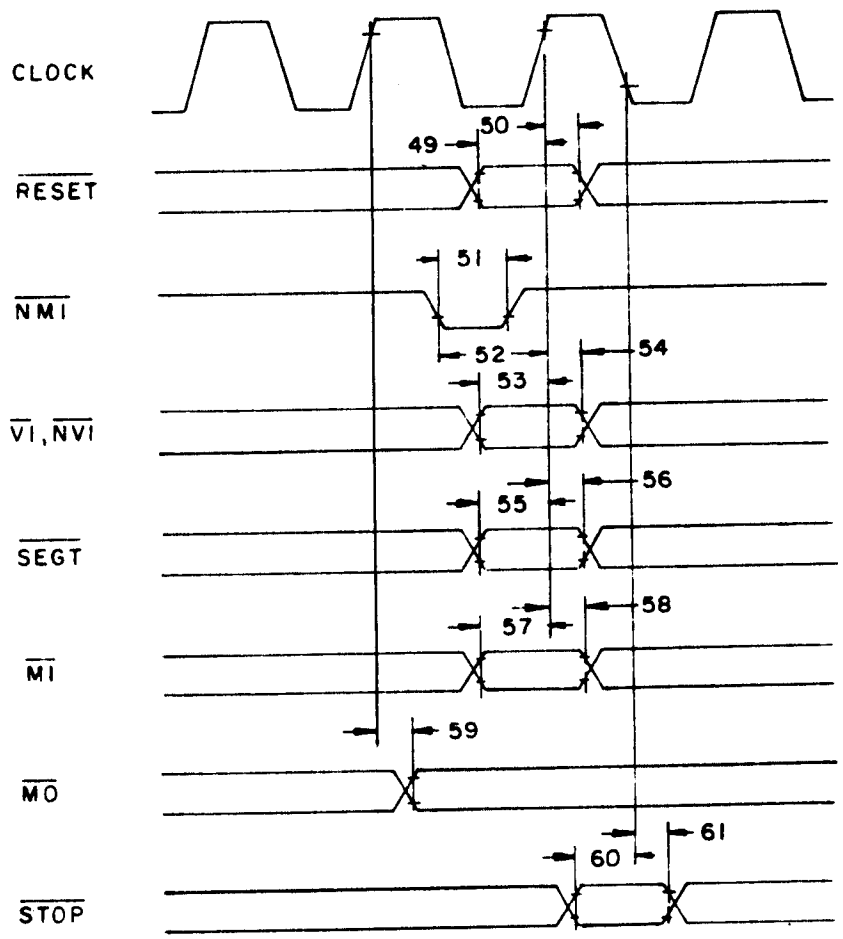


FIGURE 6. AC timing diagram (interrupt and segment trap acknowledge cycle) - Continued.



1/ THE SIGNALS APPLY TO DEVICE TYPES 01 AND 03 ONLY.

FIGURE 6. AC timing diagram (bus request acknowledge cycle) - Continued.



1/

1/ THIS SIGNAL APPLIES TO DEVICE TYPES 01 AND 03 ONLY.

FIGURE 6. AC timing diagram (miscellaneous signals) - Continued.

TABLE V. Test Vectors.

Table V, not printed herein, is a computer listing for use with table III. Each vector identifies activity states by pin number. See 6.2 for information on obtaining the complete table in a compatible output format.

NOTES:

1/ When the vectors are performed as specified in table III for subgroups 7, 8, 9, 10, and 11 they verify the dynamic, functional, threshold, and switching parameters at +25°C, -55°C, and +125°C.

TABLE VI. Microprocessor instructions for all device types.

LOAD AND EXCHANGE									
			Clock Cycles*						
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
CLR CLRB	dst	R	7	-	-				Clear dst ← 0
		IR	8	-	-				
		DA	11	12	14				
		X	11	12	15				
EX EXB	R, src	R	6	-	-				Exchange R ← src
		IR	12	-	-				
		DA	15	16	18				
		X	16	16	19				
LD LDB LDL	R, src	R	3	-	-	5	-	-	Load into Register R ← src
		IM	7	-	-	11	-	-	
		IM	5 (byte only)						
		IR	7	-	-	11	-	-	
		DA	9	10	12	12	13	15	
		X	10	10	13	13	13	16	
		BA	14	-	-	17	-	-	
		BX	14	-	-	17	-	-	
LD LDB LDL	dst, R	R	8	-	-	11	-	-	Load into Memory (Store) dst ← R
		DA	11	12	14	14	15	17	
		X	12	12	15	15	15	18	
		BA	14	-	-	17	-	-	
		BX	14	-	-	17	-	-	
LD LDB	dst, IM	IR	11	-	-				Load Immediate into Memory dst ← IM
		DA	14	15	17				
		X	15	15	18				
LDA	R, src	DA	12	13	15				Load Address R ← source address
		X	13	13	16				
		BA	15	-	-				
		BX	15	-	-				
LDAR	R, src	RA	15	-	-				Load Address Relative R ← source address
LDK	R, src	IM	5	-	-				Load Constant R ← n (n = 0 ... 15)

* NS = Non-segmented SS = Segmented short Output SL = Segmented Long Output

TABLE VI. Microprocessor instructions for all device types - Continued.

Mnemonics	Operands	Addr. Modes	Clock Cycles Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
LOAD AND EXCHANGE									
LDM	R, src, n	IR	11	-	-		+3n		Load Multiple
		DA	14	15	17				R ← src (n consecutive words)
		X	15	15	18				(n = 1 ... 16)
LDM	dst, R, n	IR	11	-	-		+3n		Load Multiple (Store Multiple)
		DA	14	15	17				dst ← R (n consecutive words)
		X	15	15	18				(n = 1 ... 16)
LDR	R, src	RA	14	-	-	17	-	-	Load Relative
LDRB									R ← src
LDRL									(range -32768 ... +32767)
LDR	dst, R	RA	14	-	-	17	-	-	Load Relative (Store Relative)
LDRB									dst ← R
LDRL									(range -32768 ... +32767)
POP	dst, IR	R	8	-	-	12	-	-	Pop
POPL		IR	12	-	-	19	-	-	dst ← IR
		DA	15	16	18	22	23	25	Autoincrement contents of R
		X	16	16	19	23	23	26	
PUSH	IR, src	R	9	-	-	12	-	-	Push
PUSHUL		IM	12	-	-	-	-	-	Autodecrement contents of R
		IR	13	-	-	20	-	-	IR ← src
		DA	13	14	16	20	21	23	
		X	14	14	17	21	21	24	
ARITHMETIC									
ADC	R, src	R	5	-	-				Add with Carry
ADCB									R ← R + src + carry
ADD	R, src	R	4	-	-	8	-	-	Add
ADDB		IM	7	-	-	14	-	-	R ← R + src
ADDL		IR	7	-	-	14	-	-	
		DA	9	10	12	15	16	18	
		X	10	10	13	16	16	19	
CP	R, src	R	4	-	-	8	-	-	Compare with Register
CPB		IM	7	-	-	14	-	-	R - src
CPL		IR	7	-	-	14	-	-	
		DA	9	10	12	15	16	18	
		X	10	10	13	16	16	19	

TABLE VI. Mircroprocessor instructions for all device types - Continued.

ARITHMETIC

Mnemonics	Operands	Addr. Modes	Clock Cycles Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
CP CPB	dst, IM	IR DA X	11 14 15	- 15 15	- 17 18				Compare with Immediate dst - IM
DAB	dst	R	5	-	-				Decimal Adjust
DEC DECB	dst, n	R IR DA X	4 11 13 14	- - 14 14	- - 16 17				Decrement by n dst ← dst - n (n = 1 ... 16)
DIV DIVL	R, src	R IM IR DA X	95 95 95 96 97	- - - 97 97	- - - 99 100	723 723 723 724 725	- - - 725 725	- - - 727 728	Divide (signed) Word: R_{n+1} ← $R_{n, n+1}$ ÷ src R_n ← remainder Long Word: $R_{n+2, n+3}$ ← $R_{n \ldots n+3}$ ÷ src $R_{n\ n+1}$ ← remainder
EXTS EXTSB EXTSL	dst	R	11	-	-	11	-	-	Extend Sign Extend sign of low order half of dst through high order half of dst
INC INCB	dst, n	R IR DA X	4 11 13 14	- - 14 14	- - 16 17				Increment by n dst ← dst + n (n = 1 ... 16)
MULT MULTL	R, src	R IM IR DA X	70 70 70 71 72	- - - 72 72	- - - 74 75	282* 282* 282* 283* 284*	- - - 284* 284*	- - - 286* 287*	Multiply (signed) Word: $R_{n, n+1}$ ← R_{n+1} · src Long Word: $R_{n \ldots n+3}$ ← $R_{n+2, n+3}$ · src *Plus seven cycles for each 1 in the multiplicand
NEG NEGB	dst	R IR DA X	7 12 15 16	- - 16 16	- - 18 19				Negate dst ← 0 - dst
SBC SBCB	R, src	R	5	-	-				Subtract with Carry R ← R - src - carry
SUB SUBB SUBL	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13	8 14 14 15 16	- - - 16 16	- - - 18 19	Subtract R ← R - src

TABLE VI. Microprocessor instructions for all device types - Continued.

LOGICAL									
			Clock Cycles						
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
AND ANDB	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13				AND R ← R AND src
COM COMB	dst	R IR DA X	7 12 15 16	- - 16 16	- - 18 19				Complement dst ← NOT dst
OR ORB	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13				OR R ← R OR src
TEST TESTB TESTL	dst	R IR DA X	7 8 11 12	- - 12 12	- - 14 15	13 13 16 17	- - 17 17	- - 19 20	Test dst OR 0
TCC TCCB	cc, dst	R	5	-	-				Test Condition Code Set LSB if cc is true
XOR XORB	R, src	R IM IR DA X	4 7 7 9 10	- - - 10 10	- - - 12 13				Exclusive OR R ← R XOR src

TABLE VI. Microprocessor instructions for all device types - Continued.

Mnemonics	Operands	Addr. Modes	Clock Cycles Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
PROGRAMS CONTROL									
CALL	dst	IR	10	-	15				Call Subroutine Autodecrement SP @ SP ← PC PC ← dst
		DA	12	18	20				
		X	13	18	21				
CALR	dst	RA	10	-	15				Call Relative Autodecrement SP @ SP ← PC PC ← PC + dst (range -4094 to +4096)
DJNZ DBJNZ	R, dst	RA	11	-	-				Decrement and Jump if Non-Zero R ← R - 1 If R ≠ 0: PC ← PC + dst (range -254 to 0)
IRET*	-	-	13	-	16				Interrupt Return PS ← @ SP Autoincrement SP
JP	cc, dst	IR	10	-	15	(taken)			Jump Conditional If cc is true: PC ← dst
		IR	7	-	7	(not taken)			
		DA	7	8	10				
		X	8	8	11				
JR	cc, dst	RA	6	-	-				Jump Conditional Relative If cc is true: PC ← PC + dst (range -256 to +254)
RET	cc	-	10	-	13	(taken)			Return Conditional If cc is true: PC ← @ SP Autoincrement SP
			7	-	7	(not taken)			
SC	src	IM	33	-	39				System Call Autodecrement SP @ SP ← old PS Push instruction PS ← System Call PS
BIT MANIPULATION									
BIT BITB	dst, b	R	4	-	-				Test Bit Static Z flag ← NOT dst bit specified by b
		IR	8	-	-				
		DA	10	11	13				
		X	11	11	14				
BIT BITB	dst, R	R	10	-	-				Test Bit Dynamic Z flag ← NOT dst bit specified by contents of R

* Privileged instruction. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

BIT MANIPULATION									
			Clock Cycles						
Mnemonics	Operands	Addr. Modes	Word, Byte NS	Word, Byte SS	Word, Byte SL	Long Word NS	Long Word SS	Long Word SL	Operation
RES RESB	dst, b	R IR DA X	4 11 13 14	- - 14 14	- - 16 17				Reset Bit Static Reset dst bit specified by b
RES RESB	dst, R	R	10	-	-				Reset Bit Dynamic Reset dst bit specified by contents R
SET SETB	dst, b	R IR DA X	4 11 13 14	- - 14 14	- - 16 17				Set Bit Static Set dst bit specified by b
SET SETB	dst, R	R	10	-	-				Set Bit Dynamic Set dst bit specified by contents of R
TSET TSETB	dst	R IR DA X	7 11 14 15	- - 15 15	- - 17 18				Test and Set S flag ← MSB of dst dst ← all 1s
ROTATE AND SHIFT									
RLDB	R, src	R	9	-	-				Rotate Digit Left
RRDB	R, src	R	9	-	-				Rotate Digit Right
RL RLB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Left by n bits (n = 1, 2)
RLC RLCB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Left through Carry by n bits (n = 1, 2)
RR RRB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Right by n bits (n = 1, 2)
RRC RRCB	dst, n	R R	6 for n = 1 7 for n = 2						Rotate Right through Carry by n bits (n = 1, 2)
SDA SDAB SDAL	dst, R	R	(15 + 3 n)			(15 + 3 n)			Shift Dynamic Arithmetic Shift dst left or right by contents of R

TABLE VI. Microprocessor instructions for all device types - Continued.

ROTATE AND SHIFT										
			Clock Cycles							
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
SDL SDLB SDLL	dst, R	R	(15 + 3 n)			(15 + 3 n)			Shift Dynamic Logical Shift dst left or right by contents of R
SLA SLAB SLAL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Left Arithmetic by n bits
SLL SLLB SLLL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Left Logical by n bits
SRA SRAB SRAL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Right Arithmetic by n bits
SRL SRLB SRLL	dst, n	R	(13 + 3 n)			(13 + 3 n)			Shift Right Logical by n bits
BLOCK TRANSFER AND STRING MANIPULATION									
CPD CPDB	R_X, src, R_Y, cc	IR	20	-	-				Compare and Decrement R_X - src Autodecrement src address $R_Y \leftarrow R_Y - 1$
CPDR CPDRB	R_X, src, R_Y, cc	IR	(11 + 9 n)						Compare, Decrement and Repeat R_X - src Autodecrement src address $R_Y \leftarrow R_Y - 1$ Repeat until cc is true or $R_Y = 0$
CPI CPIB	R_X, src, R_Y, cc	IR	20	-	-				Compare and Increment R_X - src Autoincrement src address $R_Y \leftarrow R_Y - 1$
CPIR CPIRB	R_X, src, R_Y, cc	IR	(11 + 9 n)						Compare, Increment and Repeat R_X - src Autoincrement src address $R_Y \leftarrow R_Y - 1$ Repeat until cc is true or $R_Y = 0$

TABLE VI. Microprocessor instructions for all device types - Continued.

BLOCK TRANSFER AND STRING MANIPULATION									
			Clock Cycles						
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
CPSD CPSDB	dst, src, R, cc	IR	25	-	-				Compare String and Decrement dst - src Autodecrement dst and src addresses R ← R - 1
CPSDR CPSDRB	dst, src,	IR	(11 + 14 n)						Compare String, Decrement and Repeat dst - src Autodecrement dst and src addresses R ← R - 1 Repeat until cc is true or R = 0
CPSI CPSIB	dst, src, R, cc	IR	25	-	-				Compare String and Increment dst - src Autoincrement dst and src addresses R ← R - 1
CPSIR CPSIRB	dst, src, R, cc	IR	(11 + 14 n)						Compare String, Increment and Repeat dst - src Autoincrement dst and src addresses R ← R - 1 Repeat until cc is true or R = 0
LDD LDDB	dst, src, R	IR	20	-	-				Load and Decrement dst ← src Autodecrement dst and src addresses R ← R - 1
LDDR LDDRB	dst, src, R	IR	(11 + 9 n)						Load, Decrement and Repeat dst ← src Autodecrement dst and src addresses R ← R - 1 Repeat until R = 0
LDI LDIB	dst, src, R	IR	20	-	-				Load and Increment dst ← src Autoincrement dst and src addresses R ← R - 1
LDIR LDIRB	dst, src, R	IR	(11 + 9 n)						Load, Increment and Repeat dst ← src Autoincrement dst and src addresses R ← R - 1 Repeat until R = 0

TABLE VI. Microprocessor instructions for all device types - Continued.

BLOCK TRANSFER AND STRING MANIPULATION										
			Clock Cycles							
Mnemonics	Operands	Addr. Modes	Word, Byte NS	Word, Byte SS	Word, Byte SL	Long Word NS	Long Word SS	Long Word SL	Operation
TRDB	dst, src, R	IR	25	-	-				Translate and Decrement dst ← src (dst) Autodecrement dst address R ← R - 1
TRDRB	dst, src, R	IR	(11 + 14 n)						Translate, Decrement and Repeat dst ← src (dst) Autodecrement dst address R ← R - 1 Repeat until R = 0
TRIB	dst, src, R	IR	25	-	-				Translate and Increment dst ← src (dst) Autoincrement dst address R ← R - 1
TRIRB	dst, src, R	IR	(11 + 14 n)						Translate, Increment and Repeat dst src (dst) Autoincrement dst address R ← R - 1 Repeat until R = 0
TRTDB	src1, src2, R	IR	25	-	-				Translate and Test. Decrement RH1 ← src2 (src1) Autodecrement src1 address R ← R - 1
TRTDRB	src1, src2, R	IR	(11 + 14 n)						Translate and Test. Decrement and Repeat RH1 ← src2 (src1) Autodecrement src1 address R ← R - 1 Repeat until R = 0 or RH1 = 0
TRTIB	src1, src2,	IR	25						Translate and Test. Increment RH1 ← src2 (src1) Autoincrement src laddress R ← R - 1
TRTIRB	src1, src2, R	IR	(11 + 14 n)						Translate and Test. Increment and Repeat RH1 ← src2 (src1) Autoincrement src1 address R ← R - 1 Repeat until R = 0 or RH1 = 0

TABLE VI. Microprocessor instructions for all device types - Continued.

INPUT/OUTPUT										
			Clock Cycles							
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
IN* INB*	R, src	IR DA	10 12	- -	- -				Input R ← src
IND* INDB*	dst, src, R	IR	21	-	-				Input and Decrement dst ← src Autodecrement dst address R ← R - 1
INDR* INDRB*	dst, src R	IR	(11 + 10 n)						Input, Decrement and Repeat dst ← src Autodecrement dst address R ← R - 1 Repeat until R = 0
INI* INIB*	dst, src R	IR	21	-	-				Input and Increment dst ← src Autoincrement dst address R ← R - 1
INIR* INIRB*	dst, src, R	IR	(11 + 10 n)						Input, Increment and Repeat dst ← src Autoincrement dst address R ← R - 1 Repeat until R = 0
OUT* OUTB*	dst, R	IR DA	10 12	- -	- -				Output dst ← R
OUTD* OUTDB*	dst, src, R	IR	21	-	-				Output and Decrement dst ← src Autodecrement src address R ← R - 1
OTDR* OTDRB*	dst, src, R	IR	(11 + 10 n)						Output, Decrement, and Repeat dst ← src Autodecrement src address R ← R - 1 Repeat until R = 0
OUTI* OUTIB*	dst, src, R	IR	21	-	-				Output and Increment dst ← src Autoincrement src address R ← R - 1
OTIR* OTIRB*	dst, src, R	IR	(11 + 10 n)						Output, Increment and Repeat dst ← src Autoincrement src address R ← R - 1 Repeat until R = 0

*Privileged instructions. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

INPUT/OUTPUT										
			Clock Cycles							
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
SIN* SINB*	R, src	DA	12	-	-				Special Input R ← src
SIND* SINDB*	dst, src, R	IR	21	-	-				Special Input and Decrement dst ← src Autodecrement dst address R ← R - 1
SINDR* SINDRB*	dst, src, R	IR	(11 + 10 n)						Special Input, Decrement Repeat dst ← src Autodecrement dst address R ← R - 1 Repeat until R = 0
SINI* SINIB*	dst, src, R	IR	21	-	-				Special Input and Increment dst ← src Autoincrement dst address R ← R - 1
SINIR* SINIRB*	dst, src, R	IR	(11 + 10 n)						Special Input, Increment and Repeat dst src Autoincrement dst address R ← R - 1 Repeat until R = 0
SOUT* SOUTB*	dst, src	DA	12	-	-				Special Output dst ← src
SOUTD* SOUTDB*	dst, src R	IR	21	-	-				Special Output and and Decrement dst ← src Autodecrement src address R ← R - 1 Repeat until R = 1
SOTDR* SOTDRB*	dst, src, R	IR	(11 + 10 n)						Special Output, Decrement and Repeat dst ← src Autodecrement src address R ← R - 1 Repeat until R = 0
SOUTI* SOUTIB*	dst, src, R	IR	21	-	-				Special Output and Incre- ment dst ← src Autoincrement src address R ← R - 1
SOTIR* SOTIRB*	dst, src, R	R	(11 + 10 n)						Special Output, Increment and Repeat dst src Autoincrement src address R ← R - 1 Repeat until R = 0

*Privileged instructions. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

CPU CONTROL									
			Clock Cycles						
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
COMFLG	flags	-	7	-	-				Complement Flag (Any combination of C, Z, S, P/V)
DI*	int	-	6	-	-				Disable Interrupt (Any combination of NVI, VI)
EI*	int	-	6	-	-				Enable Interrupt (Any combination of NVI, VI)
HALT*	-	-	(8 +3 n)						HALT
LDCTL*	CTLR, src	R	7	-	-				Load into Control Register CTLR ← src
LDCTL*	dst, CTLR	R	7	-	-				Load into Control Register dst ← CTLR
LDCTLB	FLGR, src	R	7	-	-				Load into Flag Byte Register FLGR ← src
LDCTLB	dst, FLGR	R	7	-	-				Load from Flag Byte Register dst ← FLGR
LDPS*	src	IR	12	-	16				Load Program Status PS ← src
		DA	16	20	22				
		X	17	20	23				
MBIT*	-	-	-	7	-				Test Multi-Micro Bit Set S if $\overline{M_1}$ is Low; reset S if $\overline{M_1}$ is High.
MREQ*	dst	R	(12 + 7 n)						Multi-Micro Request
MRES*	-	-	5	-	-				Multi-Micro Reset
MSET*	-	-	5	-	-				Multi-Micro Set
NOP	-	-	7	-	-				No Operation

TABLE VI. Microprocessor instructions for all device types - Continued.

CPU CONTROL									
			Clock Cycles						
Mnemonics	Operands	Addr. Modes	Word, Byte NS	SS	SL	Long Word NS	SS	SL	Operation
RESFLG	flag	-	7	-	-				Reset Flag (Any combination of C, Z, S, P/V)
SETFLG	flag	-	7	-	-				Set Flag (Any combination of C, Z, S, P/V)

*Privileged instruction. Executed in system mode only.

TABLE VI. Microprocessor instructions for all device types - Continued.

CONDITION CODES

Code	Meaning	Flag settings	CC Field
	Always false	-	0000
	Always true	-	1000
Z	Zero	Z = 1	0110
NZ	Not zero	Z = 0	1110
C	Carry	C = 1	0111
NC	No Carry	C = 0	1111
PL	Plus	S = 0	1101
MI	Minus	S = 1	0101
NE	Not equal	Z = 0	1110
EQ	Equal	Z = 1	0110
OV	Overflow	P/V = 1	0100
NOV	No overflow	P/V = 0	1100
PE	Parity is even	P/V = 1	0100
PO	Parity is odd	P/V = 0	1100
GE	Greater than or equal (signed)	(S XOR P/V) = 0	1001
LT	Less than (signed)	(S XOR P/V) = 1	0001
GT	Greater than (signed)	(Z OR (S XOR P/V) = 0	1010
LE	Less than or equal (signed)	(Z OR (S XOR P/V) = 1	0010
UGE	Unsigned greater than or equal	C = 0	1111
ULT	Unsigned less than	C = 1	0111
UGT	Unsigned greater than	(C = 0) AND (Z = 0) = 1	1011
ULE	Unsigned less than or equal	(C OR Z) = 1	0011

Note that some condition codes have identical flag settings and binary fields in the instruction: Z = EQ, NZ = NE, C = ULT, NC = UGE, OV = PE, NOV = PO

STATUS LINE CODES

ST_3 - ST_0	Definition
0000	Internal operation
0001	Memory refresh
0010	I/O reference
0011	Special I/O reference (e.g., to an MMU)
0100	Segment trap acknowledge
0101	Non-maskable interrupt acknowledge
0110	Non-vectored interrupt acknowledge
0111	Vectored interrupt acknowledge
1000	Data memory request
1001	Stack memory request
1010	Data memory request (EPU)
1011	Stack memory request (EPU)
1100	Program reference, nth word
1101	Instruction fetch, first word
1110	EPU transfer
1111	Reserved

b. Steady state life test (method 1005 of MIL-STD-883).

(1) Test condition D or E using the circuit shown on figure 4.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.

4.5 Methods of inspection. Methods of inspection shall be as follows:

4.5.1 Voltage and current. All voltage values given are referenced to the microcircuit ground terminal. Current values given are conventional and are positive when flowing into the referenced terminal.

4.5.2 High-voltage (V_{ZAP}) test of input protection circuits. The following terminals, NMI, MREQ, AD_{13} and BUSAK of the device under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V. This destructive test shall be conducted as follows using the test circuit shown on figure 7.

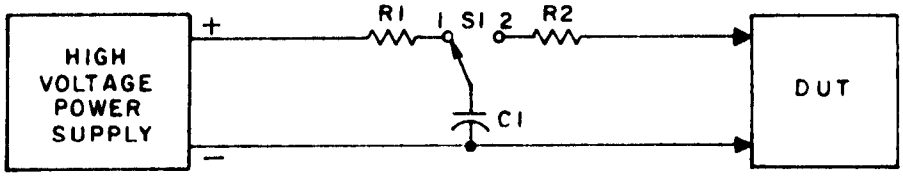
a. Measure I_{IH} and I_{IL} at the inputs selected as stated above at 25°C. These measurements shall be made in accordance with table III herein. The test limits for each single terminal measurement of I_{IH} and I_{IL} shall be as specified in table III.

b. Apply the test voltage (V_{ZAP} = 400 V) to the same terminals selected for leakage current measurements. Apply V_{ZAP} in a 2 mode sequence as shown below and by charging C_1 to V_{ZAP} with S_1 in position 1 and then switching to position 2.

(1) Terminal (-) to GND.

(2) Terminal (+) to GND.

c. Within 24 hours repeat the I_{IH} and I_{IL} measurements on the same terminals as performed above. After the V_{ZAP} test a DUT exhibiting leakage currents in excess of the specified limits is defective.



V_{ZAP} = 400 V minimum charge on C1.
1 MΩ ≤ R1 ≤ 5 MΩ.
R2 = 1.5 kilohms ±5%.
C1 = 100 pF ±10%.
S1 = Hg-wetted "bounceless" relay.
All pins are at ground except the DUT pin being tested.

FIGURE 7. High voltage (V_{ZAP}) test circuit.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Test vector table. Table V (test vectors), which forms a part of this specification, is not printed herein because of its extreme length and complexity; and, even when presented as hard copy, it requires conversion to on-line format. When the entire sequence of vector groups is needed for driving devices as part of an inspection, a test program output should be obtained in a form compatible with test system architecture. The preparing activity, or Defense Electronics Supply Center as its agent, may be consulted for information on obtaining such output. For reference purposes, Rome Air Development Center (RADC-RBRM) and Defense Electronics Supply Center (DESC-ECS) each maintain a limited quantity of dated, hard copy printouts of this table.

6.3 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.4 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to qualifying activity, if applicable.

e. Requirements for failure analysis, (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These special requirements shall not affect the part number.

h. Requirements for "JAN" marking.

6.5 Terms and definitions. The abbreviations, terms, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

AD_0-AD_{15} (Address/Data bus)	Inputs/outputs, active high, 3-state. These multiplexed address and data lines are used both for I/O and to address memory. AD_{15} = MSB.
$\overline{AS}$ (Address strobe)	Output, active low, 3-state. The rising edge of $\overline{AS}$ indicates addresses are valid.
$\overline{BUSAK}$ (Bus Acknowledge)	Output, active low. A low on this line indicates the CPU has relinquished control of the bus. This occurs after completion of the current machine cycle. $\overline{BUSAK}$ goes inactive one clock cycle after the synchronization of $\overline{BUSRQ}$ being released.

$\overline{BUSRQ}$ (Bus request)	Input, active low. This line must be driven low to request the bus from the CPU. It is sampled for being active at the beginning of each machine cycle. when it is released, it is synchronized with the next rising clock edge.
$\overline{DS}$ (Data strobe)	Output, active low, 3-state. This line times the data in and out of the CPU.
$\overline{MREQ}$ (Memory request)	Output, active low, 3-state. A low on this line indicates that the address/data bus hold a memory address.
$\overline{MI}$, $\overline{MO}$ (Multi-Micro In, Multi-Micro Out)	Input and output, active low. These two lines form a resource-request daisy chain that allows one CPU in a multi-microprocessor system to access a shared resource. $\overline{MI}$ is sampled on the rising edge of T3 of the last machine cycle of any instruction and internally latched.
$\overline{NMI}$ (Non-Maskable Interrupt)	Edge triggered, input, active low. A high-to-low transition on $\overline{NMI}$ requests, a non-maskable interrupt. The NMI interrupt has the highest priority of the three types of interrupts. The internal $\overline{NMI}$ latch is sampled on the rising edge of T3 of the last machine cycle of any instruction.
$\overline{NVI}$ (Non-Vectored Interrupt)	Input, active low. A low on this line requests a non-vectored interrupt. It is sampled on the rising edge of T3 of the last machine cycle of any instruction.
CLK (System Clock)	Input. CLK is a 5 V single-phase time-base input.
$\overline{RESET}$ (Reset)	Input, active low. A low on this line resets the CPU. $\overline{RESET}$ must be active for at least five clock cycles.
R/$\overline{W}$ (Read/Write)	Output, low = write, 3-state. R/$\overline{W}$ indicates that the CPU is reading from, or writing to memory or I/O.
ST_0-ST_3 (Status)	Outputs, active high, 3-state. These lines specify the CPU status.
$\overline{STOP}$ (Stop)	Input, active low. This input can be used to single-step instruction execution. It is sampled on the last falling clock edge preceding any first instruction fetch cycle.
$\overline{VI}$ (Vectored Interrupt)	Input, active low. A low on this line requests a vectored interrupt. It is sampled on the rising edge of T3 of the last machine cycle of any instruction.
$\overline{WAIT}$ (Wait)	Input, active low. This line indicates to the CPU that the memory or I/O device is not ready for data transfer. It is sampled on the falling edge of T2 and any subsequent $\overline{WAIT}$ states.
B/$\overline{W}$ (Byte/Word)	Output, low = word, 3-state. This signal defines the type of memory reference on the 16-bit address/data bus.
N/$\overline{S}$ (Normal/System Mode)	Output, low = system mode, 3-state. N/$\overline{S}$ indicates the CPU is in the normal or system mode.

SN_0-SN_6 (Segment Number)	Outputs, active high, 3-state. These lines provide the 7-bit segment number used to address one of 128 segments by the memory management unit. Output by device types 01 and 03 only. SN_6 = MSB.
$\overline{SEGT}$ (Segment Trap)	Input, active low. The memory management unit interrupts the CPU with a low on this line when the MMU detects a segmentation trap. Input on the 01 and 03 device types only. It is sampled on the rising edge of T3 of the last machine cycle of any instruction.

6.6 Logistic support. Lead material and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead finish "C" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.7 Handling. MOS integrated circuits should be handled with certain precautions to avoid damage due to the accumulation of static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage; however, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive carriers.

e. Avoid uses of plastic, rubber, or silk in MOS areas.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types, and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military-device type	Generic-industry type
01	Z8001 CPU
02	Z8002 CPU
03	Z8001A CPU
04	Z8002A CPU

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - SH, OS
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Agent:
DLA - ES

Preparing activity:
Air Force - 17

(Project 5962-0563)