QUALIFICATION
REQUIREMENTS
REMOVED

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS

MONOLITHIC 8-BIT MICROPROCESSOR (FIXED INSTRUCTION)

INACTIVE FOR NEW DESIGN AFTER DATE OF THIS REVISION.

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic CMOS silicon gate microprocessor. One product assurance class and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The complete part number shall be as specified in MIL-M-38510, with the exception that the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device types shall be as follows:

Device type	Circuit
01	8-bit fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline, (see MIL-M-38510, appendix C)
Q	D-5 (40-lead, 9/16" x 2 1/16"), dual-in-line package

1.3 Absolute maximum ratings:

Storage-temperature range (T_{stg}) - - - -	-65°C to +150°C
Operating temperature range (T_A) - - - -	-55°C to +125°C
DC supply-voltage range (V_{CC} - V_{DD}) (all voltage values referenced to V_{SS} terminal) $V_{CC} \leq V_{DD}$ - - - - - - - - - -	-0.5 V dc to +13 V dc
Power dissipation per packge (P_D):	
T_A = -55°C to +100°C - - - - - - - - - -	500 mW
T_A = +100°C to +125°C - - - - - - - - -	Derate linearly at 12 mW/°C to 200 mW
Device dissipation per output transistor:	
T_A = -55°C to +125°C - - - - - - - - - -	100 mW
Input voltage range, all inputs - - - -	-0.5 V dc to V_{DD} +0.5 V dc
DC input current, any one input - - - -	±10 mA
Lead temperature (during soldering):	
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 seconds maximum - - - - - - - - - -	265°C
Maximum junction temperature (T_J) - - -	150°C
Thermal resistance, junction to case (θ_{JC}) - - - - - - - - - - - - - - - - - - -	30°C/W

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: National Aeronautics and Space Administration, George C. Marshall Space Flight Center, ATTN: EG02, Huntsville, AL 35812, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end at the end of this document or by letter.

1.4 Recommended operating conditions. (At T_A = -55°C to +125°C.)

Supply voltage range (V_{DD})- - - - - - - - -	4.5 V dc to 11 V dc
Supply voltage range (V_{CC})- - - - - - - - -	4.5 V dc to V_{DD}
Input voltage range - - - - - - - - - - - - -	V_{SS} to V_{CC}

1.5 Recommended timing conditions- (At T_A = -55°C to +125°C.)

Maximum clock input rise or fall time (t_r or t_f, at V_{CC} - 4.5 V dc to 11 V dc and V_{DD} = 4.5 V dc to 11 V dc)-	0.6 µs
Instruction time 1/	
At V_{CC} = V_{DD} = 5 V dc - - - - - - - - -	10.7 µs
At V_{CC} = V_{DD} = 10 V dc- - - - - - - - -	4.2 µs
Maximum DMA transfer rate:	
At V_{CC} = V_{DD} = 5 V dc - - - - - - - - -	190 Kbytes/sec
At V_{CC} = V_{DD} = 10 V dc- - - - - - - - -	480 Kbytes/sec
Clock input frequency (f_{CL}) 2/:	
At V_{CC} = V_{DD} = 5 V dc - - - - - - - - -	DC to 1.5 MHz
At V_{CC} = V_{DD} = 10 V dc- - - - - - - - -	DC to 3.8 MHz

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2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

1/ Equals 2 machine cycles at maximum clock frequency for all instructions except long branch and long skip.
2/ Load capacitance (C_L) = 50 pF.

3.2.1 Terminal connections. Terminal connections shall be as specified on figure 1.

3.2.2 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.3 Functional description, terms, and symbols. Functional description, terms, and symbols shall be as specified in 6.5.

3.2.4 Case outline. The case outline shall be as specified in MIL-M-38510 and in 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510 (see 6.6).

3.4 Electrical performance characteristics. The electrical performance characteristics shall be as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Microprocessor instruction set. The microprocessor instruction set shall be as specified in table VI.

3.7 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.8 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line. Not necessarily the line producing the device type described herein.

3.9 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007 of MIL-STD-883, as applicable, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following modifications and additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) The burn-in test as described in 3.1.10 of method 5004 shall be performed as indicated. (3.1.11 and 3.1.12 are not required; 3.1.9 is optional for class B devices.)

(2) For class B devices, dynamic burn-in using the circuit shown on figure 3 or equivalent shall be performed for 160 hours minimum at 125°C.

b. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroups 1 and 7 (after cooldown) of final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroups 1 and 7, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_A \leq +125°C$	Figure	Limits Min	Limits Max	Unit
Quiescent device current	I_{SS}	$V_{CC} = V_{DD} = 5$ V	7(a)	0	-500	μA
		$V_{CC} = V_{DD} = 10$ V	7(a)	0	-1,000	μA
		$V_{CC} = V_{DD} = 13$ V	7(a)	0	-1,500	μA
Output low drive current	I_{OL}	$V_{CC} = V_{DD} = 5$ V; $V_O = 0.4$ V		0.95	---	mA
		$V_{CC} = V_{DD} = 10$ V; $V_O = 0.5$ V		1.70	---	mA
$\overline{XTAL}$ output low current	I_{OLX}	$V_{CC} = V_{DD} = 5$ V; $V_O = 0.4$ V		66	---	μA
Output high drive current	I_{OH}	$V_{CC} = V_{DD} = 5$ V; $V_O = 4.6$ V		-0.23	---	mA
		$V_{CC} = V_{DD} = 10$ V; $V_O = 9.5$ V		-0.54	---	mA
$\overline{XTAL}$ output high current	I_{OHX}	$V_{CC} = V_{DD} = 5$ V; $V_O = 4.6$ V		-33	---	μA
Low-level output voltage	V_{OL}	$V_{CC} = V_{DD} = 5$ V; $I_{OL} = 0$ mA		---	0.2	V
		$V_{CC} = V_{DD} = 10$ V; $I_{OL} = 0$ mA		---	0.2	V
High-level output voltage	V_{OH}	$V_{CC} = V_{DD} = 5$ V; $I_{OH} = 0$ mA		4.8	---	V
		$V_{CC} = V_{DD} = 10$ V; $I_{OH} = 0$ mA		9.8	---	V
Input low threshold voltage	V_{IL}	$V_{CC} = V_{DD} = 5$ V; $V_{OL} = 0.5$ V; $V_{OH} = 4.5$ V		---	1.2	V
		$V_{CC} = V_{DD} = 10$ V; $V_{OL} = 1.0$ V; $V_{OH} = 9.0$ V		---	3.0	V
Input high threshold voltage	V_{IH}	$V_{CC} = V_{DD} = 5$ V; $V_{OL} = 0.5$ V; $V_{OH} = 4.5$ V		3.5	---	V
		$V_{CC} = V_{DD} = 10$ V; $V_{OL} = 1.0$ V; $V_{OH} = 9.0$ V		7.0	---	V
Input high leakage current	I_{IH}	$V_{CC} = V_{DD} = 13$ V; $V_{IN} = 13$ V	7(b)	0	+2,000	nA
Input low leakage current	I_{IL}	$V_{CC} = V_{DD} = 13$ V; $V_{IN} = 0$ V	7(b)	0	-2,000	nA
High impedance high-level output leakage current	I_{ZH}	$V_{CC} = V_{DD} = 13$ V; $V_{IN} = 13$ V	7(c)	0	+2,000	nA
High impedance low-level output leakage current	I_{ZL}	$V_{CC} = V_{DD} = 13$ V; $V_{IN} = 0$ V	7(c)	0	-2,000	nA
Low clock $\overline{XTAL}$ output voltage	V_{OLX}	$V_{CLOCK} = 1.5$ V; $V_{CC} = V_{DD} = 5$ V; $T_A = 25°C$		4.5	---	V

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_A \leq +125°C$	Figure	Limits		Unit
				Min	Max	
High clock $\overline{XTAL}$ output voltage	V_{OHX}	V_{CLOCK} = 3.5 V; V_{CC} = V_{DD} = 5 V; T_A = 25°C		---	0.5	V
Negative $\overline{XTAL}$ threshold voltage	V_{TNX}	V_{DD} = 5 V; V_{SS} = GND; V_{CC} = OPEN; I_{CLOCK} = 10 μA; T_A = 25°C		.30	2.75	V
Positive $\overline{XTAL}$ threshold voltage	V_{TPX}	V_{CC} = V_{DD} = GND; V_{SS} = OPEN; I_{CLOCK} = -10 μA; T_A = 25°C		-.30	-2.75	V
Positive clamping input to V_{DD}	V_{IC}(pos)	V_{CC} = V_{DD} = GND; V_{SS} = OPEN; I_I = 1 mA; T_A = 25°C		---	1.5	V
Negative clamping input to V_{SS}	V_{IC}(neg)	V_{SS} = GND; V_{CC} & V_{DD} = OPEN; I_I = 1 mA; T_A = 25°C		---	-1.5	V
Maximum frequency	f_{MAX}	V_{CC} = V_{DD} = 5 V		1.5	---	MHz
	f_{MAX}	V_{CC} = V_{DD} = 10 V		3.8	---	MHz

TABLE I. Electrical performance characteristics - Continued.

Test			Symbol	Conditions $-55°C \leq T_A \leq +125°C$	Figure	Limits				Unit
	Clock ref	Signal				Cond A		Cond B		
						Min	Max	Min	Max	
Propagation delay times	1*	TPA	t_{PLH1}	C_L = 50 pF; f = 1 MHz	8, 9	---	550	---	300	ns
	2*	TPA	t_{PHL1}			100	550	50	300	ns
	6**	TPB	t_{PLH1}	Cond A: $V_{CC} = V_{DD} = 5$ V		---	550	---	300	ns
	7**	TPB	t_{PHL1}	Cond B: $V_{CC} = V_{DD} = 10$ V		100	550	50	300	ns
	0*	Memory high-address byte	t_{PLH5}, t_{PHL5}			---	1,650	---	700	ns
	2**	Memory low-address byte	t_{PLH6}, t_{PHL6}			140	650	70	400	ns
	0*	$\overline{MRD}$	t_{PLH2}			---	600	---	350	ns
	1**	$\overline{MRD}$	t_{PHL2}			---	600	---	350	ns
	7*	$\overline{MWR}$	t_{PLH3}			---	550	---	300	ns
	5*	$\overline{MWR}$	t_{PHL3}			---	550	---	300	ns
	1**	DATA from CPU to BUS	t_{PZH1}, t_{PZL1}			---	700	---	450	ns
	0*	DATA from CPU to BUS	t_{PHZ1}, t_{PLZ1}			---	700	---	450	ns
	0*	State code	t_{PLH7}, t_{PHL7}			---	850	---	400	ns
	3**	Q	t_{PLH8}, t_{PHL8}			---	750	---	350	ns
	0*	N0-N2	t_{PLH4}, t_{PHL4}			---	1,000	---	450	ns

* Falling edge of clock pulse.

** Rising edge of clock pulse.

TABLE I. Electrical performance characteristics - Continued.

Test			Symbol	Conditions $-55°C \leq T_A \leq +125°C$	Figure	Limits		Unit
	Clock ref	Signal				Cond A Min***	Cond B Min***	
Target setup and hold times	7**	DATA from BUS to CPU	t_{SLH1}, t_{SHL1}	C_L = 50 pF; f = 1 MHz	10	50	80	ns
			t_{HLH1}, t_{HHL1}	Cond A: $V_{CC} = V_{DD} = 5$ V		450	250	ns
	7*	$\overline{INTERRUPT}$, $\overline{DMA}$	t_{SHL2}	Cond B: $V_{CC} = V_{DD} = 10$ V		50	90	ns
			t_{HLH2}			300	200	ns
	3*	$\overline{WAIT}$	t_{SHL4}			100	150	ns
	1**	$\overline{EF}$	t_{SLH3}, t_{SHL3}			70	100	ns
			t_{HLH3}, t_{HHL3}			350	200	ns
$\overline{CLEAR}$ pulse width			t_{WL2}			500	250	ns
CLOCK pulse width			t_{WL1}, t_{WH1}			250	110	ns

* Falling edge of clock pulse.

** Rising edge of clock pulse.

*** These limits are the minimum setup and hold times and pulse widths required for system design.

c. Interim and final electrical parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

d. The constant acceleration test per 3.1.4 of method 5004 shall be performed using test condition D.

TABLE II. Electrical test requirements.

MIL-STD-883 method	MIL-STD-883 test requirements	Subgroups table III) Class B devices
5004	Interim electrical parameters (pre burn-in) (method 5004)	1,7 (optional)
	Interim electrical parameters (between 2 static burn-ins and between static test II and dynamic burn-in)	N/A
	Final electrical test parameters (method 5004)	1*,2,7* 8(+125°C only)
5005	Group A test electrical tests	1,2,4**,7, 8,9**,10**
	Group B electrical parameters	None
	V_{ZAP}	4.5.3
	Group C end-point electrical parameters	1,2,7,8
	Additional electrical subgroups for group C periodic inspections	None
	Group D end-point electrical parameters	1,2,7,8

* PDA applies to subgroups 1 and 7 (see 4.2b).
**These subgroups are used for initial QCI only (see 4.4.1b and 4.4.1f).

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4). Generic test data (see 6.7) may be used to satisfy the requirements for groups C and D inspections. Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD value shown in table I of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 of method 5005 of MIL-STD-883 shall be omitted.

c. Instruction mnemonies for the functional tests of subgroups 7 and 8 and switching tests of subgroups 9, 10, and 11 shall be as specified in table IV.

d. Test vectors for subgroups 7 through 11 shall be as defined in table VI. (See 6.2).

e. For class B devices, subgroups 9 and 10 shall be performed only during initial OCI.

f. The output/load circuit for subgroups 7 through 11 shall be as shown on figure 4.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Subgroup 7 shall be added to the group B inspection requirements for class B devices and shall consist of the test, conditions, and limits specified in 4.5.3. The LTPD for this subgroup shall be 20.

4.4.3 Group C and D inspection. Groups C and D inspections shall consist of the test subgroups and LTPD values shown in table III and IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Use the circuit shown on figure 3.

(2) T_A = +125°C, minimum.

c. Additional electrical subgroups as specified in table II shall be added to the group C inspection requirements for class B devices.

4.4.4 Constant acceleration. The constant acceleration tests of groups B, C, and D shall be performed using test condition D.

4.5 Methods of examination and test. Methods of examination and tests shall be as specified as specified follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.3 High voltage (V_{ZAP}) test of input protection circuits. Unless otherwise specified, four input terminals of the device under test (DUT) shall be subjected to a voltage pulse from a 100 pF source charged to 400 V. This destructive test shall be conducted as follows using the test circuit on figure 5:

a. Select one input terminal from each of the following groups:

(1) CLOCK (pin 1).
(2) $\overline{\text{DMA-IN}}$, $\overline{\text{DMA-OUT}}$, $\overline{\text{INTERRUPT}}$ (pins 36, 37, 38).
(3) DATA BUS (pins 8 through 15).
(4) All other inputs (pins 2, 3, 21, 22, 23, 24).

b. Measure I_{IH} and I_{IL} at the selected terminals of the DUT at 25°C. Also measure I_{SS} at 25°C with $V_{CC} = V_{DD}$ = 13 V dc. These measurements shall be made in accordance with table III herein. The test limits shall be as specified in table III.

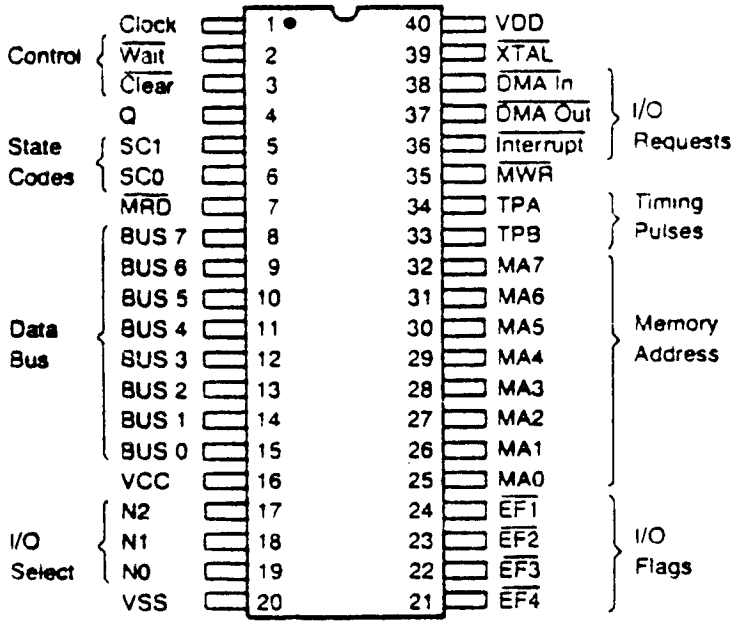


FIGURE 1. Terminal connections.

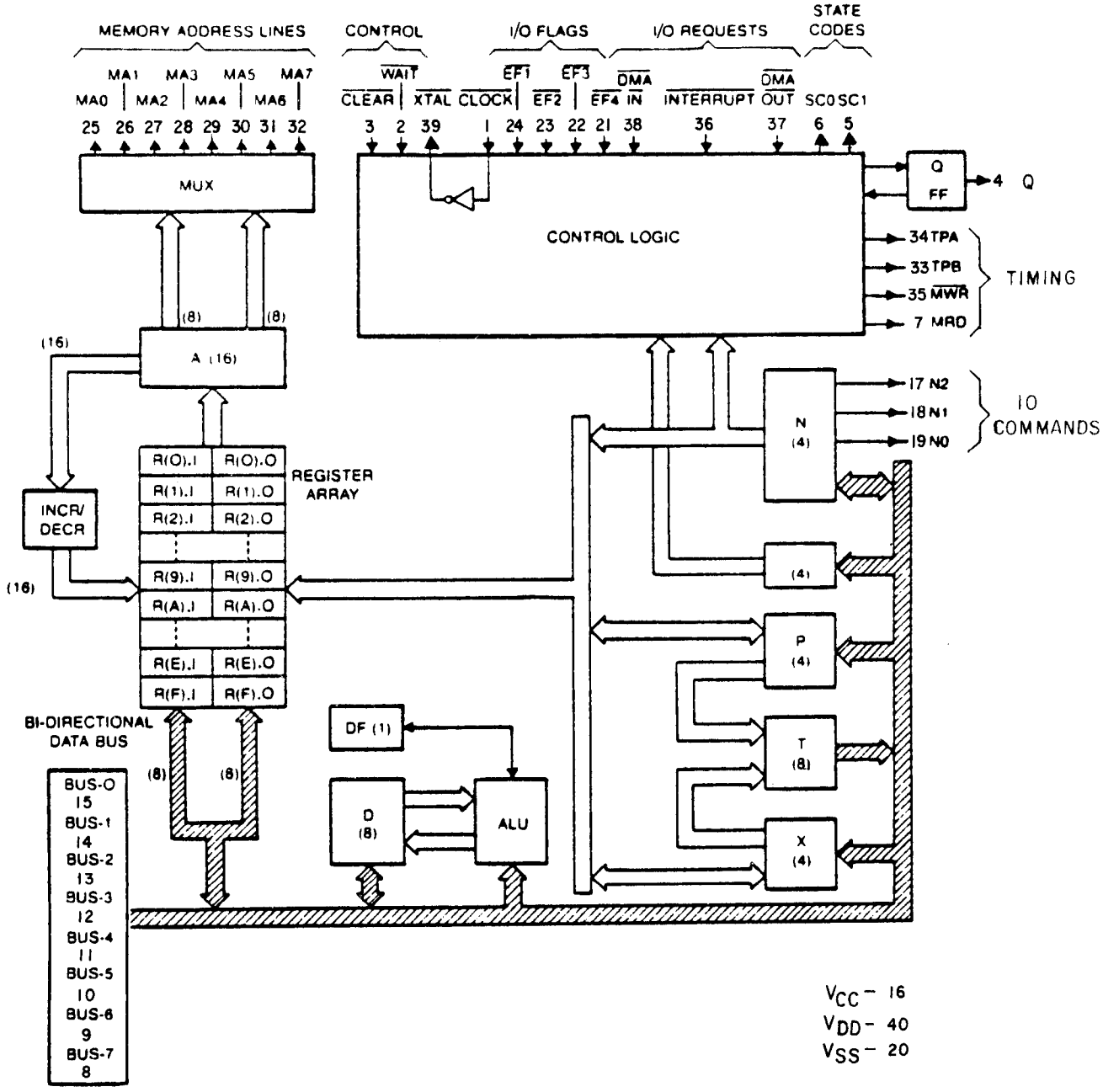


FIGURE 2. Functional block diagram.

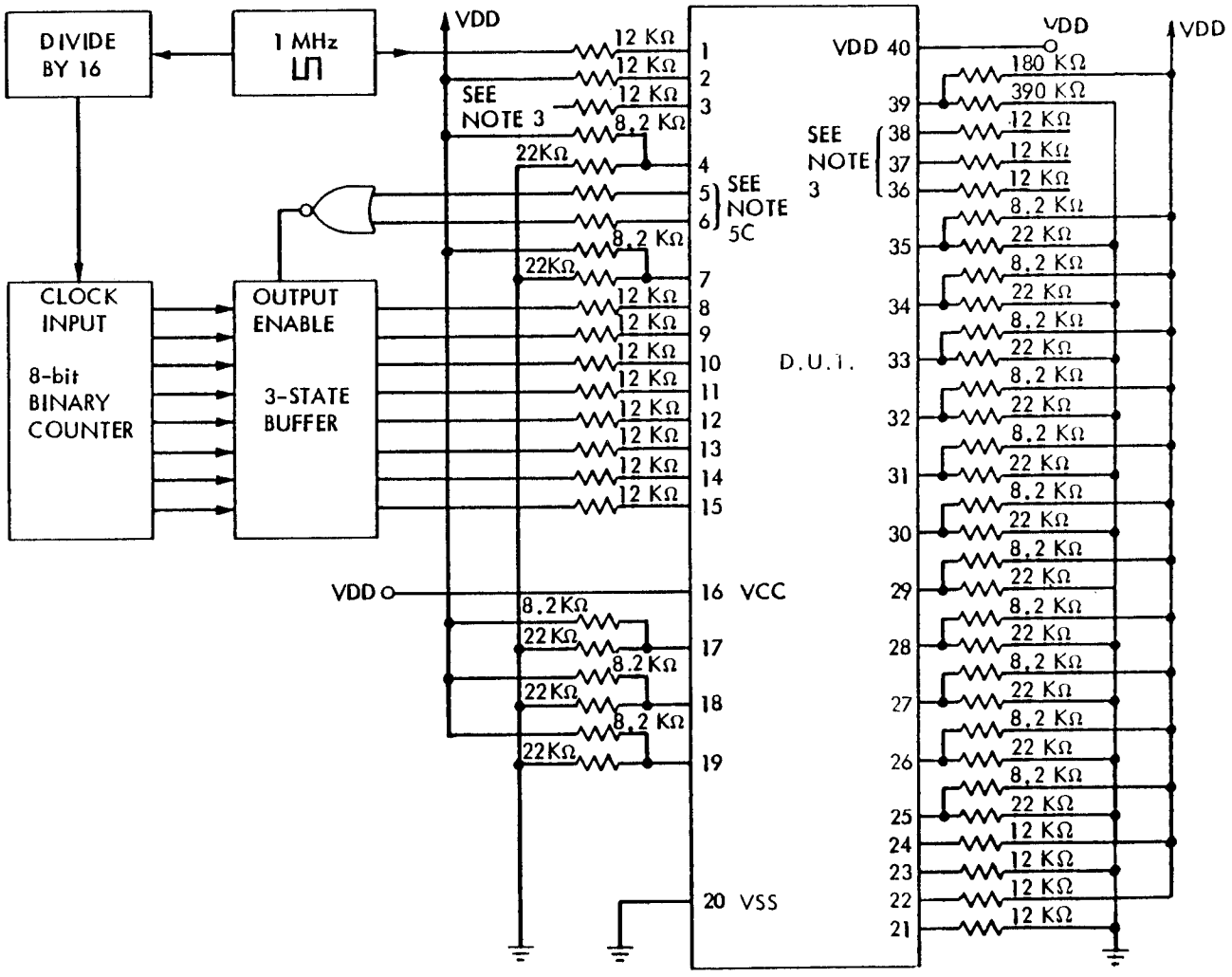
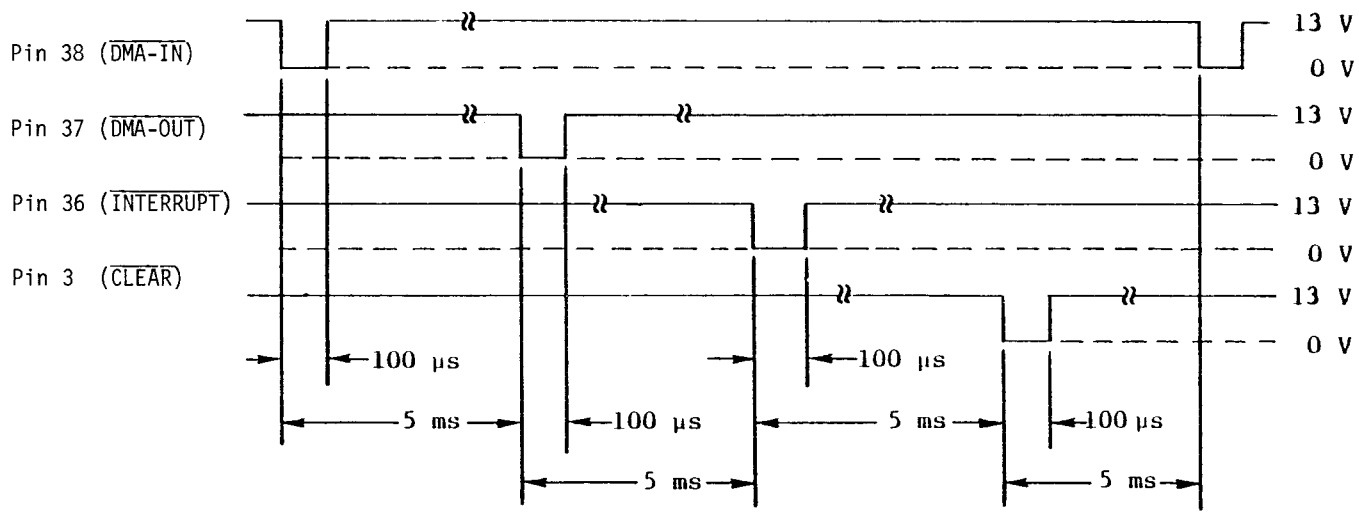


FIGURE 3. Dynamic burn-in and operating life test circuit.

NOTES:
1. Tolerance on all resistors is ±10%.
2. V_{DD} = 13 volts minimum.
3. Pins 3, 36, 37, and 38 shall be activated sequentially as shown in the timing diagram below:



4. The clock input (pin 1) shall be driven by a 1 MHz square wave, 50% duty cycle, 13 volts peak-to-peak.
5. The circuit for driving the data bus is optional. Any circuit which meets the following requirements is acceptable:

   a. The data bus of each device under test (D.U.T.) shall be protected by a 3-state buffer which is in the high impedance state except when the state code lines of that D.U.T. are both low (i.e., the microprocessor is in the S0, or fetch, state).

   b. Each of the 256 possible 8-bit binary bytes shall be applied to the inputs of the 3-state buffer, changing every 16 clock pulses. No input combination shall be repeated until all other combinations have been applied.

   c. Resistors at pins 5 and 6 shall be selected as required for proper operation of the external circuit.

FIGURE 3. Dynamic burn-in and operating life test circuit - Continued.

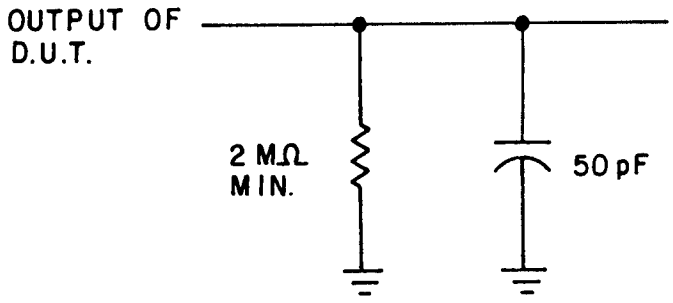
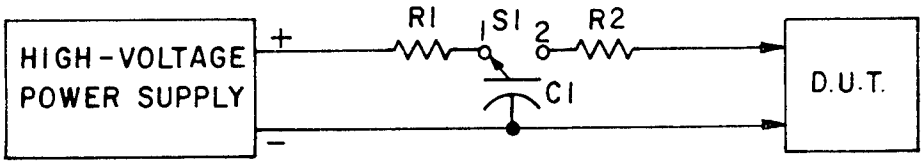


FIGURE 4. Output load circuit for functional and switching tests.

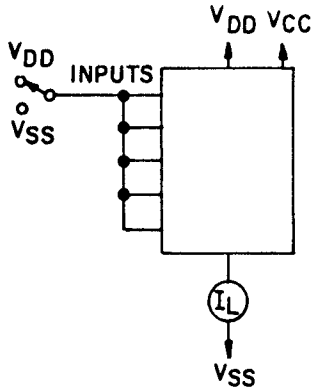


V_{ZAP} = 400 V charge on C1.
10 MΩ ≤ R1 ≤ 50 MΩ.
R2 = 1.5 kilohms.
C1 = 100 pF.
S1 = Hg-wetted "bounceless" relay

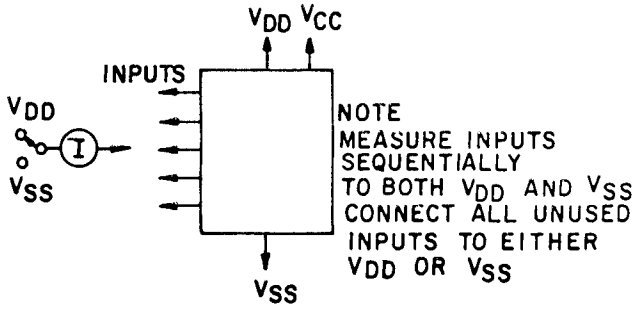
Modes for high voltage test.

Mode	+ Terminal	- Terminal
1	V_{DD}	Input
2	Input	V_{SS}
3	Input	Associated output
4	Associated output	Input

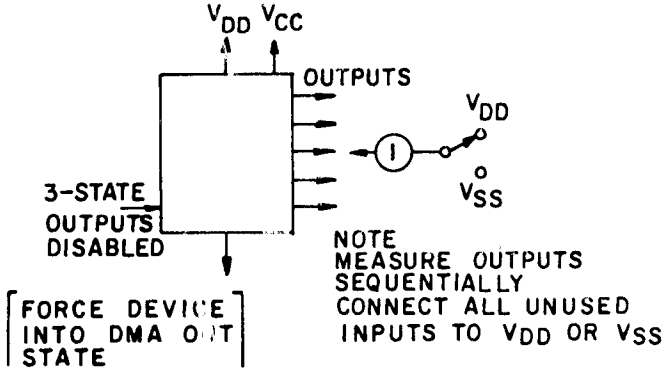
FIGURE 5. High voltage (V_{ZAP}) test circuits.



(a) Quiescent device current



(b) Input leakage current



(c) High-impedance output leakage current

FIGURE 6. DC parameter test circuits.

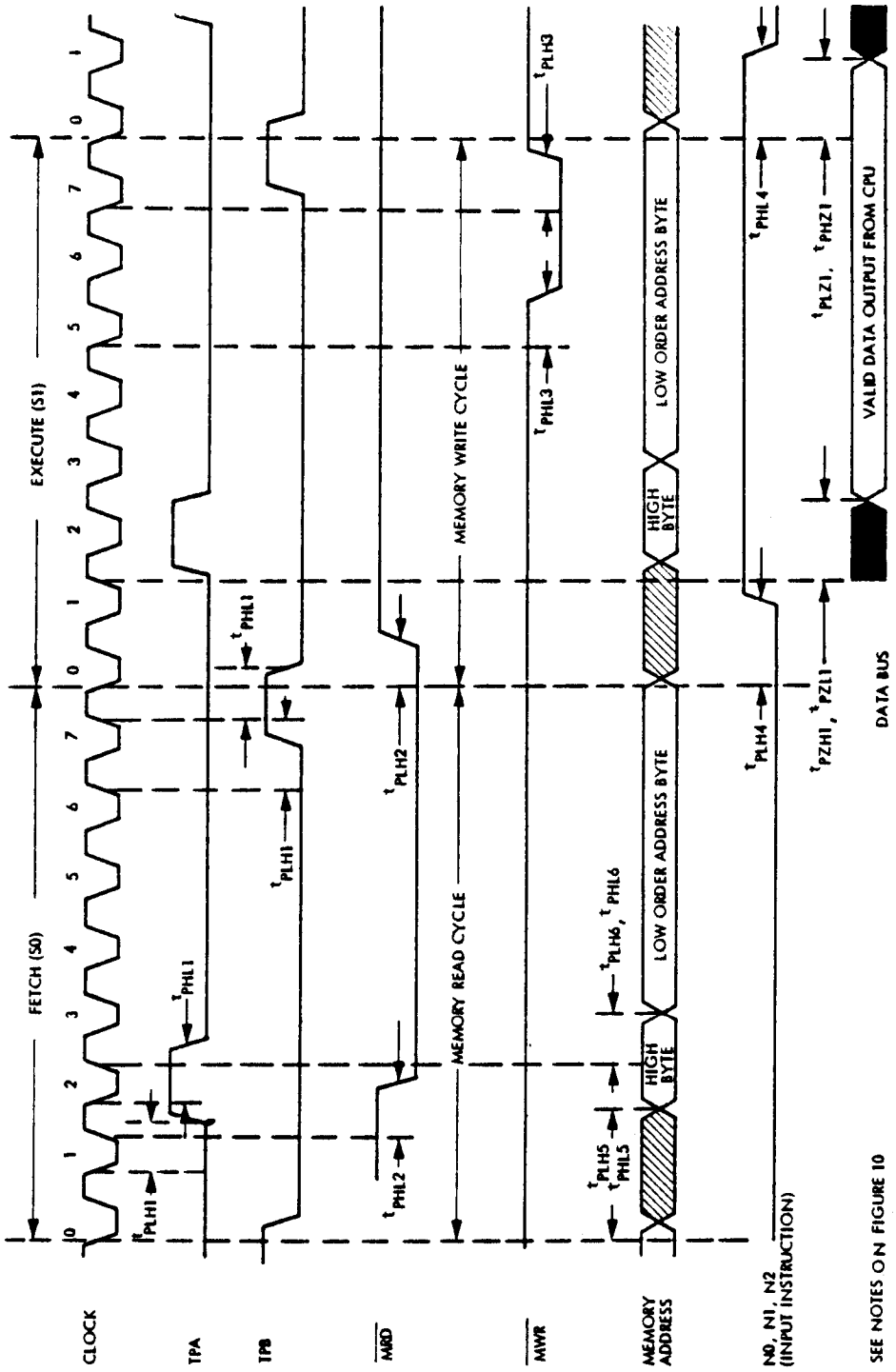


FIGURE 7. Output timing diagram (memory write instructions).

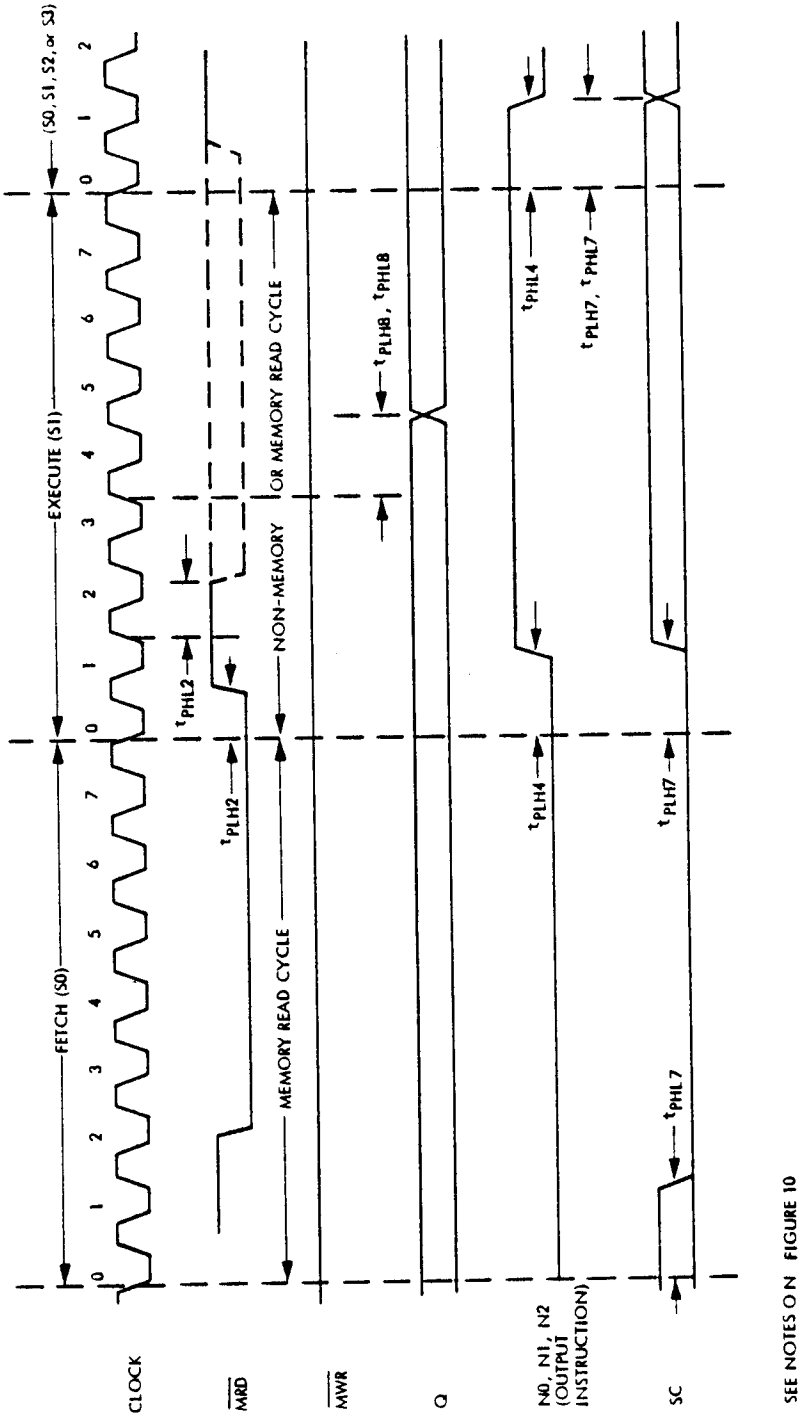
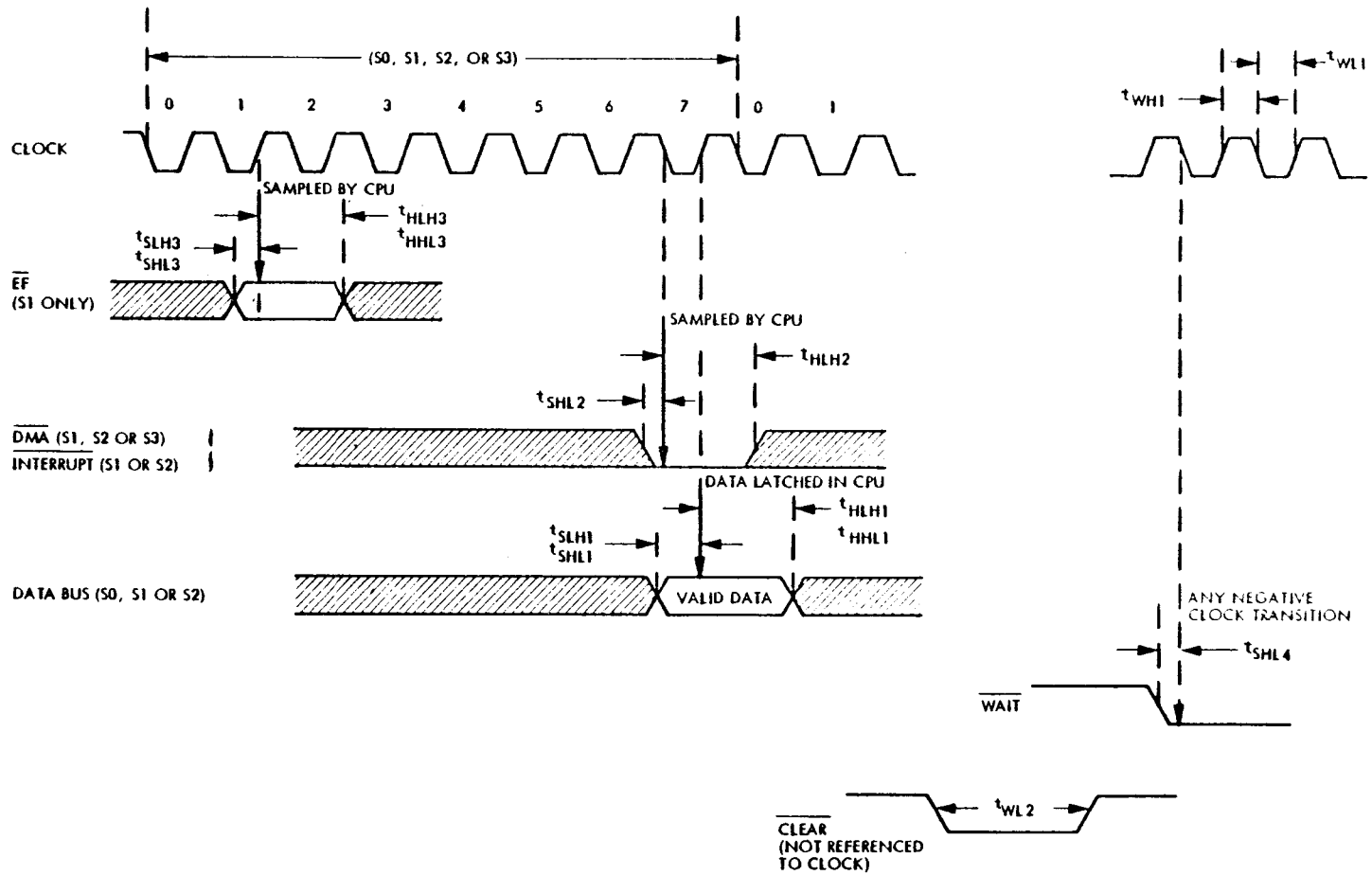


FIGURE 8. Output timing diagram (control outputs).



NOTES:
1. Timing diagrams are used to show signal relationships only.
2. All measurements are referenced to 50% point of the waveforms.
3. Shaded areas indicate "don't care" on inputs or undefined states on outputs. Multiple transitions may occur during this period.
4. Solid areas indicate high-impedance state.

FIGURE 9. Input timing diagram.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	TEST No.	1 CLOCK	2 $\overline{WAIT}$	3 $\overline{CLEAR}$	4 Q	5 SC1	6 SC0	7 $\overline{MRD}$	8 BUS 7	9 BUS 6	10 BUS 5	11 BUS 4	12 BUS 3	13 BUS 2	14 BUS 1	15 BUS 0	16 V_{CC}	17 N2	18 N1	19 N0	20 V_{SS}
V_{IC}(pos)		1	1 mA															GND				
		2		1 mA																		
		3			1 mA																	
		4								1 mA												
		5									1 mA											
		6										1 mA										
		7											1 mA									
		8												1 mA								
		9													1 mA							
		10														1 mA						
		11															1 mA					
		12																				
		13																				
		14																				
		15																				
		16																				
		17																				
		18																				
V_{IC}(neg)		19	-1 mA																			GND
		20		-1 mA																		
		21			-1 mA																	
		22								-1 mA												
		23									-1 mA											
		24										-1 mA										
		25											-1 mA									
		26												-1 mA								
		27													-1 mA							
		28														-1 mA						
		29															-1 mA					
		30																				
		31																				
		32																				
		33																				
		34																				
		35																				
		36																				
I_{SS}	3005	37	GND	5 V	GND													5 V				0 V
I_{SS}	3005	38	GND	10 V	GND													10 V				0 V
I_{SS}	3005	39	GND	13 V	GND													13 V				0 V
I_{IH}	3010	40	13 V	0 V	0 V													13 V				GND
		41	0 V	13 V	0 V																	
		42		0 V	13 V																	
		43			0 V																	
		44																				
		45																				
		46																				
		47																				
		48																				
		49																				
I_{IH} 1/	3010	50		13 V																		
		51	GND	13 V	13 V					13 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V					
I_{IH}	3010	52	GND	13 V	13 V					0 V	13 V	0 V	0 V	0 V	0 V	0 V	0 V					

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Test No.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits Subgroup 1 T_A = 25°C Min	Subgroup 1 Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 Max	Unit
	$\overline{EF4}$	$\overline{EF3}$	$\overline{EF2}$	$\overline{EF1}$	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	TPB	TPA	$\overline{MWR}$	$\overline{INTR}$	$\overline{DMA-0}$	$\overline{DMA-I}$	$\overline{XTAL}$	V_{DD}								
1																				GND	CLOCK		1.5					V
2																					$\overline{WAIT}$							
3																					$\overline{CLEAR}$							
4																					BUS 7							
5																					BUS 6							
6																					BUS 5							
7																					BUS 4							
8																					BUS 3							
9																					BUS 2							
10																					BUS 1							
11																					BUS 0							
12	1 mA																				$\overline{EF4}$							
13		1 mA																			$\overline{EF3}$							
14			1 mA																		$\overline{EF2}$							
15				1 mA																	$\overline{EF1}$							
16																1 mA					$\overline{INTR}$							
17																	1 mA				$\overline{DMA-0}$							
18																		1 mA			$\overline{DMA-I}$							
19																					CLOCK		-1.5					
20																					$\overline{WAIT}$							
21																					$\overline{CLEAR}$							
22																					BUS 7							
23																					BUS 6							
24																					BUS 5							
25																					BUS 4							
26																					BUS 3							
27																					BUS 2							
28																					BUS 1							
29																					BUS 0							
30	-1 mA																				$\overline{EF4}$							
31		-1 mA																			$\overline{EF3}$							
32			-1 mA																		$\overline{EF2}$							
33				-1 mA																	$\overline{EF1}$							
34																-1 mA					$\overline{INTR}$							
35																	-1 mA				$\overline{DMA-0}$							
36																		-1 mA			DMA-I							
37	5 V	5 V	5 V	5 V												5 V	5 V	5 V		5 V	V_{SS}	0	-50	0	-500	0	-50	μA
38	10 V	10 V	10 V	10 V												10 V	10 V	10 V		10 V	V_{SS}		-100		-1,000		-100	
39	13 V	13 V	13 V	13 V												13 V	13 V	13 V		13 V	V_{SS}		-200		-1,500		-200	
40	0 V	0 V	0 V	0 V												0 V	0 V	0 V		13 V	CLOCK		0.3		2		0.3	
41	0 V																				$\overline{WAIT}$							
42	0 V																				$\overline{CLEAR}$							
43	13 V																				$\overline{EF4}$							
44	0 V	13 V																			$\overline{EF3}$							
45		0 V	13 V																		$\overline{EF2}$							
46			0 V	13 V																	$\overline{EF1}$							
47				0 V												13 V					$\overline{INTR}$							
48				0 V												0 V	13 V				$\overline{DMA-0}$							
49				0 V												0 V	0 V	13 V			$\overline{DMA-I}$							
50																	GND				---							
51																	GND		13 V		BUS 7	0	0.3	0	2	0	0.3	μA
52																	GND		13 V		BUS 6	0	0.3	0	2	0	0.3	μA

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	1 CLOCK	2 $\overline{WAIT}$	3 $\overline{CLEAR}$	4 Q	5 SC1	6 SC0	7 $\overline{MRD}$	8 BUS 7	9 BUS 6	10 BUS 5	11 BUS 4	12 BUS 3	13 BUS 2	14 BUS 1	15 BUS 0	16 V_{CC}	17 N2	18 N1	19 N0	20 V_{SS}
I_{IH}	3010	53	GND	13 V	13 V					0 V	0 V	13 V	0 V	0 V	0 V	0 V	0 V	13 V				GND
		54										0 V	13 V	0 V	0 V							
		55											0 V	13 V	0 V							
		56												0 V	13 V							
		57												0 V	0 V	13 V						
		58												0 V	0 V	0 V	13 V					
I_{IL}	3009	59	0 V																			
		60	13 V	0 V																		
		61		13 V	0 V																	
		62			13 V																	
		63																				
		64																				
		65																				
		66																				
		67																				
		68																				
1/ $\overline{I_{IL}}$	3009	69																				
		70	GND		13 V					0 V	13 V	13 V	13 V	13 V	13 V	13 V	13 V					
		71								13 V	0 V	13 V	13 V									
		72									13 V	0 V	13 V									
		73										13 V	0 V									
		74											13 V	0 V								
		75												13 V	0 V							
		76												13 V	13 V	0 V						
		77												13 V	13 V	13 V	0 V					
2/ I_{ZH}		78																				
		79	GND							13 V	0 V	0 V	0 V	0 V	0 V	0 V	0 V					
		80								0 V	13 V	0 V	0 V									
		81									0 V	13 V	0 V									
		82										0 V	13 V									
		83											0 V	13 V								
		84												0 V	13 V							
		85												0 V	0 V	13 V						
		86												0 V	0 V	0 V	13 V					
I_{ZL}		87									13 V	13 V	13 V	13 V	13 V	13 V						
		88								13 V	0 V	13 V	13 V									
		89									13 V	0 V	13 V									
		90										13 V	0 V									
		91											13 V	0 V								
		92												13 V	0 V							
		93												13 V	13 V	0 V						
		94												13 V	13 V	13 V	0 V					
I_{OL}	4/	95				0.4 V												5 V				
		96					0.4 V															
		97						0.4 V														
		98							0.4 V													
		99								0.4 V												
		100									0.4 V											
		101										0.4 V										
		102											0.4 V									
		103												0.4 V								
		104													0.4 V							
		105														0.4 V						

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Test No.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits: Subgroup 1 T_A = 25°C Min	Subgroup 1 Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 Max	Unit
	$\overline{EF4}$	$\overline{EF3}$	$\overline{EF2}$	$\overline{EF1}$	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	TPB	TPA	$\overline{MWR}$	$\overline{INTR}$	$\overline{DMA-0}$	$\overline{DMA-I}$	$\overline{XTAL}$	V_{DD}								
53																	GND	13 V	13 V	13 V	BUS 5	0	0.3	0	2	0	0.3	μA
54																					BUS 4							
55																					BUS 3							
56																					BUS 2							
57																					BUS 1							
58																					BUS 0							
59	13 V	13 V	13 V	13 V												13 V	13 V						-0.3		-2		-0.3	
60	13 V																											
61	13 V																				$\overline{CLEAR}$							
62	0 V																				$\overline{EF4}$							
63	13 V	0 V																			$\overline{EF3}$							
64		13 V	0 V																		$\overline{EF2}$							
65			13 V	0 V																	$\overline{EF1}$							
66				13 V												0 V					$\overline{INTR}$							
67				13 V												13 V	0 V				$\overline{DMA-0}$							
68				13 V												13 V	13 V	0 V			$\overline{DMA-I}$							
69																	GND	13 V			---							
70																			13.0		BUS 7	0	-0.3	0	-2	0	-0.3	μA
71																					BUS 6							
72																					BUS 5							
73																					BUS 4							
74																					BUS 3							
75																					BUS 2							
76																					BUS 1							
77																					BUS 0							
78																					---							
79																			13 V		BUS 7	0	0.3	0	2	0	0.3	μA
80																					BUS 6							
81																					BUS 5							
82																					BUS 4							
83																					BUS 3							
84																					BUS 2							
85																					BUS 1							
86																					BUS 0							
87																					BUS 7		-0.3		-2		-0.3	
88																					BUS 6							
89																					BUS 5							
90																					BUS 4							
91																					BUS 3							
92																					BUS 2							
93																					BUS 1							
94																					BUS 0							
95																				5 V	Q	1.50	---	0.95	---	1.80	---	mA
96																					SC1							
97																					$\overline{SC0}$							
98																					$\overline{MRD}$							
99																					BUS 7							
100																					BUS 6							
101																					BUS 5							
102																					BUS 4							
103																					BUS 3							
104																					BUS 2							
105																					BUS 1							

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	1 CLOCK	2 $\overline{WAIT}$	3 $\overline{CLEAR}$	4 Q	5 SC1	6 SC0	7 $\overline{MRD}$	8 BUS 7	9 BUS 6	10 BUS 5	11 BUS 4	12 BUS 3	13 BUS 2	14 BUS 1	15 BUS 0	16 V_{CC}	17 N2	18 N1	19 N0	20 V_{SS}
I_{OL}		106															0.4 V	5 V	0.4 V	0.4 V	0.4 V	GND
		107																				
		108																				
		109																				
		110																				
		111																				
		112																				
		113																				
		114																				
		115																				
		116																				
		117																				
		118																				
		119																				
		120																				
		121				0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	0.5 V	10 V	0.5 V	0.5 V	0.5 V	
		122																				
		123																				
		124																				
		125																				
		126																				
		127																				
		128																				
		129																				
		130																				
		131																				
		132																				
		133																				
		134																				
		135																				
		136																				
		137																				
		138																				
		139																				
		140																				
		141																				
		142																				
		143																				
		144																				
		145																				
		146																				
I_{OH}		147				4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	4.6 V	5 V	4.6 V	4.6 V	4.6 V	
		148																				
		149																				
		150																				
		151																				
		152																				
		153																				
		154																				
		155																				
		156																				
		157																				
		158																				
		159																				
		160																				
		161																				

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Test No.	21 $\overline{EF4}$	22 $\overline{EF3}$	23 $\overline{EF2}$	24 $\overline{EF1}$	25 MA0	26 MA1	27 MA2	28 MA3	29 MA4	30 MA5	31 MA6	32 MA7	33 TPB	34 TPA	35 $\overline{MWR}$	36 $\overline{INTR}$	37 $\overline{DMA-0}$	38 $\overline{DMA-1}$	39 $\overline{XTAL}$	40 V_{DD}	Measured terminal	Test limits: Subgroup 1 T_A = 25°C Min	Subgroup 1 Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 Max	Unit
106																				5 V	BUS 0	1.50		0.95		1.80		mA
107																					N2							
108																					N1							
109																					N0							
110					0.4 V																MA0							
111						0.4 V															MA1							
112							0.4 V														MA2							
113								0.4 V													MA3							
114									0.4 V												MA4							
115										0.4 V											MA5							
116											0.4 V										MA6							
117												0.4 V									MA7							
118													0.4 V								TPB							
119														0.4 V							TPA							
120															0.4 V						$\overline{MWR}$							
121																				10 V	Q	2.80		1.70		3.30		
122																					SC1							
123																					SC0							
124																					$\overline{MRD}$							
125																					BUS 7							
126																					BUS 6							
127																					BUS 5							
128																					BUS 4							
129																					BUS 3							
130																					BUS 2							
131																					BUS 1							
132																					BUS 0							
133																					N2							
134																					N1							
135																					N0							
136					0.5 V																MA0							
137						0.5 V															MA1							
138							0.5 V														MA2							
139								0.5 V													MA3							
140									0.5 V												MA4							
141										0.5 V											MA5							
142											0.5 V										MA6							
143												0.4 V									MA7							
144													0.5 V								TPB							
145														0.5 V							TPA							
146															0.5 V						$\overline{MWR}$							
147																				5 V	Q	-0.35		-0.23		-0.42		
148																					SC1							
149																					SC0							
150																					$\overline{MRD}$							
151																					BUS 7							
152																					BUS 6							
153																					BUS 5							
154																					BUS 4							
155																					BUS 3							
156																					BUS 2							
157																					BUS 1							
158																					BUS 0							
159																					N2							
160																					N1							
161																					N0							

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	1 CLOCK	2 $\overline{WAIT}$	3 $\overline{CLEAR}$	4 Q	5 SC1	6 SC0	7 $\overline{MRD}$	8 BUS 7	9 BUS 6	10 BUS 5	11 BUS 4	12 BUS 3	13 BUS 2	14 BUS 1	15 BUS 0	16 V_{CC}	17 N2	18 N1	19 N0	20 V_{SS}
I_{OH}		162																5 V				GND
		163																				
		164																				
		165																				
		166																				
		167																				
		168																				
		169																				
		170																				
		171																				
		172																				
		173				9.5 V												10 V				
		174					9.5 V															
		175						9.5 V														
		176							9.5 V													
		177								9.5 V												
		178									9.5 V											
		179										9.5 V										
		180											9.5 V									
		181												9.5 V								
		182													9.5 V							
		183														9.5 V						
		184															9.5 V					
		185																	9.5 V			
		186																		9.5 V		
		187																			9.5 V	
		188																				
		189																				
		190																				
		191																				
		192																				
		193																				
		194																				
		195																				
		196																				
		197																				
		198																				
I_{OLX}		199	5 V	5 V	GND													5 V				
I_{OHX}		200	GND																			
V_{OLX}		201	1.5 V																			
V_{OHX}		202	3.5 V																			
V_{TNX}		203	10 μA	GND																		
V_{TPX}		204	-10 μA	GND														GND				

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Test No.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test limits: Subgroup 1 T_A = 25°C Min	Subgroup 1 Max	Subgroup 2 T_A = 125°C Min	Subgroup 2 Max	Subgroup 3 T_A = -55°C Min	Subgroup 3 Max	Unit
	$\overline{EF4}$	$\overline{EF3}$	$\overline{EF2}$	$\overline{EF1}$	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	TPB	TPA	$\overline{MWR}$	$\overline{INTR}$	$\overline{DMA-0}$	$\overline{DMA-I}$	$\overline{XTAL}$	V_{DD}								
162					4.6 V															5 V	MA0	-0.35		-0.23		-0.42		mA
163						4.6 V															MA1							
164							4.6 V														MA2							
165								4.6 V													MA3							
166									4.6 V												MA4							
167										4.6 V											MA5							
168											4.6 V										MA6							
169												4.6 V									MA7							
170													4.6 V								TPB							
171														4.6 V							TPA							
172															4.6 V						$\overline{MWR}$							
173																				10 V	Q	-0.85		-0.54		-0.95		
174																					SC1							
175																					$\overline{SC0}$							
176																					$\overline{MRD}$							
177																					BUS 7							
178																					BUS 6							
179																					BUS 5							
180																					BUS 4							
181																					BUS 3							
182																					BUS 2							
183																					BUS 1							
184																					BUS 0							
185																					N2							
186																					N1							
187																					N0							
188					9.5 V																MA0							
189						9.5 V															MA1							
190							9.5 V														MA2							
191								9.5 V													MA3							
192									9.5 V												MA4							
193										9.5 V											MA5							
194											9.5 V										MA6							
195												9.5 V									MA7							
196													9.5 V								TPB							
197														9.5 V							TPA							
198															9.5 V						$\overline{MWR}$							
199	5 V	5 V	5 V	5 V												5 V	5 V	5 V	0.4 V	5 V	$\overline{XTAL}$	100		66		120		μA
200	5 V	5 V	5 V	5 V															4.6 V		$\overline{XTAL}$	-50		-33		-60		μA
201																			OUT		$\overline{XTAL}$	4.5						V
202																			OUT		$\overline{XTAL}$		0.5					
203																GND	GND	GND			CLOCK 3/	0.30	2.75					
204																GND	GND	GND		GND	CLOCK 3/	-0.30	-2.75					

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	Instruction sequence (per table IV)	Vectors (per table V)	Clock input conditions (see fig 9)		Supply voltage conditions				Functional output cond/limits (C_L = 50 pF)		Threshold limits		Measured terminal	Test limits						Unit
																Subgroup 7 T_A = 25°C		Subgroup 8 T_A = 125°C		Subgroup 8 T_A = -55°C		
					f_{CL}	t_{WL}	V_{CC}	V_{DD}	V_{IH}	V_{IL}	V_{OH}	V_{OL}	V_{IH}	V_{IL}		Min	Max	Min	Max	Min	Max	
									All inputs													
V_{IH}, V_{IL} (functional tests)		205	AC	All	1.0 MHz	250 ns	5 V	5 V			4.5 V	0.5 V	3.5 V	1.2 V	All outputs except XTAL							
		206	IT	1 to 161			5 V	5 V			4.5 V	0.5 V	3.5 V	1.2 V								
		207	AC	All			10 V	10 V			9.0 V	1.0 V	7.0 V	3.0 V								
		208	IT	1 to 161			10 V	10 V			9.0 V	1.0 V	7.0 V	3.0 V								
f_{max}		209	MF	All	5/	5/	5 V	5 V	5 V	0 V	3.0 V	2.0 V										
f_{max}		210	MF		6/	6/	10 V	10 V	10 V		6.0 V	4.0 V										
Main functional tests	3014	211	0 to C		1.2 MHz	250 ns	4.5 V	4.5 V	4.5 V		3.5 V	1.0 V										
		212	0 to C		2.4 MHz	150 ns	9 V	9 V	9 V		7.0 V	2.0 V										
		213	0 to C		2.4 MHz	150 ns	11 V	11 V	11 V		8.0 V	2.0 V										

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	General test conditions, waveforms	Supply voltage conditions				Instruction sequence (per table IV)	Vectors (per table V)	t_{WL} (clock)	Reference clock cycle edge	Measured terminal 7/	Test limits						Unit
													Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
				V_{CC}	V_{DD}	V_{IH}	V_{IL}						Min	Max	Min	Max	Min	Max	
t_{PLH1} (TPA)	3003	214	f_{CL} = 1 MHz,	5 V	5 V	5 V	0 V	AC		250 ns	1 falling	34		450		550		400	ns
t_{PHL1} (TPA)		215	C_L = 50 pF								2 falling	34	130		160		100		
t_{PLH1} (TPB)		216	(see fig 7,8, 9)								6 rising	33							
t_{PHL1} (TPB)		217									7 rising	33	130		160		100		
t_{PLH5}, t_{PHL5} (HI-ADDR)		218									0 falling	25-32		1,200		1,650		1,100	
t_{PLH6}, t_{PHL6} (LO-ADDR)		219									2 rising	25-32	170	550	220	650	140	500	
t_{PLH2} ($\overline{MRD}$)		220									0 falling	7		450		600		400	
t_{PHL2} ($\overline{MRD}$)		221									1 rising	7				600			
t_{PLH3} ($\overline{MWR}$)		223									7 falling	35				550			
t_{PHL3} ($\overline{MWR}$)		224									5 falling	35				550			
t_{PZH1}, t_{PZL1} (DATA)		225									1 rising	8-15		600		700		550	
t_{PLZ1}, t_{PHZ1} (DATA)		226									0 falling	8-15		600		700		550	
t_{PLH7}, t_{PHL7} (SC)	3003	227									0 rising	5, 6		650		850		550	
t_{PLH8}, t_{PHL8} (Q)	3003	228									3 falling	4		600		750		500	
t_{PLH4}, t_{PHL4} (N)	3003	229									0 rising	17-19		800		1,000		700	

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	General test conditions, waveforms	Supply voltage conditions				Instruction sequence (per table IV)	Vectors (per table V)	t_{WL} (clock)	Reference clock cycle edge	Measured terminal 7/	Test limits						Unit
				V_{CC}	V_{DD}	V_{IH}	V_{IL}						Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
													Min	Max	Min	Max	Min	Max	
t_{SLH1}, t_{SHL1} (DATA)		230	f_{CL} = 1 MHz, C_L = 50 pF (see fig 7,8, 9)	5 V	5 V	5 V	0 V	AC		250 ns	7 rising	8-15	0		0		50		ns
t_{HLH1}, t_{HHL1} (DATA)		231								250 ns	7 rising	8-15	350		450		300		
t_{WL1}, t_{WH1} (CLOCK)		232										1	190		250		190		
t_{SLH3}, t_{SHL3} ($\overline{EF}$)		233						IT	1-161, 162-322	250 ns	1 rising	21-24	50		50		70		
t_{HLH3}, t_{HHL3} ($\overline{EF}$)		234							1-161, 162-322		1 rising	21-24	250		350		250		
t_{WL2} ($\overline{CLEAR}$)		235							323-451			3	400		500		350		
t_{SHL2} ($\overline{DMA}$, $\overline{INTR}$)		236							452-620, 621-701, 702-814		7 falling	36-38	30		30		50		
t_{HLH2} ($\overline{DMA}$, $\overline{INTR}$)		237							452-620, 621-701, 702-814		7 falling	36-38	250		300		250		
t_{SHL4} ($\overline{WAIT}$)		238							815-919		3 falling	2	70		70		100		
t_{PLH1} (TPA)	3003	239		10V	10V	10V	0 V	AC			1 falling	34		250		300		220	
t_{PHL1} (TPA)		240									2 falling	34	60		70		50		
t_{PLH1} (TPB)		241									6 rising	33							
t_{PHL1} (TPB)		242									7 rising	33	60		70		50		
t_{PLH5}, t_{PHL5} (HI-ADDR)		243									0 falling	25-32		600		700		500	

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	General test conditions, waveforms	Supply voltage conditions				Instruction sequence (per table IV)	Vectors (per table V)	t_{WL} (clock)	Reference clock cycle edge	Measured terminal 7/	Test limits						Unit
													Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
				V_{CC}	V_{DD}	V_{IH}	V_{IL}						Min	Max	Min	Max	Min	Max	
t_{PLH6}, t_{PHL6} (LO-ADDR)	3003	244	f_{CL} = 1 MHz, C_L = 50 pF, (see fig 7,8, 9)	10V	10V	10V	0 V	AC		250 ns	2 rising	25-32	80	350	100	400	70	300	ns
t_{PLH2} ($\overline{MRD}$)		245									0 falling	7		300		350		270	
t_{PHL2} ($\overline{MRD}$)		246									1 rising	7		300		350		270	
t_{PLH3} ($\overline{MWR}$)		247									7 falling	35		250		300		220	
t_{PHL3} ($\overline{MWR}$)		248									5 falling	35		250		300		220	
t_{PZH1}, t_{PZL1} (DATA)		249									1 rising	8-15		400		450		350	
t_{PLZ1}, t_{PHZ1} (DATA)		250									0 falling	8-15		400		450		350	
t_{PLH7}, t_{PHL7} (SC)	3003	251									0 falling	5, 6		350		400		300	
t_{PLH8}, t_{PHL8} (Q)	3003	252									3 rising	4		300		350		270	
t_{PLH4}, t_{PHL4} (N)	3003	253									0 falling	17-19		400		450		350	
t_{SLH1}, t_{SHL1} (DATA)		254									7 rising	8-15	50		50		80		
t_{HLH1}, t_{HHL1} (DATA)		255									7 rising	8-15	200		250		150		
t_{WL1}, t_{WH1} (CLOCK)		256										1	80		110		80		

See footnotes at end of table.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

Symbol	MIL-STD-883 method	Test No.	General test conditions, waveforms	Supply voltage conditions				Instruction sequence (per table IV)	Vectors (per table V)	t_{WL} (clock)	Reference clock cycle edge	Measured terminal 7/	Test limits						Unit
				V_{CC}	V_{DD}	V_{IH}	V_{IL}						Subgroup 9 T_A = 25°C		Subgroup 10 T_A = 125°C		Subgroup 11 T_A = -55°C		
													Min	Max	Min	Max	Min	Max	
t_{SLH3}, t_{SHL3} ($\overline{EF}$)		257	f_{CL} = 1 MHz, C_L = 50 pF (see fig 7,8, 9)	10V	10V	10V	0 V	IT	1-161, 162-322	250 ns	1 rising	21-24	80		80		100		ns
t_{HLH3}, t_{HHL3} ($\overline{EF}$)		258							1-161, 162-322		1 rising	21-24	150		200		150		
t_{WL2} ($\overline{CLEAR}$)		259							323-451			3	200		250		200		
t_{SHL2} ($\overline{DMA}$, $\overline{INTR}$)		260							452-620, 621-701, 702-814		7 falling	36-38	70		70		90		
t_{HLH2} ($\overline{DMA}$, $\overline{INTR}$)		261							452-620, 621-701, 702-814		7 falling	36-38	150		200		150		
t_{SHL4} ($\overline{WAIT}$)		262							815-919		3 falling	2	100		100		150		

1/ Tests 50 and 69 are preconditioning sequences to assure that the data bus is an input for the next eight tests. The following sequence is recommended:

a. With pin 2 = V_{DD}, take pin 3 to V_{SS}, hold it low for at least 1 millisecond, then take it back to V_{DD}.
b. With pin 37 = GND, apply 10 clock pulses (L-H-L) to pin.
c. BUS is now an input; measure I_{IH} or I_{IL} on pins 8 through 15 as specified in the next eight tests.

2/ Test 78 is a preconditioning sequence to force the device into the DMA-OUT state for the next 16 tests. The following sequence is recommended:

a. With pins 2, 3, 37, and 38 remaining unchanged from their condition for the I_{IL} tests on the data bus, apply 20 clock pulses (L-H-L) to pin 1.
b. BUS is now in the high-impedance state; measure I_{ZH} and I_{ZL} on pins 8 through 15 as specified in the next 16 tests.

3/ Short pin 39 to pin 1 and measure voltage at pin 1, with specified current applied. Voltage shall be measured with respect to pin 20 for test 203, and pin 16 for test 204.

TABLE III. Group A inspection for device type 01 - Continued.
Terminal conditions (pins not designated are open)

4/ Prior to test 95, the device shall be preconditioned for tests 95 through 198. The following sequence is recommended:

a. With pins 2, 3, and 38 unchanged from their condition for the I_{ZL} tests, take pin 37 to V_{CC}.
b. While maintaining voltage on pins 2, 3, 37, and 38, apply 10 clock pulses (L-H-L) to pin 1.

5/ Conditions for test 209.

Subgroups 7 (+25°C) and 8 (-55°C):
f_{CL} = 2.5 MHz, t_{WL} = 190 ns.
Subgroup 8 (+125°C):
f_{CL} = 1.5 MHz, t_{WL} = 250 ns.

6/ Conditions for test 210.

Subgroups 7 (+25°C) and 8 (-55°C):
f_{CL} = 6.2 MHz, t_{WL} = 80 ns.
Subgroup 8 (+125°C):
f_{CL} = 3.8 MHz, t_{WL} = 110 ns.

7/ Where propagation delay tests for subgroups 9, 10, and 11 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst delay requires recording. This may be a minimum reading, a maximum reading, or both as indicated in the table.

TABLE IV. Instruction sequence mnemonics.

SEQUENCE AC

```
[1]     CLEAR 1
[2]     LDI 0
[3]     SHL
[4]     PHI 1
[5]     PLO F
[6]     LDI FF
[7]     PLO 1
[8]     PHI F
[9]     SEX 1
[10]    SEP F
[11]    RET    MEMORY DATA: FF
[12]    INP F    I/O DATA: 55
[13]    PHI A
[14]    PLO 2
[15]    INP 9    I/O DATA: AA
[16]    PLO A
[17]    PHI 2
[18]    STR A
[19]    OUT 2    I/O DATA: FF
[20]    OUT 4    I/O DATA: 0
[21]    MARK
[22]    LDA 0    MEMORY DATA: 0
[23]    STXD
[24]    PHI 5
[25]    PLO 5
[26]    SEX 5
[27]    SEP 5       (INT)
[28]    SAV       (D/I)
[29]    SEQ
[30]    REQ
[31]    SEP 2
[32]    LBZ AA 54
[33]    LSIE    MEMORY DATA: FF FF
[34]    LBNF 0 FE
[35]    LSDF    MEMORY DATA: 0 0
[36]    SEX A
[37]    OR    MEMORY DATA: FF
[38]    STR F
[39]    LBNF FE FF
[40]    NOP    MEMORY DATA: A0
[41]    ADD    MEMORY DATA: 1
[42]    PLO 7
[43]    PHI C
[44]    ADC    MEMORY DATA: FE
[45]    PHI 7
[46]    PLO C
[47]    RET    MEMORY DATA: 77
[48]    MARK
[49]    SAV       (D/I,D/C,INT)
[50]    RET    MEMORY DATA: AA
[51]    MARK
[52]    SAV
[53]    LBNZ F0 E       (INT)
[54]    RET    MEMORY DATA: CA
[55]    ANI 55
[56]    STR 2
[57]    B1 F       (EF)
[58]    INP 0    I/O DATA: F0       (W)
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE IT

```
[1]     CLEAR 1
[2]     BN1 0        (EF)
[3]     BN1 AA        (EF)
[4]     BN2 0        (EF)
[5]     BN2 55        (EF)
[6]     BN3 0        (EF)
[7]     BN3 A5        (EF)
[8]     BN4 0        (EF)
[9]     BN4 5A        (EF)
[10]    NOP   MEMORY DATA: FF
[11]    CLEAR 1
[12]    B1 0        (EF)
[13]    B1 FF        (EF)
[14]    B2 0        (EF)
[15]    B2 F0        (EF)
[16]    B3 0        (EF)
[17]    B3 F        (EF)
[18]    B4 0        (EF)
[19]    B4 FF        (EF)
[20]    NOP   MEMORY DATA: FF
[21]    CLEAR 1
[22]    LDI 0
[23]    PHI 1
[24]    PLO 1
[25]    LDI FF
[26]    PHI 2
[27]    PLO 2        (INT)
[28]    SAV
[29]    CLEAR 1
[30]    LDI 0
[31]    PHI 1
[32]    PLO 1
[33]    LDI FF
[34]    PHI 2
[35]    PLO 2        (INT)
[36]    SAV        (INT)
[37]    RET   MEMORY DATA: 1        (INT)
[38]    SAV
[39]    CLEAR 1
[40]    LDI 0        (D/I)
[41]    PLO 1        (D/I,D/C)
[42]    PHI 1
[43]    CLEAR 1
[44]    LDI FF
[45]    PLO 1
[46]    PHI 1        (D/C)
[47]    STR 1        (D/I,D/C)
[48]    PLO 2
[49]    CLEAR 1
[50]    LDI FF        (W)
[51]    PLO 1        (W)
[52]    PHI 1
[53]    STR 1        (W)
[54]    NOP   MEMORY DATA: FF        (W)
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE MF

```
[1]     CLEAR 2
[2]     LDI 0
[3]     SHL
[4]     PHI 1
[5]     PLO F
[6]     LDI FF
[7]     PLO 1
[8]     PHI F
[9]     SEX 1
[10]    SEP F
[11]    RET    MEMORY DATA: FF
[12]    INP F    I/O DATA: 55
[13]    PHI A
[14]    PLO 2
[15]    INP 9    I/O DATA: AA
[16]    PLO A
[17]    PHI 2
[18]    STR A
[19]    OUT 2    I/O DATA: FF
[20]    OUT 4    I/O DATA: 0
[21]    MARK
[22]    LDA 0    MEMORY DATA: 0
[23]    STXD
[24]    PHI 5
[25]    PLO 5
[26]    SEX 5
[27]    SEP 5       (INT)
[28]    SAV       (D/I)
[29]    SEQ
[30]    REQ
[31]    SEP 2
[32]    LBZ AA 54
[33]    LSIE    MEMORY DATA: FF FF
[34]    LBNF 0 FE
[35]    LSDF    MEMORY DATA: 0 0
[36]    SEX A
[37]    OR    MEMORY DATA: FF
[38]    STR F
[39]    LBNF FE FF
[40]    NOP    MEMORY DATA: A0
[41]    ADD    MEMORY DATA: 1
[42]    PLO 7
[43]    PHI C
[44]    ADC    MEMORY DATA: FE
[45]    PHI 7
[46]    PLO C
[47]    RET    MEMORY DATA: 77
[48]    MARK
[49]    SAV       (D/I,D/C,INT)
[50]    RET    MEMORY DATA: AA
[51]    MARK
[52]    SAV
[53]    LBNZ F0 E       (INT)
[54]    RET    MEMORY DATA: CA
[55]    ANI 55
[56]    STR 2
[57]    B1 F       (EF)
[58]    INP D    I/O DATA: F0
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 6

[1]	CLEAR 1	
[2]	LBR 0 FF	
[3]	LBG F F	
[4]	LBNG F F	
[5]	LDI 0	
[6]	LBZ 33 33	
[7]	LBNZ 33 33	
[8]	SHR	
[9]	LBDF 55 55	
[10]	LBNF 55 55	
[11]	SEQ	
[12]	LBQ AA AA	
[13]	LBNQ AA AA	
[14]	PHI 1	
[15]	ORI FF	
[16]	PLO 1	
[17]	ADI FF	
[18]	SEP 1	
[19]	LBZ F F	
[20]	LBNZ F F	
[21]	LBDF 33 33	
[22]	LBNF 33 33	
[23]	ADI 57	
[24]	PHI 1	
[25]	BR 55	
[26]	XRI FF	
[27]	PHI 1	
[28]	BQ AA	
[29]	BNQ AA	
[30]	ORI 5F	
[31]	PLO 2	
[32]	ANI 6	
[33]	PHI 2	
[34]	SEP 2	
[35]	ORI F	
[36]	PHI 2	
[37]	BZ F	
[38]	BNZ F	
[39]	ANI 33	
[40]	XRI 30	
[41]	PHI 2	
[42]	BDF 33	
[43]	BNF 33	
[44]	ANI 33	
[45]	XRI 66	
[46]	PHI 2	
[47]	B1 55	(EF)
[48]	BN1 55	(EF)
[49]	XRI FF	
[50]	PHI 2	
[51]	B2 AA	(EF)
[52]	BN2 AA	(EF)
[53]	XRI AA	
[54]	PHI 3	
[55]	LDI FF	
[56]	PLO 3	
[57]	SEP 3	
[58]	LDI F	

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 1

```
[1]     PHI 3
[2]     B3 F        (EF)
[3]     BN3 F        (EF)
[4]     LDI 33
[5]     PHI 3
[6]     B4 33        (EF)
[7]     BN4 33        (EF)
[8]     REQ
[9]     ORI 74
[10]    ANI 05
[11]    PHI 3
[12]    BQ 55
[13]    BNQ 55
[14]    ADI 55
[15]    PHI 3
[16]    ADI 56
[17]    BZ AA
[18]    BNZ AA
[19]    PHI 4
[20]    ADI FF
[21]    PLO 4
[22]    SEP 4
[23]    ADI 10
[24]    PHI 4
[25]    ADI F0
[26]    BDF F
[27]    BNF F
[28]    ADCI 34
[29]    PHI 4
[30]    B1 33        (EF)
[31]    BN1 33        (EF)
[32]    ADCI 21
[33]    PHI 4
[34]    B2 55        (EF)
[35]    BN2 55        (EF)
[36]    ADCI 55
[37]    PHI 4
[38]    B3 AA        (EF)
[39]    BN3 AA        (EF)
[40]    SDI AA
[41]    PHI 5
[42]    SDI FF
[43]    PLO 5
[44]    SEP 5
[45]    LSDF    MEMORY DATA: 0 0
[46]    LSNF    MEMORY DATA: 0 0
[47]    LSKP    MEMORY DATA: F F
[48]    LSQ    MEMORY DATA: F0 F0
[49]    LSNQ    MEMORY DATA: FF FF
[50]    LSZ    MEMORY DATA: A A
[51]    LSNZ    MEMORY DATA: 55 55
[52]    SDI F
[53]    LSDF    MEMORY DATA: A5 5A
[54]    LSNF    MEMORY DATA: 33 55
[55]    SEQ
[56]    LSQ    MEMORY DATA: 0 F
[57]    LSNQ    MEMORY DATA: F 0
[58]    PHI 5
[59]    PLO 5
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 2

```
[1]     SDI F
[2]     LSZ    MEMORY DATA: 0 F
[3]     LSNZ   MEMORY DATA: F 0
[4]     SDI 33
[5]     PHI 5
[6]     PLC 5
[7]     SMI DE
[8]     PHI 5
[9]     BNF 55
[10]    SMI AB
[11]    PHI 5
[12]    BNF AA
[13]    SMI AA
[14]    PHI 6
[15]    SMI 1
[16]    PLC 6
[17]    SEP 6
[18]    SMI F0
[19]    PHI 6
[20]    BDF F
[21]    SMPI DC
[22]    PHI 6
[23]    BNF 33
[24]    SMBI 80
[25]    PHI 6
[26]    BNF AA
[27]    SMBI 54
[28]    PHI 6
[29]    BDF 55
[30]    SHL
[31]    SMBI AA
[32]    PLC 7
[33]    SDBI 0
[34]    PHI 7
[35]    SEP 7
[36]    LSDF   MEMORY DATA: AA 55
[37]    SDBI 10
[38]    PHI 7
[39]    BDF F
[40]    SDBI 42
[41]    PHI 7
[42]    BDF 33
[43]    SHL
[44]    SDBI 66
[45]    PLC 7
[46]    SDBI 55
[47]    PHI 7
[48]    BNF 55
[49]    SDBI 0
[50]    PHI 7
[51]    BNF AA
[52]    SMI 1
[53]    ADCI 56
[54]    PHI 8
[55]    LSDF   MEMORY DATA: A F
[56]    LDX   MEMORY DATA: FF
[57]    PLC 8
[58]    SEP 8
[59]    LDX   MEMORY DATA: F
[60]    PHI 8
[61]    PLC 8
[62]    SEX 1
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 3

```
[1]     LDX   MEMORY DATA: 33
[2]     PHI 8
[3]     PLO 8
[4]     OR   MEMORY DATA: 47
[5]     AND   MEMORY DATA: C5
[6]     PHI 8
[7]     BDF 55
[8]     OR   MEMORY DATA: AF
[9]     AND   MEMORY DATA: AA
[10]    PHI 8
[11]    SEX 2
[12]    PLO 8
[13]    OR   MEMORY DATA: 55
[14]    PLO 9
[15]    AND   MEMORY DATA: 0
[16]    PHI 9
[17]    SEP 9
[18]    XOR   MEMORY DATA: FF
[19]    SEX 3
[20]    PLO 9
[21]    SEP 9
[22]    AND   MEMORY DATA: F
[23]    PHI 9
[24]    PLO 9
[25]    AND   MEMORY DATA: FF
[26]    XOR   MEMORY DATA: 3C
[27]    SEX 4
[28]    PHI 9
[29]    BDF 33
[30]    AND   MEMORY DATA: FD
[31]    XOR   MEMORY DATA: 64
[32]    PHI 9
[33]    BDF 55
[34]    XOR   MEMORY DATA: FF
[35]    PHI 9
[36]    BDF AA
[37]    SEX 5
[38]    ADD   MEMORY DATA: 55
[39]    PLO A
[40]    LSNF   MEMORY DATA: F F
[41]    ADC   MEMORY DATA: 1
[42]    PHI A
[43]    SEP A
[44]    LSDF   MEMORY DATA: A A0
[45]    ADD   MEMORY DATA: F
[46]    SEX 6
[47]    PHI A
[48]    BNF F
[49]    ADC   MEMORY DATA: 24
[50]    PHI A
[51]    BR 33
[52]    ADC   MEMORY DATA: 22
[53]    PHI A
[54]    BNF 55
[55]    ADC   MEMORY DATA: 55
[56]    PHI A
[57]    SHL
[58]    BDF AA
[59]    SEX 7
[60]    ADC   MEMORY DATA: AB
[61]    PHI F
[62]    LSNF   MEMORY DATA: 55 AA
[63]    SM   MEMORY DATA: 1
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 4

```
[1]     PLO B
[2]     SEP B
[3]     BNF 0
[4]     SM    MEMORY DATA: F0
[5]     PHI B
[6]     LSDF    MEMORY DATA: FF 0
[7]     SEX B
[8]     SM    MEMORY DATA: CC
[9]     PHI B
[10]    BNF 33
[11]    SMB    MEMORY DATA: CC
[12]    PHI B
[13]    BNF 55
[14]    SMB    MEMORY DATA: AA
[15]    PHI B
[16]    BNF AA
[17]    SMB    MEMORY DATA: AA
[18]    PLO C
[19]    SMB    MEMORY DATA: FE
[20]    PHI C
[21]    SEX 9
[22]    SEP C
[23]    LSDF    MEMORY DATA: 0 FF
[24]    SD    MEMORY DATA: F
[25]    PHI C
[26]    BNZ F
[27]    SD    MEMORY DATA: 42
[28]    PHI C
[29]    BDF 33
[30]    SD    MEMORY DATA: CC
[31]    PHI C
[32]    BDF AA
[33]    SEX A
[34]    SD    MEMORY DATA: A9
[35]    BDF 0
[36]    SD    MEMORY DATA: 54
[37]    PHI C
[38]    BNF 55
[39]    SDB    MEMORY DATA: 55
[40]    PLO D
[41]    SDB    MEMORY DATA: 0
[42]    PHI D
[43]    SEP D
[44]    SEX B
[45]    SDB    MEMORY DATA: 10
[46]    PHI D
[47]    BDF F
[48]    SDB    MEMORY DATA: 42
[49]    PHI D
[50]    BDF 33
[51]    SDB    MEMORY DATA: 0
[52]    PLO D
[53]    BNF 33
[54]    SEX C
[55]    SDB    MEMORY DATA: 23
[56]    PHI D
[57]    BNF 55
[58]    LBR AA AA
[59]    LDX    MEMORY DATA: FF
[60]    PLO E
[61]    AND    MEMORY DATA: 0
[62]    PHI E
[63]    SEX D
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 5

```
[1]     SEP F
[2]     LBR F F
[3]     OR    MEMORY DATA: 33
[4]     PHI E
[5]     B1 33        (EF)
[6]     OR    MEMORY DATA: 44
[7]     AND    MEMORY DATA: DD
[8]     PHI E
[9]     SEX E
[10]    B2 55        (EF)
[11]    XOR    MEMORY DATA: FF
[12]    PHI E
[13]    B3 AA        (EF)
[14]    XOR    MEMORY DATA: 55
[15]    PLO F
[16]    XOR    MEMORY DATA: FF
[17]    PHI F
[18]    SEP F
[19]    SEX F
[20]    LBNF F F
[21]    ADC    MEMORY DATA: 33
[22]    PHI F
[23]    B4 33        (EF)
[24]    LBNZ 55 55
[25]    SDB    MEMORY DATA: DE
[26]    PHI F
[27]    BN1 AA        (EF)
[28]    BN2 0        (EF)
[29]    BN3 FF        (EF)
[30]    BN4 55        (EF)
[31]    LDI 1
[32]    SHR
[33]    STR 0
[34]    SHRC
[35]    STR 1
[36]    SHL
[37]    STR 2
[38]    SHLC
[39]    STR 3
[40]    SHLC
[41]    STR 4
[42]    SHL
[43]    STR 5
[44]    SHL
[45]    STR 6
[46]    SHL
[47]    STR 7
[48]    SHL
[49]    STR 8
[50]    SHL
[51]    STR 9
[52]    SHL
[53]    STR A
[54]    SHL
[55]    STR B
[56]    SHL
[57]    STR C
[58]    SHLC
[59]    STR D
[60]    ORI 1
[61]    SHR
[62]    STR E
[63]    SHR
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 6

[1]	STR F	[33]	PLO E
[2]	SHRC	[34]	LBR FF FF
[3]	STR F	[35]	DEC 0
[4]	PHI 0	[36]	STR 0
[5]	PLO 0	[37]	STR 1
[6]	PLO 1	[38]	STR 2
[7]	PHI 1	[39]	STR 3
[8]	PLO 2	[40]	STR 4
[9]	PHI 2	[41]	STR 5
[10]	PHI 3	[42]	STR 6
[11]	PLO 3	[43]	STR 7
[12]	PHI 4	[44]	STR 8
[13]	PLO 4	[45]	STR 9
[14]	PHI 5	[46]	STR A
[15]	PLO 5	[47]	STR B
[16]	PHI 6	[48]	STR C
[17]	PLO 6	[49]	STR D
[18]	PHI 7	[50]	STR E
[19]	PLO 7	[51]	INC 0
[20]	PHI 8	[52]	DEC 1
[21]	PLO 8	[53]	LBR FF FF
[22]	PHI 9	[54]	STR 1
[23]	PLO 9	[55]	STR 2
[24]	PHI A	[56]	STR 3
[25]	PLO A	[57]	STR 4
[26]	PHI B	[58]	STR 5
[27]	PLO B	[59]	STR 6
[28]	PHI C	[60]	STR 7
[29]	PLO C	[61]	STR 8
[30]	PHI D	[62]	STR 9
[31]	PLO D	[63]	STR A
[32]	PHI E		

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 7

[1]	STR B	[33]	STR C
[2]	STR C	[34]	STR D
[3]	STR D	[35]	STR E
[4]	STR E	[36]	INC 3
[5]	INC 1	[37]	DEC 4
[6]	DEC 2	[38]	LBR FF FF
[7]	LBR FF FF	[39]	STR 4
[8]	STR 2	[40]	STR 5
[9]	STR 3	[41]	STR 6
[10]	STR 4	[42]	STR 7
[11]	STR 5	[43]	STR 8
[12]	STR 6	[44]	STR 9
[13]	STR 7	[45]	STR A
[14]	STR 8	[46]	STR B
[15]	STR 9	[47]	STR C
[16]	STR A	[48]	STR D
[17]	STR B	[49]	STR E
[18]	STR C	[50]	INC 4
[19]	STR D	[51]	DEC 5
[20]	STR E	[52]	LBR FF FF
[21]	INC 2	[53]	STR 5
[22]	DEC 3	[54]	STR 6
[23]	LBR FF FF	[55]	STR 7
[24]	STR 3	[56]	STR 8
[25]	STR 4	[57]	STR 9
[26]	STR 5	[58]	STR A
[27]	STR 6	[59]	STR B
[28]	STR 7	[60]	STR C
[29]	STR 8	[61]	STR D
[30]	STR 9	[62]	STR E
[31]	STR A		
[32]	STR B		

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 8

[1]	INC 5
[2]	DEC 6
[3]	LBR FF FF
[4]	STR 6
[5]	STR 7
[6]	STR 8
[7]	STR 9
[8]	STR A
[9]	STR B
[10]	STR C
[11]	STR D
[12]	STR E
[13]	INC 6
[14]	DEC 7
[15]	LBR FF FF
[16]	STR 7
[17]	STR 8
[18]	STR 9
[19]	STR A
[20]	STR B
[21]	STR C
[22]	STR D
[23]	STR E
[24]	INC 7
[25]	DEC 8
[26]	LBR FF FF
[27]	STR 8
[28]	STR 9
[29]	STR A
[30]	STR B
[31]	STR C
[32]	STR D
[33]	STR E
[34]	STR 0
[35]	STR 1
[36]	STR 2
[37]	STR 3
[38]	STR 4
[39]	STR 5
[40]	STR 6
[41]	STR 7
[42]	INC 8
[43]	DEC 9
[44]	LBR FF FF
[45]	STR 9
[46]	STR A
[47]	STR B
[48]	STR C
[49]	STR D
[50]	STR E
[51]	INC 9
[52]	DEC A
[53]	LBR FF FF
[54]	STR A
[55]	STR B
[56]	STR C
[57]	STR D
[58]	STR E
[59]	INC A
[60]	DEC B
[61]	LBR FF FF

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE 9

```
[1]     STR B
[2]     STR C
[3]     STR D
[4]     STR E
[5]     INC B
[6]     DEC C
[7]     LBR FF FF
[8]     STR C
[9]     STR D
[10]    STR F
[11]    INC C
[12]    DEC D
[13]    LBR FF FF
[14]    STR D
[15]    STR E
[16]    INC D
[17]    DEC E
[18]    LBR FF FF
[19]    STR E
[20]    INC E
[21]    LBR FF FF
[22]    STR 0
[23]    STR 1
[24]    STR 2
[25]    STR 3
[26]    STR 4
[27]    STR 5
[28]    STR 6
[29]    STR 7
[30]    STR 8
[31]    STR 9
[32]    STR A
[33]    STR B
[34]    STR C
[35]    STR D
[36]    STR E
[37]    SEX 5
[38]    LDN F     MEMORY DATA: 5A
[39]    STXD
[40]    LDN 5     MEMORY DATA: A5
[41]    STXD
[42]    SEX 0
[43]    STXD
[44]    LDXA      MEMORY DATA: FF
[45]    SEP 0
[46]    STR F
[47]    SEX A
[48]    LDXA      MEMORY DATA: 0
[49]    STXD
[50]    SEP A
[51]    IRX
[52]    SEX 5
[53]    IRX
[54]    STR 5
[55]    LDA 2     MEMORY DATA: 69
[56]    STR 2
[57]    LDA D     MEMORY DATA: 96
[58]    STR D
[59]    SEP 5
[60]    OUT 1     I/O DATA: FF
[61]    OUT 2     I/O DATA: AA
[62]    OUT 3     I/O DATA: 55
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE A

[1]	SEX F	
[2]	OUT 4	I/C DATA: 12
[3]	OUT 5	I/C DATA: 34
[4]	OUT 6	I/C DATA: 56
[5]	OUT 7	I/C DATA: 78
[6]	INP 9	I/C DATA: EE
[7]	PLC F	
[8]	INP A	I/C DATA: CC
[9]	PHI F	
[10]	INP B	I/C DATA: CC
[11]	PLC F	
[12]	INP C	I/C DATA: BF
[13]	PHI 3	
[14]	SEX 3	
[15]	INP D	I/C DATA: AA
[16]	PLC 3	
[17]	INP E	I/C DATA: 98
[18]	PHI 3	
[19]	INP F	I/C DATA: 76
[20]	PLC 1	
[21]	SEP 1	
[22]	SEX 0	
[23]	MARK	
[24]	SAV	
[25]	SEP 0	
[26]	MARK	
[27]	SAV	
[28]	SEP 2	
[29]	MARK	
[30]	SAV	
[31]	SEP 0	
[32]	MARK	
[33]	SAV	
[34]	SEP 4	
[35]	MARK	
[36]	SAV	
[37]	SEP 0	
[38]	MARK	
[39]	SAV	
[40]	SEP 8	
[41]	MARK	
[42]	SAV	
[43]	SEP 0	
[44]	MARK	
[45]	SAV	
[46]	GHI 0	
[47]	PLO 0	
[48]	GLO 0	
[49]	PHI 0	
[50]	GHI F	
[51]	PLO 0	
[52]	GLO F	
[53]	PHI 0	
[54]	LSIE	MEMORY DATA: F0 F
[55]	DIS	MEMORY DATA: 2F
[56]	LSIE	MEMORY DATA: F F
[57]	NOP	MEMORY DATA: AA
[58]	RET	MEMORY DATA: E
[59]	LSIE	MEMORY DATA: AA 55
[60]	NOP	MEMORY DATA: 66
[61]	STR 0	
[62]	STR 2	

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE B

```
[1]   SKP    MEMORY DATA: FF        (W,D/I,INT)
[2]   DIS    MEMORY DATA: 7E        (INT)
[3]   LDI FF        (W,D/I,D/C)
[4]   PHI 0        (W,D/C,INT)
[5]   PLO 0        (W)
[6]   SEQ
[7]   LSIE    MEMORY DATA: FF 0        (W,D/D,INT)
[8]   INC 0
[9]   CLEAR 1
[10]  LSIE    MEMORY DATA: A5 5A
[11]  LSQ    MEMORY DATA: 66 66        (D/I,D/C)
[12]  LDX    MEMORY DATA: FF        (W)
[13]  LDI 11
[14]  PHI E        (D/D)
[15]  PLO F        (D/I,D/C,INT)
[16]  SEP F
[17]  PHI 1
[18]  PLO 1
[19]  LDI 22
[20]  PHI 2
[21]  PLO 2
[22]  SEX F
[23]  MARK        (W,D/I)
[24]  SEX F
[25]  DIS    MEMORY DATA: FE        (INT)
[26]  NOP    MEMORY DATA: 99        (INT)
[27]  LSIE    MEMORY DATA: 12 12        (INT)
[28]  IDL    MEMORY DATA: 34        (W,D/C,INT)
[29]  RET    MEMORY DATA: 34        (W,INT)
[30]  LSIE    MEMORY DATA: 56 78
[31]  SAV        (INT)
[32]  MARK        (D/I)
[33]  LDI 0
[34]  PHI 3
[35]  PLO 3
[36]  SEP 3
[37]  SEX 2
[38]  RET    MEMORY DATA: 23
[39]  INC 1        (INT)
[40]  LSIE    MEMORY DATA: AB CC
[41]  MARK
[42]  RET    MEMORY DATA: FE
[43]  IDL    MEMORY DATA: 0        (INT)
[44]  SEQ        (INT)
[45]  LBR 12 34
[46]  CLEAR 2        (INT)
[47]  DIS    MEMORY DATA: 0        (INT)
[48]  LSIE    MEMORY DATA: 63 59        (INT)
[49]  RET    MEMORY DATA: 0        (INT)
[50]  NOP    MEMORY DATA: F        (W,D/I,D/D,INT)
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

SEQUENCE C

```
[1]   LSIE   MEMORY DATA: 12 34
[2]   LDI 33
[3]   PHI F
[4]   PLO F
[5]   SEP F
[6]   LDI 44
[7]   PHI 1
[8]   PLO 1
[9]   LDI FF
[10]  PHI 0
[11]  PLO 0
[12]  SEX A
[13]  IDL    MEMORY DATA: 0       (D/I,D/C,INT)
[14]  LDI FF
[15]  PHI 2
[16]  PLO 2
[17]  RET    MEMORY DATA: AF
[18]  LBR FF A0       (INT)
[19]  RET    MEMORY DATA: AF
[20]  STR A       (INT)
[21]  IDL    MEMORY DATA: 0       (W,D/I,D/O)
[22]  NOP    MEMORY DATA: F
[23]  SEQ
[24]  LSQ    MEMORY DATA: 43 21
[25]  LDI 0
[26]  SHR
[27]  BNZ AA
[28]  LDI 1
[29]  BNZ 3F
[30]  SHL
[31]  BNZ 2
[32]  SHL
[33]  BNZ 3
[34]  DEC 1
[35]  SHL
[36]  BNZ 7
[37]  DEC 1
[38]  SHL
[39]  BNZ F
[40]  DEC 1
[41]  SHL
[42]  BNZ 1F
[43]  DEC 1
[44]  SHL
[45]  BNZ 3F
[46]  DEC 1
[47]  SHL
[48]  BNZ 7F
[49]  DEC 1
[50]  GHI F
[51]  STR F
```

See footnotes at end of table.

TABLE IV. Instruction sequence mnemonics - Continued.

FOOTNOTES (for all sequences):

1/ Expressions in parentheses indicate that signals shall be applied to inputs as follows:

D/I = DMA-IN
D/O = DMA-OUT
EF = EF1, EF2, EF3, or EF4
INT = INTERRUPT
W = WAIT

The clock cycle at which the signal is applied is indicated in the vectors of table V.

2/ The instruction "CLEAR" followed by a number indicates application of that number of pulses to the $\overline{\text{CLEAR}}$ input. All other instructions are mnemonics as listed in table VI.

TABLE V. Functional vector patterns.

Table VI, not printed herein, is a computer-generated listing for use with table III. Each vector identifies activity states by pin number. See Section 6 for information on obtaining the complete table in compatible output format.

NOTES:

1. The vectors are divided into patterns or sequences, each corresponding to one of the instruction sequences of table V. The main functional test consists of 13 sequences designated by single digits or letters from 0 through C. There are also 3 special sequences with two-letter designations. The vectors of each pattern are numbered separately, starting with vector 1. The number of vectors in each pattern are as follows:

Sequence	No. of vectors in pattern	Sequence	No. of vectors in pattern
AC	1032	5	1032
IT	919	6	1024
MF	1032	7	1024
0	1025	8	1024
1	1032	9	1024
2	1024	A	1032
3	1032	B	1031
4	1032	C	978

Sequences AC, IT, and MF are independent and shall be used for the applicable tests of subgroups 7 through 11 as specified in table III. Sequences 0 through C shall be run consecutively in the order listed above; between sequences, the specified voltages shall continue to be applied to V_{CC}, V_{DD}, and V_{SS}, and the clock shall be stopped.

2. Sequence IT consists of a series of independent sets of vectors. The following is a correlation of the vectors with the instruction sequence of table V:

Vectors	Instructions	Vectors	Instructions
1-161	1-10	621-701	39-42
162-322	11-20	702-814	43-48
323-451	21-28	815-919	49-54
452-620	29-38		

TABLE VI. Microprocessor instruction set.

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
MEMORY REFERENCE			
LOAD VIA N	LDN	0N	M(R(N))→D; FOR N NOT 0
LOAD ADVANCE	LDA	4N	M(R(N))→D; R(N) +1
LOAD VIA X	LDX	F0	M(R(X))→D
LOAD VIA X AND ADVANCE	LDXA	72	M(R(X))→D; R(X) +1
LOAD IMMEDIATE	LDI	F8	M(R(P))→D; R(P) +1
STORE VIA N	STR	5N	D→M(R(N))
STORE VIA X AND DECREMENT	STXD	73	D→M(R(X)); R(X) −1
REGISTER OPERATIONS			
INCREMENT REG N	INC	1N	R(N) +1
DECREMENT REG N	DEC	2N	R(N) −1
INCREMENT REG X	IRX	60	R(X) +1
GET LOW REG N	GLO	8N	R(N).0→D
PUT LOW REG N	PLO	AN	D→R(N).0
GET HIGH REG N	GHI	9N	R(N).1→D
PUT HIGH REG N	PHI	BN	D→R(N).1
LOGIC OPERATIONS♦♦			
OR	OR	F1	M(R(X)) OR D→D
OR IMMEDIATE	ORI	F9	M(R(P)) OR D→D; R(P) +1
EXCLUSIVE OR	XOR	F3	M(R(X)) XOR D→D
EXCLUSIVE OR IMMEDIATE	XRI	FB	M(R(P)) XOR D→D; R(P) +1
AND	AND	F2	M(R(X)) AND D→D
AND IMMEDIATE	ANI	FA	M(R(P)) AND D→D; R(P) +1
SHIFT RIGHT	SHR	F6	SHIFT D RIGHT, LSB(D)→DF, 0→MSB(D)
SHIFT RIGHT WITH CARRY	SHRC	76♦	SHIFT D RIGHT, LSB(D)→DF, DF→MSB(D)
RING SHIFT RIGHT	RSHR		
SHIFT LEFT	SHL	FE	SHIFT D LEFT, MSB(D)→DF, 0→LSB(D)
SHIFT LEFT WITH CARRY	SHLC	7E♦	SHIFT D LEFT, MSB(D)→DF, DF→LSB(D)
RING SHIFT LEFT	RSHL		
ARITHMETIC OPERATIONS♦♦			
ADD	ADD	F4	M(R(X)) +D→DF, D
ADD IMMEDIATE	ADI	FC	M(R(P)) +D→DF, D; R(P) +1
ADD WITH CARRY	ADC	74	M(R(X)) +D +DF→DF, D
ADD WITH CARRY, IMMEDIATE	ADCI	7C	M(R(P)) +D +DF→DF, D R(P) +1
SUBTRACT D	SD	F5	M(R(X))−D→DF, D
SUBTRACT D IMMEDIATE	SDI	FD	M(R(P))−D→DF, D; R(P) +1
SUBTRACT D WITH BORROW	SDB	75	M(R(X))−D−(NOT DF)→DF, D
SUBTRACT D WITH BORROW, IMMEDIATE	SDBI	7D	M(R(P))−D−(NOT DF)→DF, D; R(P) +1
SUBTRACT MEMORY	SM	F7	D−M(R(X))→DF, D
SUBTRACT MEMORY IMMEDIATE	SMI	FF	D−M(R(P))→DF, D; R(P) +1
SUBTRACT MEMORY WITH BORROW	SMB	77	D−M(R(X))−(NOT DF)→DF, D
SUBTRACT MEMORY WITH BORROW, IMMEDIATE	SMBI	7F	D−M(R(P))−(NOT DF)→DF, D R(P) +1

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
BRANCH INSTRUCTIONS–SHORT BRANCH			
SHORT BRANCH	BR	30	M(R(P))→R(P).0
NO SHORT BRANCH (SEE SKP)	NBR	38♦	R(P) +1
SHORT BRANCH IF D=0	BZ	32	IF D=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF D NOT 0	BNZ	3A	IF D NOT 0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF DF=1	BDF	33♦	IF DF=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF POS OR ZERO	BPZ		
SHORT BRANCH IF EQUAL OR GREATER	BGE		
SHORT BRANCH IF DF=0	BNF	3B♦	IF DF=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF MINUS	BM		
SHORT BRANCH IF LESS	BL		
SHORT BRANCH IF Q=1	BQ	31	IF Q=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF Q=0	BNQ	39	IF Q=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=1	B1	34	IF EF1=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF1=0	BN1	3C	IF EF1=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=1	B2	35	IF EF2=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF2=0	BN2	3D	IF EF2=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=1	B3	36	IF EF3=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF3=0	BN3	3E	IF EF3=0, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=1	B4	37	IF EF4=1, M(R(P))→R(P).0 ELSE R(P) +1
SHORT BRANCH IF EF4=0	BN4	3F	IF EF4=0, M(R(P))→R(P).0 ELSE R(P) +1
BRANCH INSTRUCTIONS–LONG BRANCH			
LONG BRANCH	LBR	C0	M(R(P))→R(P).1 M(R(P) +1)→R(P).0
NO LONG BRANCH (SEE LSKP)	NLBR	C8♦	R(P) +2
LONG BRANCH IF D=0	LBZ	C2	IF D=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF D NOT 0	LBNZ	CA	IF D NOT 0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=1	LBDF	C3	IF DF=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF DF=0	LBNF	C8	IF DF=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=1	LBQ	C1	IF Q=1, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2
LONG BRANCH IF Q=0	LBNQ	C9	IF Q=0, M(R(P))→R(P).1 M(R(P) +1)→R(P).0 ELSE R(P) +2

TABLE VII. Microprocessor instruction set - Continued.

INSTRUCTION	MNEMONIC	OP CODE	OPERATION
SKIP INSTRUCTIONS			
SHORT SKIP (SEE NBR)	SKP	38♦	R(P) +1
LONG SKIP (SEE NLBR)	LSKP	C8♦	R(P) +2
LONG SKIP IF D=0	LSZ	CE	IF D=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF D NOT 0	LSNZ	C6	IF D NOT 0, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=1	LSDF	CF	IF DF=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF DF=0	LSNF	C7	IF DF=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=1	LSQ	CD	IF Q=1, R(P) +2 ELSE CONTINUE
LONG SKIP IF Q=0	LSNQ	C5	IF Q=0, R(P) +2 ELSE CONTINUE
LONG SKIP IF IE=1	LSIE	CC	IF IE=1, R(P) +2 ELSE CONTINUE
CONTROL INSTRUCTIONS			
IDLE	IDL	00#	WAIT FOR DMA OR INTERRUPT, M(R(0))→BUS
NO OPERATION	NOP	C4	CONTINUE
SET P	SEP	DN	N→P
SET X	SEX	EN	N→X
SET Q	SEQ	7B	1→Q
RESET Q	REQ	7A	0→Q
SAVE	SAV	78	T→M(R(X))
PUSH X,P TO STACK	MARK	79	(X,P)→T; (X,P)→M(R(2)) THEN P→X; R(2)−1
RETURN	RET	70	M(R(X))→(X,P); R(X) +1 1→IE
DISABLE	DIS	71	M(R(X))→(X,P); R(X) +1 0→IE
INPUT–OUTPUT BYTE TRANSFER			
OUTPUT 1	OUT 1	61	M(R(X))→BUS; R(X) +1; N LINES = 1
OUTPUT 2	OUT 2	62	M(R(X))→BUS; R(X) +1; N LINES = 2
OUTPUT 3	OUT 3	63	M(R(X))→BUS; R(X) +1; N LINES = 3
OUTPUT 4	OUT 4	64	M(R(X))→BUS; R(X) +1; N LINES = 4
OUTPUT 5	OUT 5	65	M(R(X))→BUS; R(X) +1; N LINES = 5
OUTPUT 6	OUT 6	66	M(R(X))→BUS; R(X) +1; N LINES = 6
OUTPUT 7	OUT 7	67	M(R(X))→BUS; R(X) +1; N LINES = 7
INPUT 1	INP 1	69	BUS→M(R(X)); BUS→D; N LINES = 1
INPUT 2	INP 2	6A	BUS→M(R(X)); BUS→D; N LINES = 2
INPUT 3	INP 3	6B	BUS→M(R(X)); BUS→D; N LINES = 3
INPUT 4	INP 4	6C	BUS→M(R(X)); BUS→D; N LINES = 4
INPUT 5	INP 5	6D	BUS→M(R(X)); BUS→D; N LINES = 5
INPUT 6	INP 6	6E	BUS→M(R(X)); BUS→D; N LINES = 6
INPUT 7	INP 7	6F	BUS→M(R(X)); BUS→D; N LINES = 7

NOTES: All instructions require two machine cycles (1 Fetch & 1 Execute) except Long Branches and Long Skips which require three machine cycles (1 Fetch & 2 Execute). NOP is considered a Long Skip. Each machine cycle = 8 external clocks, i.e. @6.4 MHz cycle = 1.25 μsec.

All instructions require 1 byte of memory except Short Branches (2 bytes). Immediate Operations (2 bytes) and Long Branches (3 bytes).

♦ NOTE: This instruction is associated with more than one mnemonic. Each mnemonic is individually listed.

♦♦ NOTE: The arithmetic operations and the shift instructions are the only instructions that can alter the DF.
After an add instruction:
DF = 1 denotes a carry has occurred.
DF = 0 denotes a carry has not occurred.
After a subtract instruction:
DF = 1 denotes no borrow. D is a positive number.
DF = 0 denotes a borrow. D is two's complement.
The syntax "-(not DF)" denotes the subtraction of the borrow.

#An idle instruction initiates a repeating S1 cycle. The processor will continue to idle until an I/O request (INTERRUPT, DMA-IN, or DMA-OUT) is activated When the request is acknowledged, the IDLE cycle is terminated and the I/O request is serviced, and then normal operation is resumed.

c. V_{ZAP} is applied to the DUT in the four modes (see figure 5) for group 1 and 2 terminals, using XTAL (pin 39) for group 1 and SC1 (pin 5) for group 2 as the associated outputs. For group 3 and 4 terminals, V_{ZAP} is applied only in modes 1 and 2. In all cases, V_{ZAP} is applied by charging C1 to V_{ZAP} with S1 in position 1 and then switching to position 2.

d. Within 24 hours, repeat the I_{SS} measurement and the I_{IH} and I_{IL} measurements on the same four terminals as performed above. If a DUT exhibits leakage currents in excess of the specified limits at this time, it is defective.

4.5.4 Quiescent supply current (I_{SS}) test. When performing quiescent supply current measurements (I_{SS}), the meter shall be placed so that all currents flow through the meter, as shown on figure 6(a).

4.6 Data reporting. When specified in the contract or purchase order, a copy of the following data, as applicable, shall be supplied:

a. Attributes data for all screening tests (see 4.2) and variables data for all dynamic burn-in, and steady-state life tests (see 3.5).

b. The quality conformance inspection data (see 4.4).

c. Final electrical parameters data (see 4.2c.).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. These devices require electrostatic protection.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Test vector table. Table IV which forms a part of this specification, is not printed herein because of its extreme length; and, even when presented as hard copy, it requires conversion to on-line format. When the sequence of vector groups is needed for testing devices as part of inspection, it should be obtained in a form compatible with test system architecture (magnetic tape format usually preferred). The preparing activity (or Defense Electronics Supply Center, as its agent) may be consulted for information on obtaining the complete table in compatible output format.

6.3 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.4 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the data (see 4.6) pertinent to the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein (including terms and symbols for device terminals) are defined in MIL-M-38510, MIL-STD-1331, and as follows:

Data bus (BUS 0 to BUS 7). The eight bidirectional data bus lines are used for transferring data between the memory, the microprocessor and I/O devices.

I/O lines (N0 to N2). These lines are activated by an I/O instruction to signal the I/O control logic of a data transfer between memory and I/O interface. These lines can be used to issue command codes for device selection codes to the I/O devices (independently or combined with the memory byte on the data bus when an I/O instruction is being executed). The N bits are low at all times except when an I/O instruction is being executed. During this time their state is the same as the corresponding bits in the N register. The direction of data flow is defined in the I/O instruction by bit N3 (internally) and is indicated by the level of the MRD signal.

$\overline{MRD}$ = V_{CC}: Data from I/O to CPU and memory.

$\overline{MRD}$ = V_{SS}: Data from memory to I/O.

Flags ($\overline{EF1}$ to $\overline{EF4}$). These inputs enable the I/O controllers to transfer status information to the processor. The levels can be tested by the conditional branch instructions. They can be used in conjunction with the INTERRUPT request line to establish interrupt priorities. These flags can also be used by I/O devices to "Call the attention" of the processor, in which case the program must routinely test the status of these flag(s). The flag(s) are sampled at the beginning of every S1 cycle.

I/O requests ($\overline{INTERRUPT}$, $\overline{DMA\text{-}IN}$, $\overline{DMA\text{-}OUT}$). These inputs are sampled by the microprocessor at the falling edge of clock pulse 7 in the S1, S2, and S3 states.

Interrupt action: X and P are stored in T after executing current instruction; designator X is set to 2; designator P is set to 1; interrupt enable is reset to 0 (inhibit); and instruction execution is resumed. The interrupt action requires one machine cycle (S3).

DMA action: Finish executing current instruction; R(0) points to memory area for data transfer; data is loaded into or read out of memory; and increment R(0).

NOTE: In the event of concurrent DMA and INTERRUPT requests, DMA-IN has priority followed by DMA-OUT and then INTERRUPT.

State code lines (SC0, SC1). These outputs indicate that the CPU is: (1) fetching an instruction, or (2) executing an instruction, or (3) processing a DMA request, or (4) acknowledging an INTERRUPT request. The levels of state code are tabulated below. All tates are valid at TPA INTERRUPT request. The levels of state code are tabulated below. All states are valid at TPA

H = V_{CC}, L = V_{SS}.

State type	State code lines	
	SC1	SC0
S0 (Fetch)	L	L
S1 (Execute)	L	H
S2 (DMA)	H	L
S3 (Interrupt)	H	H

Timing pulses (TPA, TPB). These outputs are positive pulses that occur once in each machine cycle (TPB follows TPA). They are used by I/O controllers to interpret codes and to time interaction with the data bus. The trailing edge of TPA is used by the memory system to latch the higher-order byte of the 16-bit memory address. Operation near the maximum frequency may require external delay of the TPA pulse for proper operation. TPA is suppressed in IDLE when the CPU is in the load mode.

Memory address lines (MA0 to MA7). The higher-order byte of a 16-bit memory address appears on the memory address lines MA0-7 first. Those bits required by the memory system may be strobed into external address latches by timing pulse TPA. The low-order byte of the 16-bit address appears on the address lines after the termination of TPA. Latching of all eight higher-order address bits would permit a memory system of 64K bytes.

Write pulse ($\overline{MWR}$). This output is a negative pulse appearing in a memory-write cycle, after the address lines have stabilized.

Read level ($\overline{MRD}$). A low level on $\overline{MRD}$ indicates a memory read cycle. It can be used to control three-state outputs from the addressed memory which may have a common data input and output bus. If a memory does not have a three-state high-impedance output, MRD is useful for driving memory/bus separator gates. It is also used to indicate the direction of data transfer during an I/O instruction.

Q output (Q). This is a single bit output from the CPU which can be set or reset under program control. During SEQ or REQ instruction execution, Q is set or reset between the trailing edge of TPA and the leading edge of TPB.

Clock input (CLOCK). This is an input for an externally generated single-phase clock. See 1.2.5.1 for recommended clock frequencies. The clock is counted down internally at 8 clock pulses per machine cycle.

Crystal ($\overline{XTAL}$). This connection is used with the clock input terminal, for an external crystal, if the on-chip oscillator is utilized. The crystal is connected between terminals 1 and 39 (CLOCK and XTAL) in parallel with a resistance (10 megohms typical). Frequency trimming capacitors may be required at terminals 1 and 39. Recommended crystal characteristics are as follows:

Resonance - - - - - - - - - - -	Parallel
Cut - - - - - - - - - - - - - - -	AT
Load capacitance- - - - - - -	15 pF
Q - - - - - - - - - - - - - - - -	50 K minimum

Control lines ($\overline{WAIT}$, $\overline{CLEAR}$). These input lines provide four control modes as listed in the following truth table:

$\overline{CLEAR}$	$\overline{WAIT}$	MODE
L	L	Load
L	H	Reset
H	L	Pause
H	H	Run

The function of the modes are defined as follows:

Load: Holds the CPU in the IDLE execution state and allows an I/O device to load the memory without the need for a "bootstrap" loader. It modifies the IDLE condition so that DMA-IN operation does not force execution of the next instruction.

Reset: Registers I, N, Q are reset, IE is set and 0's (V_{SS}) are placed on the data bus. TPA and TPB are suppressed while reset is held and the CPU is placed in S1. The first machine cycle after termination of reset is an initialization cycle which requires 9 clock pulses. During this cycle the CPU remains in S1 and registers X, P, and R(0) are reset. INTERRUPT and DMA servicing are suppressed during the initialization cyle.

The next cycle is an S0, S1, or an S2 but never an S3. With the use of a 71 instruction followed by 00 at memory locations 0000 and 0001, this feature may be used to reset IE, so as to preclude INTERRUPTS until ready for them. Power-up reset can be realized by connecting a buffered RC network to CLEAR.

Pause: Stops the internal CPU timing generator on the first negative high-to-low transition of the input clock. The oscillator continues to operate, but subsequent clock transitions are ignored.

Run: May be initiated from the pause or reset mode functions. If initiated from pause, the CPU resumes operation on the first negative high-to-low transition of the input clock. When initiated from the reset operation, the first machine cycle following reset is always the initialization cycle. The initialization cycle is then followed by a DMA (S2) cycle or fetch (S0) from location 0000 in memory.

Power supply inputs (V_{DD}, V_{SS}, V_{CC}). The internal voltage supply V_{DD} is isolated from the input/output voltage supply V_{CC} so that the processor may operate at maximum speed while interfacing with various external circuit technologies, including T^2L at 5 volts. V_{CC} must be less than or equal to V_{DD}. All outputs swing from V_{SS} to V_{CC}. The recommended input voltage swing is V_{SS} to V_{CC}.

6.6 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D (see 4.4.3) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	1802D

6.8 Handling. CMOS microcircuits should be handled with certain precautions to avoid damage due to accumulation of static charge. These CMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment, tools, and personnel.

c. Do not handle devices by the leads.

d. Store devices in conductive carriers or conductive foam.

e. Avoid use of plastic, rubber, or silk in areas where CMOS devices are handled.

f. Maintain relative humidity above 50 percent.

6.10 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.11 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodian:
NASA - NA

Preparing activity:
NASA - NA

(Project 5962-K646)

Review activity:
DLA - ES

Agent:
DLA - ES