| QUALIFICATION |
| REQUIREMENTS |
| REMOVED |

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, FOUR-BIT MICROPROCESSOR SLICE

MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

MIL-M-38510/440 (2901A) and MIL-M-38510/440A (2901B) have been replaced with MIL-M-38510/440C (2901C). The new revision of this device is not totally compatible with previous revisions or versions. DO NOT REPLACE previous revisions of this device without first determining electrical compatibility. It should be noted that previous versions of the 2901 are no longer being manufactured.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic, silicon, TTL compatible four-bit microprocessor slice (see 6.7). Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, with the exception that the "JAN" or "J" certification shall not be used.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	Four-bit microprocessor slice

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
Q	D-5 (40-lead 0.6" x 2.06"), dual-in-line package
Z	See figure 1 (42-lead 0.62" x 1.06"), flat package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc at -12 mA to +5.5 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	1.6 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	0.03°C/mW
Case Z	0.04°C/mW
Junction temperature (T_J) 2/	+175°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
2/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5004 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
Minimum high-level input voltage (V_{IH})	2.0 V dc
Maximum low-level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outline. The case outline shall be as specified in 1.2.3.

3.2.2 Terminal connections and pin designations. The terminal connections and pin designations shall be as specified on figure 2.

3.2.3 Logic block diagram. The logic block diagram shall be as specified on figure 3.

3.2.4 Truth tables and logic equations. The truth tables and logic equations shall be as specified on figure 4.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$			Limits		Unit
					Min	Max	
High level output voltage	V_{OH1}	V_{CC} = 4.5 V V_{IN} = 2.0 V, 0.8 V		I_{OH} = -1.6 mA Y_0, Y_1, Y_2, Y_3	2.4	4.2	V
	V_{OH3}			I_{OH} = -1.0 mA, C_{n+4}	2.4	4.2	
	V_{OH2}			I_{OH} = -800 µA, OVR, $\overline{P}$	2.4	4.2	
	V_{OH4}			I_{OH} = -600 µA, F_3	2.4	4.2	
	V_{OH4}			I_{OH} = -600 µA $RAM_{0,3}$, $Q_{0,3}$	2.4	4.2	
	V_{OH1}			I_{OH} = -1.6 mA, $\overline{G}$	2.4	4.2	
Output leakage current for F = 0 output	I_{CEX}	V_{CC} = 4.5 V, V_{OH} = 5.5 V, V_{IN} = 2.0 V, 0.8 V			-40	250	µA
Low level output voltage	V_{OL1}	V_{CC} = 4.5 V V_{IN} = 2.0 V, 0.8 V	F = 0	I_{OL} = 16 mA	0	0.5	V
	V_{OL1}		Y_0, Y_1, Y_2, Y_3	I_{OL} = 16 mA	0	0.5	
	V_{OL1}		$\overline{G}$	I_{OL} = 16 mA	0	0.5	
	V_{OL3}		C_{n+4}	I_{OL} = 10 mA,	0	0.5	
	V_{OL2}		OVR, $\overline{P}$	I_{OL} = 8.0 mA	0	0.5	
	V_{OL4}		F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0 mA	0	0.5	
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V I_{IN} = -18 mA			-0.4	-1.5	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$			Limits Min	Limits Max	Unit
Low level input current	I_{IL1}	V_{CC} = 5.5 V, V_{IN} = 0.5 V		Clock, $\overline{OE}$	+0.02	-0.36	mA
	I_{IL2}			A_0, A_1, A_2, A_3, Clock	+0.02	-0.36	
				B_0, B_1, B_2, B_3	+0.02	-0.36	
	I_{IL3}			D_0, D_1, D_2, D_3	+0.05	-0.72	
	I_{IL1}			I_0, I_1, I_2, I_6, I_8	+0.02	-0.36	
	I_{IL4}			I_3, I_4, I_5, I_7	+0.05	-0.72	
	I_{IL5}			$RAM_{0,3}, Q_{0,3}$ 1/	+0.05	-0.8	
	I_{IL6}			C_n	+0.05	-3.6	
High level input current	I_{IH1}	V_{CC} = 5.5 V, V_{IN} = 2.7 V		Clock, $\overline{OE}$	-10	20	µA
				A_0, A_1, A_2, A_3	-10	20	
				B_0, B_1, B_2, B_3	-10	20	
	I_{IH2}			D_0, D_1, D_2, D_3	-10	40	
	I_{IH1}			I_0, I_1, I_2, I_6, I_8	-10	20	
	I_{IH2}			I_3, I_4, I_5, I_7	-10	40	
	I_{IH3}			$RAM_{0,3}, Q_{0,3}$ 1/	-10	100	
	I_{IH4}			C_n	-40	200	
High impedance state output current	I_{ZH1}	V_{CC} = 5.5 V	Y_0, Y_1, Y_2, Y_3	V_O = 2.4 V	-50	50	µA
	I_{ZL1}			V_O = 0.5 V	+50	-50	
	I_{ZH2}		$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4 V	-40	100	
	I_{ZL2}			V_O = 0.5 V	20	-800	
Output short circuit current 2/	I_{OS}	V_{CC} = 5.5 V, V_O = 0 V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	-30	-85	mA
				C_{n+4}	-30	-85	
				OVR, $\overline{P}$	-30	-85	
				F_3	-30	-85	
				$RAM_{0,3}, Q_{0,3}$	-30	-85	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits		Unit
			Min	Max	
Power supply current	I_{CC}	V_{CC} = 5.5 V	100	280	mA
A_3-A_0 setup time to positive edge of clock	t_{SHL1}	C_L = 50 ±5 pF all outputs	35		ns
	t_{SLH1}		35		ns
A_3-A_0 setup time to negative edge of clock	t_{SHL2}		20		ns
	t_{SLH2}		20		ns
B_3-B_0 (source) setup time to positive edge of clock	t_{SHL3}		35		ns
	t_{SLH3}		35		ns
B_3-B_0 (source) setup time to negative edge of clock	t_{SHL4}		20		ns
	t_{SLH4}		20		ns
B_3-B_0 (DEST) setup time to negative edge of clock	t_{SHL5}		18		ns
	t_{SLH5}		18		ns
D_3-D_0 (arithmetic mode) setup time to positive edge of clock	t_{SHL6}		30		ns
	t_{SLH6}		30		ns
D_3-D_0 (I = X37) setup time to positive edge of clock	t_{SHL7}		30		ns
	t_{SLH7}		30		ns
C_n setup time to positive edge of clock	t_{SHL8}		25		ns
	t_{SLH8}		25		ns
I_2-I_0 setup time to positive edge of clock	t_{SHL9}		35		ns
	t_{SLH9}		35		ns
I_5-I_3 setup time to positive edge of clock	t_{SHL10}		35		ns
	t_{SLH10}		35		ns
I_8-I_6 setup time to negative edge of clock	t_{SHL11}		15		ns
	t_{SLH11}		15		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits Min	Limits Max	Unit
Q_3,Q_0 setup time to positive edge of clock	t_{SHL12}	C_L = 50 ±5 pF all outputs	17		ns
	t_{SLH12}		17		ns
RAM_3, RAM_0 setup time to positive edge of clock	t_{SHL13}		17		ns
	t_{SLH13}		17		ns
A_3-A_0 hold time from positive edge of clock	t_{HHL1}		4		ns
	t_{HLH1}		4		ns
B_3-B_0 hold time from positive edge of clock	t_{HHL2}		4		ns
	t_{HLH2}		4		ns
D_3-D_0 hold time from positive edge of clock	t_{HHL3}		2		ns
	t_{HLH3}		2		ns
C_n hold time from positive edge of clock	t_{HHL4}		2		ns
	t_{HLH4}		2		ns
I_8-I_0 hold time from positive edge of clock	t_{HHL5}		2		ns
	t_{HLH5}		2		ns
Q_3,Q_0 hold time from positive edge of clock	t_{HHL6}		4		ns
	t_{HLH6}		4		ns
RAM_3,RAM_0 hold time from positive edge of clock	t_{HHL7}		4		ns
	t_{HLH7}		4		ns
Delay from A_3-A_0 to Y_3-Y_0	t_{PHL1}	R_L = 68Ω R = 1.5 kΩ Y_3-Y_0, $\overline{G}$ C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH1}			53	ns
Delay from A_3-A_0 to F_3	t_{PHL2}	R_L = 110Ω R = 2.4 kΩ C_{n+4} C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH2}			53	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits Min	Limits Max	Unit
Delay from A_3-A_0 to C_{n+4}	t_{PHL3}	R_L = 140Ω R = 3.0 kΩ OVR, $\overline{P}$ C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH3}			53	ns
Delay from A_3-A_0 to $\overline{G}$ and $\overline{P}$	t_{PHL4}	R_L = 190Ω R_1 = 4.0 kΩ F_3 C_L = 50 ±5 pF all outputs		49	ns
	t_{PLH4}			49	ns
Delay from A_3-A_0 to F = 0	t_{PHL5}	R_L = 190Ω R = 1.0 kΩ $RAM_{3,0}$, $Q_{3,0}$ C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH5}			53	ns
Delay from A_3-A_0 to OVR	t_{PHL6}	R_L = 316Ω F = 0 C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH6}			53	ns
Delay from A_3-A_0 to RAM_3 and $\overline{RAM}_0$	t_{PHL7}	C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH7}			53	ns
Delay from B_3-B_0 to Y_3-Y_0	t_{PHL8}			53	ns
	t_{PLH8}			53	ns
Delay from B_3-B_0 to F_3	t_{PHL9}			53	ns
	t_{PLH9}			53	ns
Delay from B_3-B_0 to C_{n+4}	t_{PHL10}			53	ns
	t_{PLH10}			53	ns
Delay from B_3-B_0 to $\overline{G}$ and $\overline{P}$	t_{PHL11}			49	ns
	t_{PLH11}			49	ns
Delay from B_3-B_0 to F = 0	t_{PHL12}			53	ns
	t_{PLH12}			53	ns
Delay from B_3-B_0 to OVR	t_{PHL13}	R_L = 68Ω R = 1.5 kΩ Y_3-Y_0, $\overline{G}$ C_L = 50 ±5 pF all outputs		53	ns
	t_{PLH13}			53	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits		Unit
			Min	Max	
Delay from B_3-B_0 to RAM_3 and RAM_0	t_{PHL14}	R_L = 110Ω R = 2.4 kΩ		53	ns
	t_{PLH14}	C_{n+4} C_L = 50 ±5 pF all outputs		53	ns
Delay from D_3-D_0 (ARITH) to Y_3-Y_0	t_{PHL15}	R_L = 140Ω R = 3.0 kΩ		42	ns
	t_{PLH15}	OVR, $\overline{P}$ C_L = 50 ±5 pF all outputs		42	ns
Delay from D_3-D_0 (ARITH) to F_3	t_{PHL16}	R_L = 190Ω R_1 = 4.0 kΩ		42	ns
	t_{PLH16}	F_3 C_L = 50 ±5 pF all outputs		42	ns
Delay from D_3-D_0 (ARITH) to C_{n+4}	t_{PHL17}	R_L = 190Ω R = 1.0 kΩ		42	ns
	t_{PLH17}	$RAM_{3,0}$, $Q_{3,0}$ C_L = 50 ±5 pF all outputs		42	ns
Delay from D_3-D_0 (ARITH) to $\overline{G}$ and $\overline{P}$	t_{PHL18}	R_L = 316Ω F = 0		40	ns
	t_{PLH18}	C_L = 50 ±5 pF all outputs		40	ns
Delay from D_3-D_0 (ARITH) to F = 0	t_{PHL19}	C_L = 50 ±5 pF all outputs		45	ns
	t_{PLH19}			45	ns
Delay from D_3-D_0 (ARITH) to OVR	t_{PHL20}			42	ns
	t_{PLH20}			42	ns
Delay from D_3-D_0 (ARITH) to RAM_3 and RAM_0	t_{PHL21}			42	ns
	t_{PLH21}			42	ns
Delay from D_3-D_0 (I = X37) to Y_3-Y_0	t_{PHL22}			42	ns
	t_{PLH22}			42	ns
Delay from D_3-D_0 (I = X37) to F_3	t_{PHL23}			42	ns
	t_{PLH23}			42	ns
Delay from D_3-D_0 (I = X37) to F = 0	t_{PHL24}			45	ns
	t_{PLH24}			45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits Min	Limits Max	Unit
Delay from D_3-D_0 (I = X37) to RAM_3 and RAM_0	t_{PHL25}	R_L = 68Ω R = 1.5 kΩ Y_3-Y_0, $\overline{G}$ C_L = 50 ±5 pF all outputs		42	ns
	t_{PLH25}			42	ns
Delay from C_n to Y_3-Y_0	t_{PHL26}	R_L = 110Ω R = 2.4 kΩ C_{n+4} C_L = 50 ±5 pF all outputs		30	ns
	t_{PLH26}			30	ns
Delay from C_n to F_3	t_{PHL27}	R_L = 140Ω R = 3.0 kΩ OVR, $\overline{P}$ C_L = 50 ±5 pF all outputs		30	ns
	t_{PLH27}			30	ns
Delay from C_n to C_{n+4}	t_{PHL28}	R_L = 190Ω R_1 = 4.0 kΩ F_3 C_L = 50 ±5 pF all outputs		25	ns
	t_{PLH28}			25	ns
Delay from C_n to F = 0	t_{PHL29}	R_L = 190Ω R = 1.0 kΩ $RAM_{3,0}$, $Q_{3,0}$ C_L = 50 ±5 pF all outputs		33	ns
	t_{PLH29}			33	ns
Delay from C_n to OVR	t_{PHL30}	R_L = 316Ω F = 0 C_L = 50 ±5 pF all outputs		30	ns
	t_{PLH30}			30	ns
Delay from C_n to RAM_3 and RAM_0	t_{PHL31}	C_L = 50 ±5 pF all outputs		33	ns
	t_{PLH31}			33	ns
Delay from I_2-I_0 to Y_3-Y_0	t_{PHL32}			45	ns
	t_{PLH32}			45	ns
Delay from I_2-I_0 to F_3	t_{PHL33}			45	ns
	t_{PLH33}			45	ns
Delay from I_2-I_0 to C_{n+4}	t_{PHL34}			45	ns
	t_{PLH34}			45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits		Unit
			Min	Max	
Delay from I_2-I_0 to $\overline{G}$ and $\overline{P}$	t_{PHL35}	C_L = 50 ±5 pF all outputs		50	ns
	t_{PLH35}			50	ns
Delay from I_2-I_0 to F = 0	t_{PHL36}			49	ns
	t_{PLH36}			49	ns
Delay from I_2-I_0 to OVR	t_{PHL37}			45	ns
	t_{PLH37}			45	ns
Delay from I_2-I_0 to RAM_3 and RAM_0	t_{PHL38}	R_L = 68Ω R = 1.5 kΩ		45	ns
	t_{PLH38}	Y_3-Y_0, G C_L = 50 ±5 pF all outputs		45	ns
Delay from I_5-I_3 to Y_3-Y_0	t_{PHL39}	R_L = 110Ω R = 2.4 kΩ		45	ns
	t_{PLH39}	C_{n+4} C_L = 50 ±5 pF all outputs		45	ns
Delay from I_5-I_3 to F_3	t_{PHL40}	R_L = 140Ω R = 3.0 kΩ		45	ns
	t_{PLH40}	OVR, $\overline{P}$ C_L = 50 ±5 pF all outputs		45	ns
Delay from I_5-I_3 to C_{n+4}	t_{PHL41}	R_L = 190Ω R_1 = 4.0 kΩ		45	ns
	t_{PLH41}	F_3 C_L = 50 ±5 pF all outputs		45	ns
Delay from I_5-I_3 to $\overline{G}$, $\overline{P}$	t_{PHL42}	R_L = 190Ω R = 1.0 kΩ		45	ns
	t_{PLH42}	$RAM_{3,0}$, $Q_{3,0}$ C_L = 50 ±5 pF all outputs		45	ns
Delay from I_5-I_3 to F = 0	t_{PHL43}	R_L = 316Ω F = 0		45	ns
	t_{PLH43}	C_L = 50 ±5 pF all outputs		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits		Unit
			Min	Max	
Delay from I_5-I_3 to OVR	t_{PHL44}	C_L = 50 ±5 pF all outputs		45	ns
	t_{PLH44}			45	ns
Delay from I_5-I_3 to RAM_3 and $\overline{RAM}_0$	t_{PHL45}			45	ns
	t_{PLH45}			45	ns
Delay from I_8-I_6 to Y_3-Y_0	t_{PHL46}			35	ns
	t_{PLH46}			35	ns
Delay from A_3-A_0 (I = 2XX) to Y_3-Y_0	t_{PHL47}			45	ns
	t_{PLH47}			45	ns
Delay from CP to Y_3-Y_0	t_{PHL48}			45	ns
	t_{PLH48}			45	ns
Delay from CP to F_3	t_{PHL49}			45	ns
	t_{PLH49}			45	ns
Delay from CP to C_{n+4}	t_{PHL50}			45	ns
	t_{PLH50}			45	ns
Delay from CP to $\overline{G}$ and $\overline{P}$	t_{PHL51}	R_L = 68Ω R_1 = 1.5 kΩ		45	ns
	t_{PLH51}	Y_3-Y_0, $\overline{G}$ C_L = 50 ±5 pF all outputs		45	ns
Delay from CP to to F = 0	t_{PHL52}	R_L = 110Ω R_1 = 2.4 kΩ		45	ns
	t_{PLH52}	C_{n+4} C_L = 50 ±5 pF all outputs		45	ns
Delay from CP to OVR	t_{PHL53}	R_L = 140Ω R_1 = 3.0 kΩ		45	ns
	t_{PLH53}	OVR, $\overline{P}$ C_L = 50 ±5 pF all outputs		45	ns
Delay from CP to RAM_3 and $\overline{RAM}_0$	t_{PHL54}	R_L = 190Ω R_1 = 4.0 kΩ		45	ns
	t_{PLH54}	F_3 C_L = 50 ±5 pF all outputs		45	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$	Limits		Unit
			Min	Max	
Delay from CP to Q_3 and Q_0	t_{PHL55}	R_L = 190Ω R = 1.0 kΩ $RAM_{3,0}$, $Q_{3,0}$ C_L = 50 ±5 pF all outputs		38	ns
	t_{PLH55}			38	ns
Delay from $\overline{OE}$ to Y_3-Y_0	t_{PZL1}	R_L = 316Ω F = 0 C_L = 50 ±5 pF all outputs		30	ns
	t_{PZH1}			30	ns
Delay from I_8 to RAM_3 and RAM_0	t_{PZL2}	C_L = 50 ±5 pF all outputs		35	ns
	t_{PZH2}			35	ns
Delay from I_8 to Q_3 and Q_0	t_{PZL3}			35	ns
	t_{PZH3}			35	ns
Delay from $\overline{OE}$ to Y_3-Y_0 Float	t_{PLZ1}			30	ns
	t_{PHZ1}			30	ns
Delay from I_8 to RAM_3 and RAM_0 Float	t_{PLZ2}			34	ns
	t_{PHZ2}			34	ns
Delay from I_8 to Q_3 and Q_0 float	t_{PLZ3}			34	ns
	t_{PHZ3}			34	ns
Minimum clock low time	t_{PWL}			20	ns
Minimum clock high time	t_{PWH}			20	ns

1/ These are three-state outputs internally connected to TTL inputs. The tristate condition must be OFF.
2/ Not more than one output should be shorted at a time. Duration of the short circuit test shall not exceed 1 second.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. The "JAN" or "J" certification mark shall not be used.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 107 (see MIL-M-38510, appendix E).

3.8 Certification. Certification in accordance with MIL-M-38510 is not required by this device.

3.9 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line, not necessarily the line producing the device type described herein.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1,7	1,7
Final electrical test parameters (method 5004)	1*,2,3,7*, 8,9,10,11	1*,2,3,7*, 8,9**
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11	1,7,8,9**, 10,11,2,3
Group B test requirements (method 5005) subgroup 5	1,2,3,7,8, 9,10,11	N/A
Groups C and D end-point electrical parameters (method 5005)	1,2,3,7,8	1,2,3,7,8
Additional electrical subgroups for groups C and D period 1C inspections	None	None

*PDA applies to subgroups 1 and 7 (see 4.2c).
**Subgroup 9 is run concurrently with subgroup 7 with a combined LTPD of 5.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in (method 1015 of MIL-STD-883).

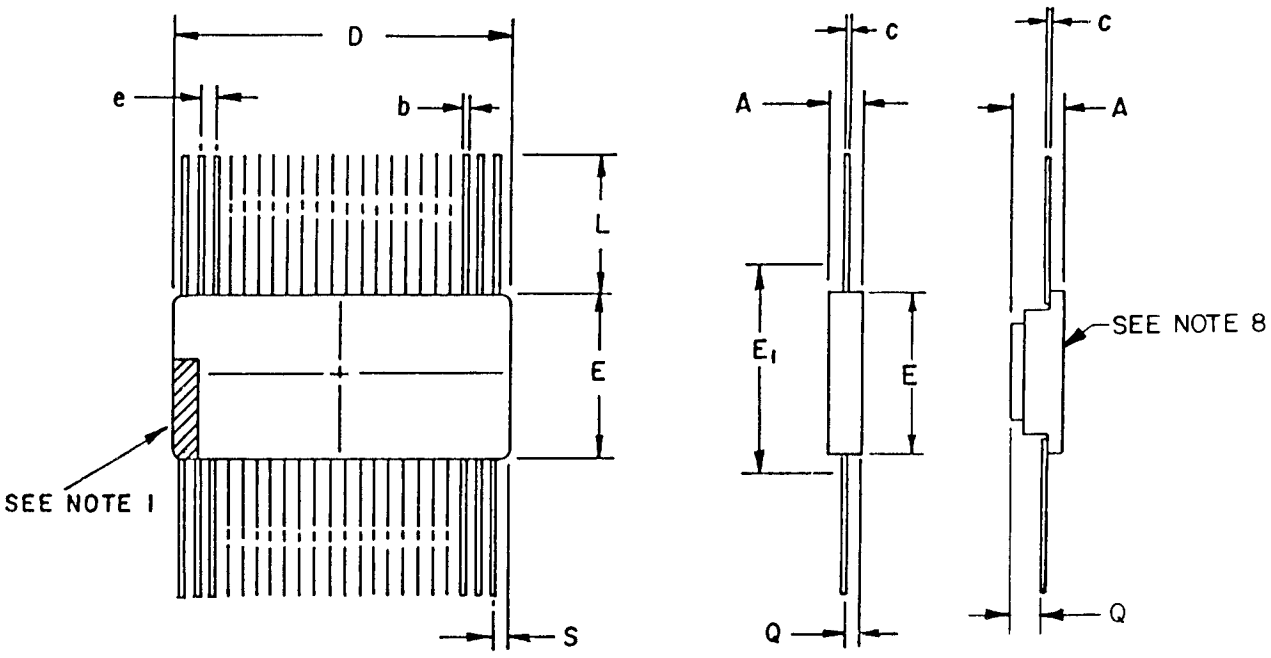
(1) Test condition C, using the circuit shown on figure 5, or equivalent.

(2) T_A = +125°C minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. Constant acceleration in accordance with test condition D of method 2001 of MIL-STD-883.



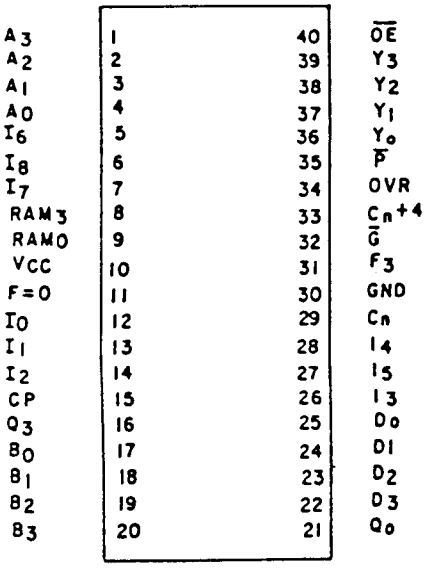
Ltr	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	.070	.115	1.78	2.92	
b	.017	.023	.43	.58	5
c	.006	.012	.15	.30	5
D	1.030	1.090	26.16	27.69	
E	.600	.660	15.24	16.76	
E_1	---	.690	---	17.53	3
e	.045	.055	1.14	1.40	4,6
L	.250	.370	6.35	9.40	
L_1	1.300	1.370	33.02	34.80	
Q	.020	.060	.51	1.52	2
S	.005	---	.13	---	7

NOTES:
1. Index area; a notch or a pin one identification mark shall be located adjacent to pin one and shall be within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. Dimension Q shall be measured at the point of exit of the lead from the body.
3. This dimension allows for off-center lid, meniscus and glass overrun.
4. The basic pin spacing is .050 (1.25 mm) between centerlines. Each pin centerline shall be located within ±.005 (.13 mm) of its exact logitudinal position relative to pins 1 and 42.
5. All leads - Increase maximum limit by .003 (.08 mm) measured at the center of the flat, when lead finish A is applied.
6. Forty spaces.
7. Applies to all four corners (leads number 1, 21, 22, and 42).
8. Configuration 2 is optional. If this configuration is used, no organic or polymeric materials shall be molded to the top of the package to cover the leads.

FIGURE 1. Case outline Z (42-lead, 0.6" x 1.0").

Device type 01

Case outline Q



Case outline Z

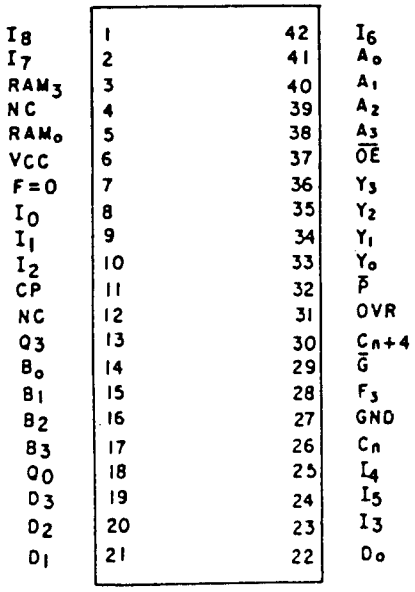


FIGURE 2. Terminal connections.

DEVICE TYPE 01

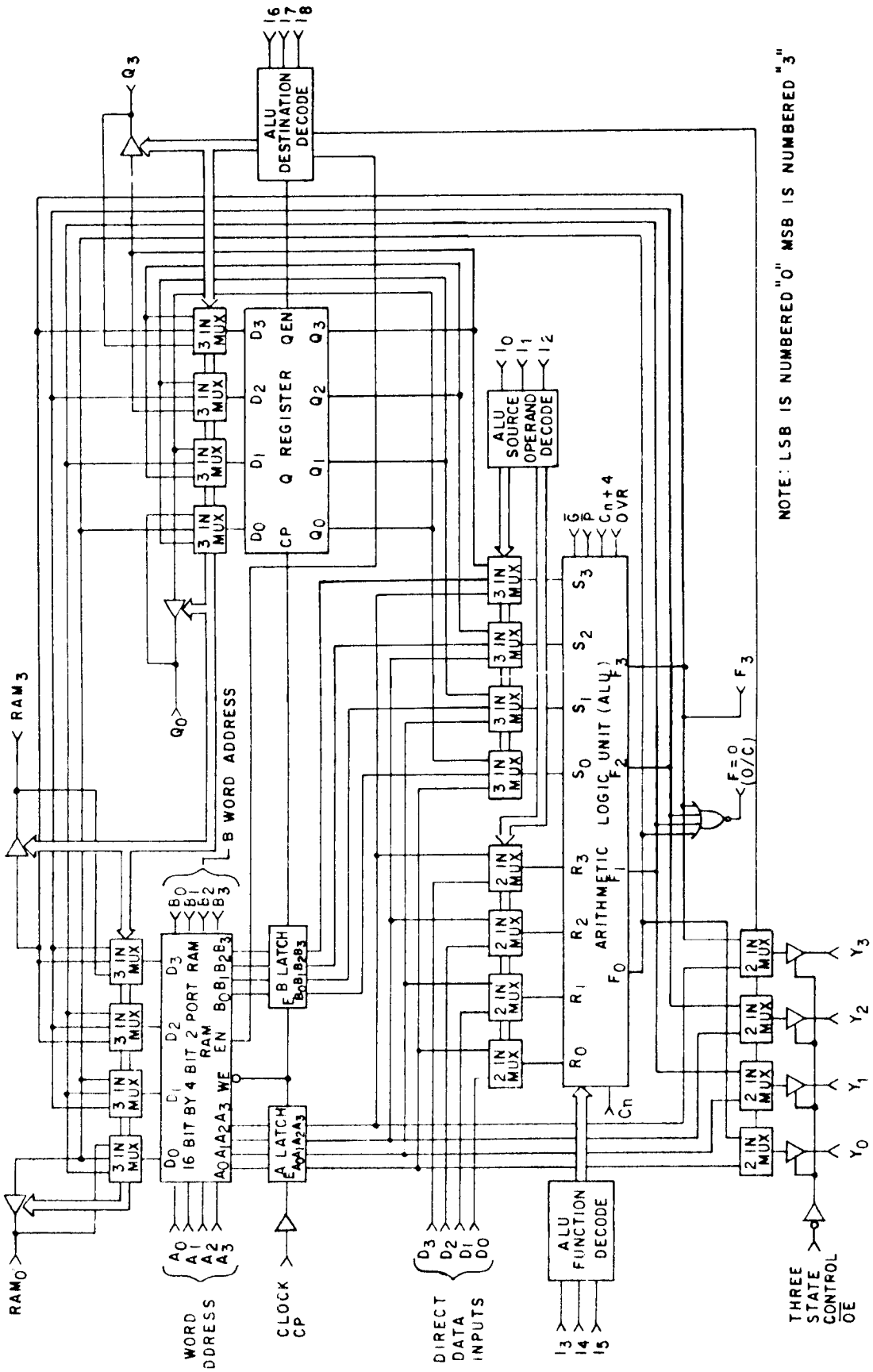


FIGURE 3. Logic block diagram.

DEVICE TYPE 01

Micro code				ALU source operands	
I_2	I_1	I_0	Octal code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	0	Q
L	H	H	3	0	B
H	L	L	4	0	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	0

ALU source operand control.

Micro code				ALU Function	Symbol
I_5	I_4	I_3	Octal code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S - R
L	H	L	2	R Minus S	R - S
L	H	H	3	R OR S	$R \vee S$
H	L	L	4	R AND S	$R \wedge S$
H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
H	H	L	6	R EX-OR S	$R \veebar S$
H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

ALU function control.

Micro code				RAM Function		Q-REG Function		Y Output	RAM Shifter		Q Shifter	
I_8	I_7	I_6	Octal code	Shift	Load	Shift	Load		RAM_0	RAM_3	Q_0	Q_3
L	L	L	0	X	None	None	F → Q	F	X	X	X	X
L	L	H	1	X	None	X	None	F	X	X	X	X
L	H	L	2	None	F → B	X	None	A	X	X	X	X
L	H	H	3	None	F → B	X	None	F	X	X	X	X
H	L	L	4	Down	F/2 → B	Down	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	Down	F/2 → B	X	None	F	F_0	IN_3	Q_0	X
H	H	L	6	Up	2F → B	Up	2Q → Q	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	Up	2F → B	X	None	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
B = Register Addressed by B inputs.
Up is toward MSB; Down is toward LSB.

ALU destination control.

FIGURE 4. Truth tables and logic equations.

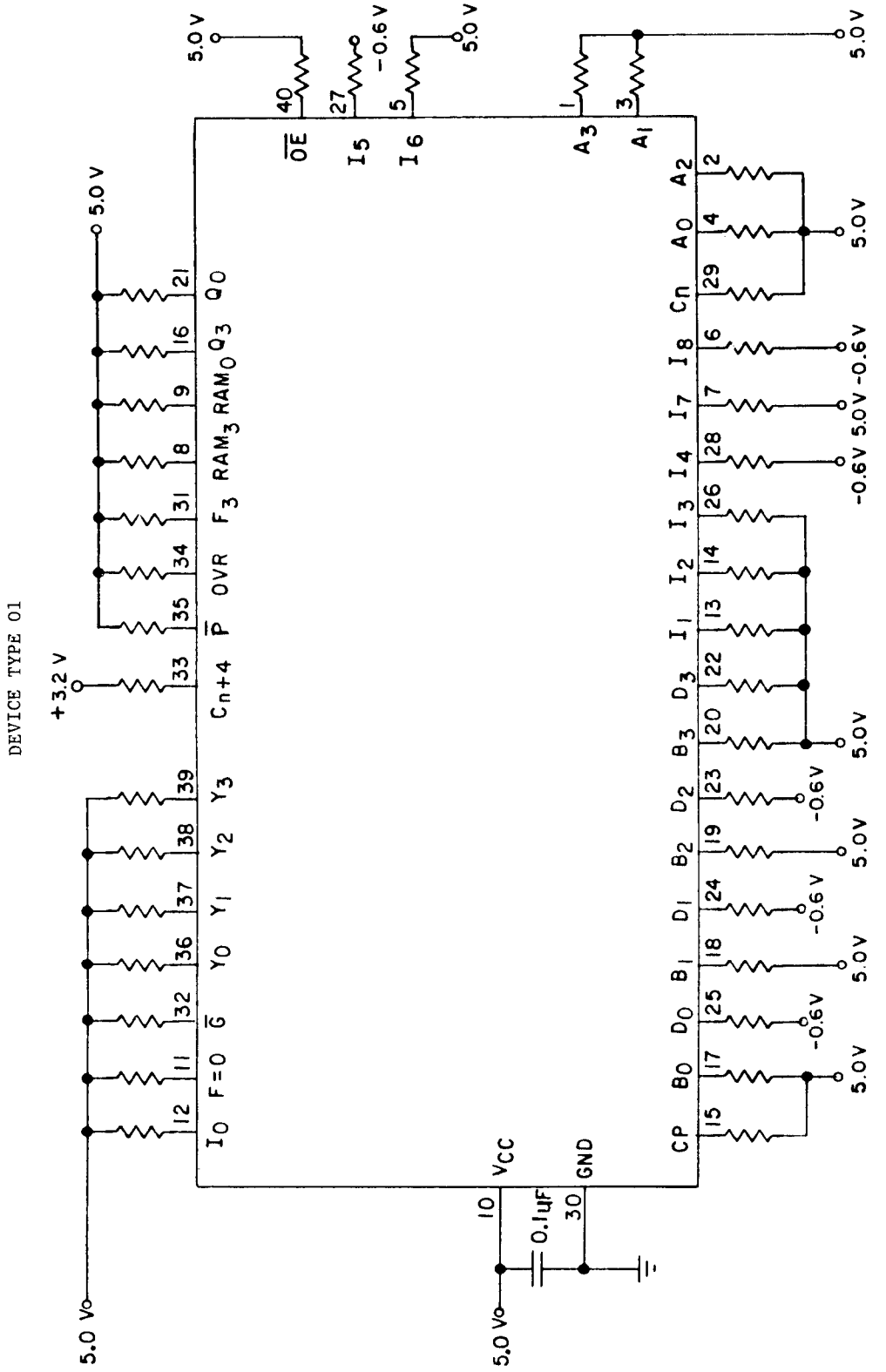
DEVICE TYPE 01

I_{210} Octal		0	1	2	3	4	5	6	7
Octal I_{543}	ALU Source / ALU Function	A,Q	A,B	0,Q	0,B	0,A	D,A	D,Q	D,0
0	C_n = L R Plus S C_n = H	A+Q A+Q+1	A+B A+B+1	Q Q+1	B B+1	A A+1	D+A D+A+1	D+Q D+Q+1	D D+1
1	C_n = L S Minus R C_n = H	Q-A-1 Q-A	B-A-1 B-A	Q-1 Q	B-1 B	A-1 A	A-D-1 A-D	Q-D-1 Q-D	-D-1 -D
2	C_n = L R Minus S C_n = H	A-Q-1 A-Q	A-B-1 A-B	-Q-1 -Q	-B-1 -B	-A-1 -A	D-A-1 D-A	D-Q-1 D-Q	D-1 D
3	R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4	R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7	R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; - = Minus; $\vee$ = OR; $\wedge$ = AND; $\veebar$ = EX-OR

Source operand and ALU function matrix.

FIGURE 4. Truth tables and logic equations - Continued.

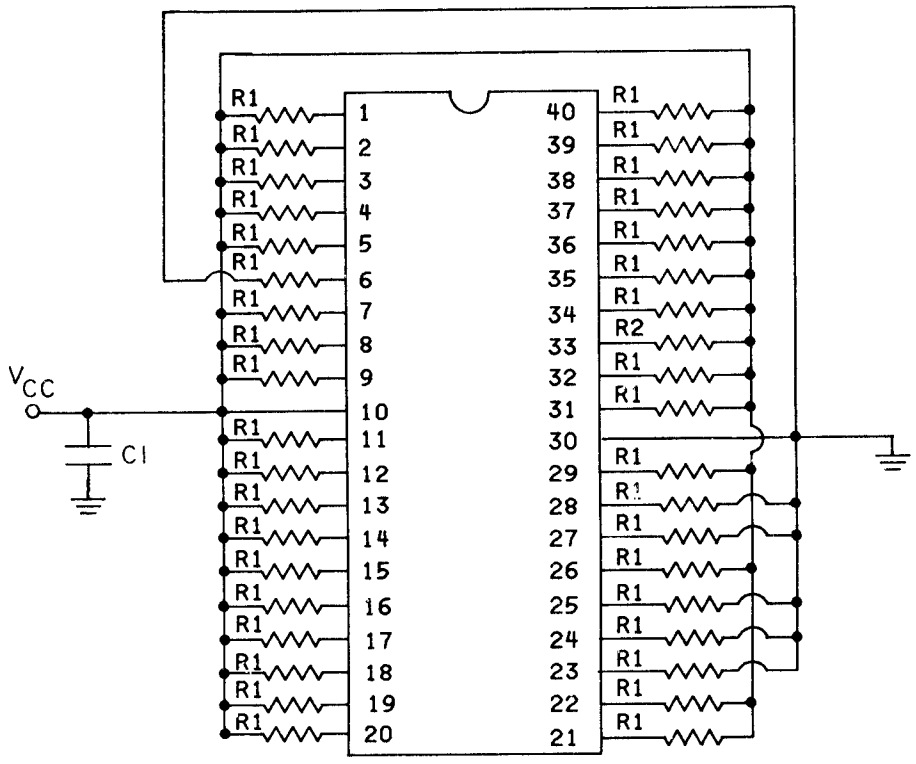


NOTES:
1. All resistors are 270Ω ±5%.
2. V_{CC} shall be no less than 4.5 V and no greater than 5.5 V.

FIGURE 5. Static burn-in circuit - case outline Q.

Alternate Condition "A"

Case outline Q

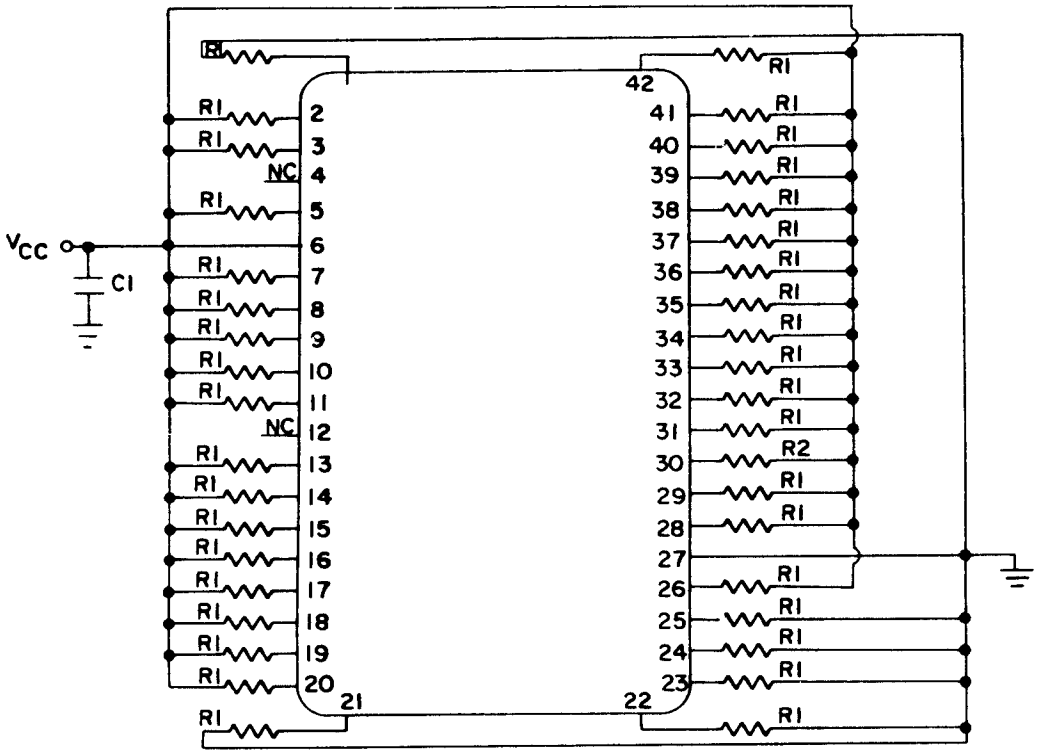


NOTES:
1. C1 = .1 µF.
2. R1 = 267Ω ±5%, R2 = 422Ω ±5%.
3. V_{CC} shall be no less than 4.5 V and no greater than 5.5 V.

FIGURE 5. Static burn-in circuit - Continued.

Alternate Condition "C"

Case outline Z



NOTES:
1. C1 = .1 µF.
2. R1 = 267Ω ±5%, R2 = 422Ω ±5%.
3. V_{CC} shall be no less than 4.5 V and no greater than 5.5 V.

FIGURE 5. Static burn-in circuit - Continued.

TABLE IIIA. Group A inspection.
Terminal conditions (input only pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Subgroup	Symbol	MIL-STD-883 method	Case Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
			Case Z	38	39	40	41	42	1	2	3	5	6	7	8	9	10	11	13	14	15	16	17
			Test no.	A_3	A_2	A_1	A_0	I_6	I_9	I_7	RAM_3	RAM_0	V_{CC}	F = 0	I_0	I_1	I_2	CP	Q_3	B_0	B_1	B_2	B_3
1 T_C = +25°C	I_{CC}	3005	1	GND	GND	GND	GND	GND	GND	5.5 V	GND	GND	5.5 V		5.5 V	5.5 V	5.5 V	GND	GND	GND	GND	GND	GND
		2/						GND	GND	GND			4.5 V		4.5 V	4.5 V	4.5 V	3/					
	V_{OH4}	3006	2					2.0 V	2.0 V	0.8 V		-0.6 mA	"		2.0 V	2.0 V	2.0 V						
		"	3					"	"	0.8 V			"		"	"	"	2.0 V					
		"	4					"	"	2.0 V	-0.6 mA		"		"	"	"						
		"	5					"	"	2.0 V			"		"	"	"	2.0 V	-0.6 mA				
		2/						4.5 V	GND	4.5 V			"		4.5 V	4.5 V	4.5 V	3/		GND	GND	GND	GND
			6					2.0 V	0.8 V	2.0 V			"		2.0 V	2.0 V	2.0 V						
	V_{OH1}	3006	7	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
		2/						4.5 V	GND	4.5 V			"		4.5 V	4.5 V	4.5 V	3/		GND	GND	GND	GND
	V_{OH3}	3006	8	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
	V_{OH2}	"	9	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
		2/						4.5 V	GND	4.5 V			"		4.5 V	4.5 V	4.5 V	3/		GND	GND	GND	GND
	V_{OH2}	3006	10	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
	V_{OH1}	"	11					2.0 V	2.0 V	2.0 V			"		"	2.0 V	2.0 V						
		"	12					"	"	"			"		"	"	"						
		"	13					"	"	"			"		"	"	"						
		"	14					"	"	"			"		"	"	"						
	I_{CEX}		15					"	0.8 V	"			"	5.5 V	"	"	"						
		2/						GND	GND	GND			"		4.5 V	4.5 V	4.5 V	3/					
	V_{OL4}	3007	16					2.0 V	2.0 V	0.8 V		6 mA	"		2.0 V	2.0 V	2.0 V						
		"	17					"	"	0.8 V			"		"	"	"						
		"	18					"	"	2.0 V	6 mA		"		"	"	"						
		"	19					"	"	"			"		"	"	"		6 mA				
	V_{OL1}	"	20					"	0.8 V	"			"	16 mA	"	"	"						
		2/						4.5 V	GND	4.5 V			"		4.5 V	4.5 V	4.5 V	3/		GND	GND	GND	GND
	V_{OL4}	3007	21					2.0 V	0.8 V	2.0 V			"		2.0 V	2.0 V	2.0 V						

See footnotes at end of table.

TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Case Q	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Limits		Unit
Case Z	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37		Min	Max	
Test no.	Q_0	D_3	D_2	D_1	D_0	I_3	I_5	I_4	C_n	GND	F_3	$\overline{G}$	C_{n+4}	OVR	$\overline{P}$	Y_0	Y_1	Y_2	Y_3	$\overline{OE}$				
1	GND	5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	GND	5.5 V	GND										5.5 V	V_{CC}	100	280	mA
2/		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	4.5 V		"										GND				
2		2.0 V	2.0 V	2.0 V	2.0 V	2.0 V	0.8 V	2.0 V		"											RAM_0	2.4	4.2	V
3	-0.6 mA	"	"	"	"	"	"	"		"											Q_0	"	"	"
4		"	"	"	"	"	"	"		"											RAM_3	"	"	"
5		"	"	"	"	"	"	"		"											Q_3	"	"	"
2/		4.5 V	GND	GND	GND	4.5 V	GND	4.5 V		"										GND				
6		2.0 V	0.8 V	0.8 V	0.8 V	2.0 V	0.8 V	2.0 V		"	-0.5 mA										F_3	2.4	4.2	V
7						0.8 V	0.8 V	0.8 V		"		-1.6 mA									$\overline{G}$	2.4	4.2	V
2/		4.5 V	GND	GND	GND	4.5 V	GND	4.5 V		"										GND				
8						0.8 V	0.8 V	0.8 V		"			-1.0 mA								C_{n+4}	2.4	4.2	V
9						0.8 V	0.8 V	0.8 V		"				-0.8 mA							OVR	2.4	4.2	V
2/		GND	GND	GND	GND	4.5 V	GND	4.5 V		"										GND				
10						0.8 V	0.8 V	0.8 V		"					-0.8 mA						$\overline{P}$	2.4	4.2	V
11		2.0 V	2.0 V	2.0 V	2.0 V	"	2.0 V	2.0 V		"						-1.6 mA				0.8 V	Y_0	"	"	"
12		"	"	"	"	"	"	"		"							-1.6 mA			"	Y_1	"	"	"
13		"	"	"	"	"	"	"		"								-1.6 mA		"	Y_2	"	"	"
14		"	"	"	"	"	"	"		"									-1.6 mA	"	Y_3	"	"	"
15		0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	0.8 V	2.0 V		"											F = 0	-40	250	µA
2/		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	4.5 V		"										GND				
16		0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	0.8 V	2.0 V		"											RAM_0	0	0.5	V
17	6 mA	"	"	"	"	"	"	"		"											Q_0	"	"	"
18		"	"	"	"	"	"	"		"											RAM_3	"	"	"
19		"	"	"	"	"	"	"		"											Q_3	"	"	"
20		2.0 V	"	"	"	"	"	"		"											F = 0	"	"	"
2/		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	4.5 V		"										GND				
21		0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	0.8 V	2.0 V		"	6 mA										F_3	0	0.5	V

See footnotes at end of table.

TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Subgroup	Symbol	MIL-STD-883 method	Case Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
			Case Z	38	39	40	41	42	1	2	3	5	6	7	8	9	10	11	13	14	15	16	17
			Test no.	A_3	A_2	A_1	A_0	I_6	I_8	I_7	RAM_3	RAM_0	V_{CC}	F = 0	I_0	I_1	I_2	CP	Q_3	B_0	B_1	B_2	B_3
1 T_C = +25°C	V_{OL1}	3007	22	0.8 V	0.8 V	0.8 V	0.8 V						4.5 V		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
		2/						4.5 V	GND	4.5 V			"		4.5 V	4.5 V	4.5 V	3/		GND	GND	GND	GND
	V_{OL3}		23	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
	V_{OL2}		24	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V			0.8 V	0.8 V	0.8 V	0.8 V
		2/						4.5 V	GND	4.5 V			"		4.5 V	4.5 V	4.5 V	3/		GND	GND	GND	GND
			25	0.8 V	0.8 V	0.8 V	0.8 V						"		2.0 V	0.8 V	0.8 V	2.0 V		0.8 V	0.8 V	0.8 V	0.8 V
	V_{OL1}	3007	26					2.0 V	0.8 V	0.8 V			"		"	2.0 V	2.0 V						
		"	27					"	"	"			"		"	"	"						
		"	28					"	"	"			"		"	"	"						
		"	29					"	"	"			"		"	"	"						
	I_{ZH1}		30					4.5 V	GND	GND			5.5 V		4.5 V	4.5 V	4.5 V						
			31					"	"	"			"		"	"	"						
			32					"	"	"			"		"	"	"						
			33					GND	"	"			"		"	"	"	3/					
	I_{ZH2}		34					"	"	"	2.4 V		"		"	"	"						
			35					"	"	"		2.4 V	"		"	"	"						
			36					"	"	"			"		"	"	"		2.4 V				
			37					"	"	"			"		"	"	"						
	I_{ZL1}		38					4.5 V	"	"			"		"	"	"						
			39					"	"	"			"		"	"	"						
			40					"	"	"			"		"	"	"						
			41					GND	"	"			"		"	"	"	3/					
	I_{ZL2}		42					"	"	"	0.5 V		"		"	"	"						
			43					"	"	"		0.5 V	"		"	"	"						
			44					"	"	"			"		"	"	"		0.5 V				
			45					"	"	"			"		"	"	"						
	I_{IH1}	3010	46	2.7 V									"										
		"	47		2.7 V								"										
		"	48			2.7 V							"										
		"	49				2.7 V						"										
		"	50					2.7 V					"										
		"	51						2.7 V				"										
		"	52										"		2.7 V								
		"	53										"			2.7 V							
		"	54										"				2.7 V						
		"	55										"					2.7 V					
		"	56										"							2.7 V			
		"	57										"								2.7 V		
		"	58										"									2.7 V	
		"	59										"										2.7 V

See footnotes at end of table.

TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Case Q	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Limits		Unit
Case Z	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37				
Test no.	Q_0	D_3	D_2	D_1	D_0	I_3	I_5	I_4	C_n	GND	F_3	$\overline{G}$	C_{n+4}	OVR	$\overline{P}$	Y_0	Y_1	Y_2	Y_3	$\overline{OE}$		Min	Max	
22						0.8 V	0.8 V	0.8 V		GND		16 mA									$\overline{G}$	0	0.5	V
2/		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	GND	4.5 V		"										GND				
23						0.8 V	0.8 V	0.8 V		"			10 mA								C_{n+4}	0	0.5	V
24						0.8 V	0.8 V	0.8 V		"				8 mA							OVR	0	0.5	V
2/		GND	GND	GND	GND	4.5 V	GND	4.5 V		"										GND				
25						0.8 V	0.8 V	0.8 V		"					8 mA						$\overline{P}$	0	0.5	V
26		0.8 V	0.8 V	0.8 V	0.8 V	2.0 V	0.8 V	2.0 V		"						16 mA				0.8 V	Y_0	"	"	"
27		"	"	"	"	"	"	"		"							16 mA			"	Y_1	"	"	"
28		"	"	"	"	"	"	"		"								16 mA		"	Y_2	"	"	"
29		"	"	"	"	"	"	"		"									16 mA	"	Y_3	"	"	"
30		GND	GND	GND	GND	4.5 V	GND	4.5 V		"						2.4 V				0 V	Y_0	-50	50	µA
31		"	"	"	"	"	"	"		"							2.4 V			"	Y_1	"	"	"
32		"	"	"	"	"	"	"		"								2.4 V		"	Y_2	"	"	"
33		"	"	"	"	"	"	"		"									2.4 V	"	Y_3	"	"	"
34		"	"	"	"	"	"	"		"											RAM_3	-10	100	"
35		"	"	"	"	"	"	"		"											RAM_0	"	"	"
36		"	"	"	"	"	"	"		"											Q_3	"	"	"
37	2.4 V	"	"	"	"	"	"	"		"											Q_0	"	"	"
38		4.5 V	4.5 V	4.5 V	4.5 V	"	"	"		"						0.5 V				0 V	Y_0	50	-50	"
39		"	"	"	"	"	"	"		"							0.5 V			"	Y_1	"	"	"
40		"	"	"	"	"	"	"		"								0.5 V		"	Y_2	"	"	"
41		"	"	"	"	"	"	"		"									0.5 V	"	Y_3	"	"	"
42		"	"	"	"	"	"	"		"											RAM_3	20	-800	"
43		"	"	"	"	"	"	"		"											RAM_0	"	"	"
44		"	"	"	"	"	"	"		"											Q_3	"	"	"
45	0.5 V	"	"	"	"	"	"	"		"											Q_0	"	"	"
46										"											A_3	-10	20	"
47										"											A_2	"	"	"
48										"											A_1	"	"	"
49										"											A_0	"	"	"
50										"											I_6	"	"	"
51										"											I_8	"	"	"
52										"											I_0	"	"	"
53										"											I_1	"	"	"
54										"											I_2	"	"	"
55										"											C_8	"	"	"
56										"											B_0	"	"	"
57										"											B_1	"	"	"
58										"											B_2	"	"	"
59										"											B_3	"	"	"

See footnotes at end of table.

TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Subgroup	Symbol	MIL-STD-883 method	Case Q	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
			Case Z	38	39	40	41	42	1	2	3	5	6	7	8	9	10	11	13	14	15	16	17
			Test no.	A_3	A_2	A_1	A_0	I_6	I_8	I_7	RAM_3	RAM_0	V_{CC}	F = 0	I_0	I_1	I_2	CP	Q_3	B_0	B_1	B_2	B_3
1 T_C = +25°C	I_{IH2}	3010	60										5.5 V				GND						
		"	61										"				"						
		"	62										"				"						
		"	63										"										
		"	64										"										
		"	65							2.7 V			"										
	I_{IH1}	"	66										"										
	I_{IH2}	"	67										"										
		"	68										"										
	I_{IH3}	"	69						GND	GND		2.7 V	"										
		"	70						"	GND			"										
		"	71						"	4.5 V	2.7 V		"										
		"	72						"	4.5 V			"						2.7 V				
	I_{IH4}	"	73										"		5.5 V	5.5 V	5.5 V						
	I_{IL2}	3009	74	0.5 V									"										
		"	75		0.5 V								"										
		"	76			0.5 V							"										
		"	77				0.5 V						"										
	I_{IL1}	"	78					0.5 V					"										
		"	79						0.5 V				"										
		"	80										"		0.5 V								
		"	81										"			0.5 V							
	I_{IL2}	"	82										"				0.5 V						
		"	83										"					0.5 V					
		"	84										"							0.5 V			
		"	85										"								0.5 V		
		"	86										"									0.5 V	
		"	87										"										0.5 V
	I_{IL1}	"	88										"										
	I_{IL4}		89							0.5 V			"										
	I_{IL3}	3009	90										"			4.5 V	4.5 V						
		"	91										"			"	"						
		"	92										"			"	"						
		"	93										"			"	"						
	I_{IL4}		94										"										
			95										"										
			96										"										

See footnotes at end of table.

TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Case Q	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Limits		Unit
Case Z	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37				
Test no.	Q_0	D_3	D_2	D_1	D_0	I_3	I_5	I_4	C_n	GND	F_3	$\overline{G}$	C_{n+4}	OVR	$\overline{P}$	Y_0	Y_1	Y_2	Y_3	$\overline{OE}$		Min	Max	
60		2.7 V								GND											D_3	-10	40	µA
61			2.7 V							"											D_2	"	"	"
62				2.7 V						"											D_1	"	"	"
63					2.7 V					"											D_0	"	"	"
64						2.7 V		GND		"											I_3	"	"	"
65										"											I_7	"	"	"
66										"										2.7 V	$\overline{OE}$	"	20	"
67							2.7 V	GND		"											I_5	"	40	"
68						GND		2.7 V		"											I_4	"	"	"
69										"											RAM_0	"	100	"
70	2.7 V									"											Q_0	"	"	"
71										"											RAM_3	"	"	"
72										"											Q_3	"	"	"
73		GND	GND	GND	GND	5.5 V	GND	5.5 V	2.7 V	"											C_n	-40	200	"
74										"											A_3	0.02	-0.36	mA
75										"											A_2	"	"	"
76										"											A_1	"	"	"
77										"											A_0	"	"	"
78										"											I_6	"	"	"
79										"											I_8	"	"	"
80										"											I_0	"	"	"
81										"											I_1	"	"	"
82										"											I_2	"	"	"
83										"											$\overline{CP}$	"	"	"
84										"											B_0	"	"	"
85										"											B_1	"	"	"
86										"											B_2	"	"	"
87										"											B_3	"	"	"
88										"										0.5 V	$\overline{OE}$	"	"	"
89										"											I_7	.05	-0.72	"
90		0.5 V								"											D_3	"	"	"
91			0.5 V							"											D_2	"	"	"
92				0.5 V						"											D_1	"	"	"
93					0.5 V					"											D_0	"	"	"
94						0.5 V		5.5 V		"											I_3	"	"	"
95							0.5 V	GND		"											I_5	"	"	"
96						5.5 V		0.5 V		"											I_4	"	"	"

See footnotes at end of table.

TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Subgroup	Symbol	MIL-STD-883 method	Case Q / Case Z	1 / 38	2 / 39	3 / 40	4 / 41	5 / 42	6 / 1	7 / 2	8 / 3	9 / 5	10 / 6	11 / 7	12 / 8	13 / 9	14 / 10	15 / 11	16 / 13	17 / 14	18 / 15	19 / 16	20 / 17
			Test no.	A_3	A_2	A_1	A_0	I_6	I_8	I_7	RAM_3	RAM_0	V_{CC}	F = 0	I_0	I_1	I_2	CP	Q_3	B_0	B_1	B_2	B_3
1 T_C = +25°C	I_{IL5}		97					GND	5.5 V	GND	0.5 V		5.5 V										
			98					"	"	GND			"						0.5 V				
			99					"	"	5.5 V		0.5 V	"										
			100					"	"	5.5 V			"										
	I_{IL6}		101										"		5.5 V	5.5 V	5.5 V	GND					
		2/						GND	GND	GND			"		4.5 V		4.5 V	3/					
	I_{OS}	3011	102					4.5 V	4.5 V	GND		0.0 V	"		"	4.5 V	"	4.5 V					
		"	103					"	"	"			"		"		"	"					
		"	104					"	"	4.5 V	0.0 V		"		"		"	"					
		"	105					"	"	"			"		"		"	"	0.0 V				
		2/						"	GND	"			"		"		"	3/		GND	GND	GND	GND
		3011	106					"	GND	"			"		"	4.5 V	"	4.5 V					
	I_{OS}	3011	107	GND	GND	GND	GND						"		"	GND	GND	"		"	"	"	"
		"	108	"	"	"	"						"		"	"	"	"		"	"	"	"
		"	109	"	"	"	"						"		"	"	"	"		"	"	"	"
		"	110	"	"	"	"						"		"	"	"	"		"	"	"	"
		"	111					4.5 V	4.5 V	4.5 V			"		"		4.5 V	"					
		"	112					"	"	"			"		"		"	"					
		"	113					"	"	"			"		"		"	"					
		"	114					"	"	"			"		"		"	"					
		2/						"	GND	"			"		"		"	3/		GND	GND	GND	GND
	V_{IC}		115	-18 mA									4.5 V										
			116		-18 mA								"										
			117			-18 mA							"										
			118				-18 mA						"										
			119					-18 mA					"										
			120						-18 mA				"										
			121							-18 mA			"										
			122								-18 mA		"										
			123									-18 mA	"										
			124										"		-18 mA								
			125										"			-18 mA							
			126										"				-18 mA						
			127										"					-18 mA					
			128										"						-18 mA				
			129										"							-18 mA			
			130										"								-18 mA		
			131										"									-18 mA	
			132										"										-18 mA
			133										"										
			134										"										
			135										"										
			136										"										
			137										"										
			138										"										
			139										"										
			140										"										
			141										"										
			142										"										

See footnotes at end of table.

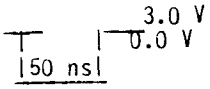
TABLE IIIA. Group A inspection - Continued.
Terminal conditions (input pins not designated must be ≥2.0 V or ≤0.8 V). 1/

Case Q	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Limits		Unit
Case Z	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37		Min	Max	
Test no.	Q_0	D_3	D_2	D_1	D_0	I_3	I_5	I_4	C_n	GND	F_3	$\overline{G}$	C_{n+4}	OVR	$\overline{P}$	Y_0	Y_1	Y_2	Y_3	$\overline{OE}$				
97										GND											RAM_3	.05	-0.8	mA
98										"											Q_3	"	"	"
99										"											RAM_0	"	"	"
100	0.5 V									"											Q_0	"	"	"
101		5.5 V	5.5 V	5.5 V	5.5 V	GND	GND	GND	0.5 V	"											C_n	0.5	-3.6	"
2/		4.5 V	4.5 V	4.5 V	4.5 V	4.5 V	"	4.5 V		"										GND				
102		"	"	"	"	"	"	"		"											RAM_0	-30	-85	mA
103	0.0 V	"	"	"	"	"	"	"		"											Q_0	"	"	"
104		"	"	"	"	"	"	"		"											RAM_3	"	"	"
105		"	"	"	"	"	"	"		"											Q_3	"	"	"
2/		GND	GND	GND	GND	"	"	"		"										GND				
106		4.5 V	GND	GND	GND	"	"	"		"	0.0 V										F_3	-30	-85	mA
107						GND	"	GND		"		0.0 V									$\overline{G}$	-30	-85	mA
108						"	"	"		"			0.0 V								C_{n+4}	"	"	"
109						"	"	"		"				0.0 V							OVR	"	"	"
110						"	"	"		"					0.0 V						$\overline{P}$	"	"	"
111		4.5 V	4.5 V	4.5 V	4.5 V	"	4.5 V	4.5 V		"						0.0 V				GND	Y_0	"	"	"
112		"	"	"	"	"	"	"		"							0.0 V			"	Y_1	"	"	"
113		"	"	"	"	"	"	"		"								0.0 V		"	Y_2	"	"	"
114		"	"		"	"	"	"		"									0.0 V	"	Y_3	"	"	"
2/		GND	GND	GND	GND	4.5 V	GND	"		"										"				
115										"											A_3	-0.4	-1.5	V
116										"											A_2	"	"	"
117										"											A_1	"	"	"
118										"											A_0	"	"	"
119										"											I_6	"	"	"
120										"											I_8	"	"	"
121										"											I_7	"	"	"
122										"											RAM_3	"	"	"
123										"											RAM_0	"	"	"
124										"											I_0	"	"	"
125										"											I_1	"	"	"
126										"											I_2	"	"	"
127										"											$\overline{CP}$	"	"	"
128										"											Q_3	"	"	"
129										"											B_0	"	"	"
130										"											B_1	"	"	"
131										"											B_2	"	"	"
132										"											B_3	"	"	"
133	-18 mA									"											Q_0	"	"	"
134		-18 mA								"											D_3	"	"	"
135			-18 mA							"											D_2	"	"	"
136				-18 mA						"											D_1	"	"	"
137					-18 mA					"											D_0	"	"	"
138						-18 mA				"											I_3	"	"	"
139							-18 mA			"											I_5	"	"	"
140								-18 mA		"											I_4	"	"	"
141									-18 mA	"											C_n	"	"	"
142										"										-18 mA	$\overline{OE}$	"	"	"

See footnotes at end of table.

1/ Unless otherwise specified, values of terminal conditions are in volts.

2/ This step is a set-up for subsequent tests. (No measurement at this step).

3/ Apply clock as shown at 150 ns minimum after all other inputs are applied 

4/ V_{CC} = 4.5 V and 5.5 V.

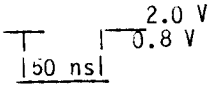
5/ Apply clock as shown at 150 ns minimum after all other inputs are applied 

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11). 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals Case Q Input under test	Measurement terminals Case Q Output under test	Measurement terminals Case Z Input under test	Measurement terminals Case Z Output under test	Test limits Subgroup 9 T_C = 25°C Min	Test limits Subgroup 9 T_C = 25°C Max	Test limits Subgroup 10 T_C = 125°C Min	Test limits Subgroup 10 T_C = 125°C Max	Test limits Subgroup 11 T_C = -55°C Min	Test limits Subgroup 11 T_C = -55°C Max	Unit
t_{PHL1} t_{PLH1}	143	7		1-4	36-39	38-41	33-36		53		53		53	ns
t_{PHL2} t_{PLH2}	144	"		1-4	31	38-41	28		53		53		53	"
t_{PHL3} t_{PLH3}	145	"		1-4	33	38-41	30		53		53		53	"
t_{PHL4} t_{PLH4}	146	"		1-4	32, 35	38-41	29, 32		49		49		49	"
t_{PHL5} t_{PLH5}	147	"		1-4	11	38-41	7		53		53		53	"
t_{PHL6} t_{PLH6}	148	"		1-4	34	38-41	31		53		53		53	"
t_{PHL7} t_{PLH7}	149	"		1-4	8, 9	38-41	3, 5		53		53		53	"
t_{PHL8} t_{PLH8}	150	"		17-20	36-39	14-17	33-36		53		53		53	"
t_{PHL9} t_{PLH9}	151	"		17-20	31	14-17	28		53		53		53	"

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals				Test limits						Unit
				Case Q		Case Z		Subgroup 9 T_C = 25°C		Subgroup 10 T_C = 125°C		Subgroup 11 T_C = -55°C		
				Input under test	Output under test	Input under test	Output under test	Min	Max	Min	Max	Min	Max	
t_{PHL10} t_{PLH10}	152	7		17-20	33	14-17	30		53		53		53	ns
t_{PHL11} t_{PLH11}	153	"		17-20	32, 35	14-17	29, 32		49		49		49	"
t_{PHL12} t_{PLH12}	154	"		17-20	11	14-17	7		53		53		53	"
t_{PHL13} t_{PLH13}	155	"		17-20	34	14-17	31		53		53		53	"
t_{PHL14} t_{PLH14}	156	"		17-20	8, 9	14-17	3, 5		53		53		53	"
t_{PHL15} t_{PLH15}	157	"		22-25	36, 39	19-22	33, 36		42		42		42	"
t_{PHL16} t_{PLH16}	158	"		22-25	31	19-22	28		42		42		42	"
t_{PHL17} t_{PLH17}	159	"		22-25	33	19-22	30		42		42		42	"
t_{PHL18} t_{PLH18}	160	"		22-25	32, 35	19-22	29, 32		40		40		40	"
t_{PHL19} t_{PLH19}	161	"		22-25	11	19-22	7		45		45		45	"

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals				Test limits						Unit
				Case Q		Case Z		Subgroup 9 T_C = 25°C		Subgroup 10 T_C = 125°C		Subgroup 11 T_C = -55°C		
				Input under test	Output under test	Input under test	Output under test	Min	Max	Min	Max	Min	Max	
t_{PHL20} t_{PLH20}	162	7		22-25	34	19-22	31		42		42		42	ns
t_{PHL21} t_{PLH21}	163	"		22-25	8, 9	19-22	3, 5		42		42		42	"
t_{PHL22} t_{PLH22}	164	"		22-25	36-39	19-22	33, 36		42		42		42	"
t_{PHL23} t_{PLH23}	165	"		22-25	31	19-22	28		42		42		42	"
t_{PHL24} t_{PLH24}	166	"		22-25	11	19-22	7		45		45		45	"
t_{PHL25} t_{PLH25}	167	"		22-25	8, 9	19-22	3, 5		42		42		42	"
t_{PHL26} t_{PLH26}	168	"		29	36-39	26	33-36		30		30		30	"
t_{PHL27} t_{PLH27}	169	"		29	31	26	28		30		30		30	"
t_{PHL28} t_{PLH28}	170	"		29	33	26	30		25		25		25	"

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals				Test limits						Unit
				Case Q		Case Z		Subgroup 9 T_C = 25°C		Subgroup 10 T_C = 125°C		Subgroup 11 T_C = -55°C		
				Input under test	Output under test	Input under test	Output under test	Min	Max	Min	Max	Min	Max	
t_{PHL29} t_{PLH29}	171	7		29	11	26	7		33		33		33	ns
t_{PHL30} t_{PLH30}	172	"		29	34	26	31		30		30		30	"
t_{PHL31} t_{PLH31}	173	"		29	8, 9	26	3, 5		33		33		33	"
t_{PHL32} t_{PLH32}	174	"		12-14	36, 39	8-10	33, 35		45		45		45	"
t_{PHL33} t_{PLH33}	175	"		12-14	31	8-10	28		45		45		45	"
t_{PHL34} t_{PLH34}	176	"		12-14	33	8-10	30		45		45		45	"
t_{PHL35} t_{PLH35}	177	"		12-14	32, 35	8-10	29, 32		50		50		50	"
t_{PHL36} t_{PLH36}	178	"		12-14	11	8-10	7		49		49		49	"
t_{PHL37} t_{PLH37}	179	"		12-14	34	8-10	31		45		45		45	"

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals				Test limits						Unit
				Case Q		Case Z		Subgroup 9 T_C = 25°C		Subgroup 10 T_C = 125°C		Subgroup 11 T_C = -55°C		
				Input under test	Output under test	Input under test	Output under test	Min	Max	Min	Max	Min	Max	
t_{PHL38} t_{PLH38}	180	7		12-14	8, 9	8-10	3, 5		45		45		45	ns
t_{PHL39} t_{PLH39}	181	"		26-28	36, 39	23-25	33-36		45		45		45	"
t_{PHL40} t_{PLH40}	182	"		26-28	31	23-25	28		45		45		45	"
t_{PHL41} t_{PLH41}	183	"		26-28	33	23-25	30		45		45		45	"
t_{PHL42} t_{PLH42}	184	"		26-28	32, 35	23-25	29, 32		45		45		45	"
t_{PHL43} t_{PLH43}	185	"		26-28	11	23-25	7		45		45		45	"
t_{PHL44} t_{PLH44}	186	"		26-28	34	23-25	31		45		45		45	"
t_{PHL45} t_{PLH45}	187	"		26-28	8, 9	23-25	3, 5		45		45		45	"
t_{PHL46} t_{PLH46}	188	"		5-7	36-39	1,2,42	33-36		35		35		35	"

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals				Test limits						Unit
				Case Q		Case Z		Subgroup 9 T_C = 25°C		Subgroup 10 T_C = 125°C		Subgroup 11 T_C = -55°C		
				Input under test	Output under test	Input under test	Output under test	Min	Max	Min	Max	Min	Max	
t_{PHL47} t_{PLH47}	189	7		1-4	36-39	38-41	33-36		45		45		45	ns
t_{PHL48} t_{PLH48}	190	"		15	36-39	11	33-36		45		45		45	"
t_{PHL49} t_{PLH49}	191	"		15	31	11	28		45		45		45	"
t_{PHL50} t_{PLH50}	192	"		15	33	11	30		45		45		45	"
t_{PHL51} t_{PLH51}	193	"		15	32, 35	11	29, 32		45		45		45	"
t_{PHL52} t_{PLH52}	194	"		15	11	11	7		45		45		45	"
t_{PHL53} t_{PLH53}	195	"		15	34	11	31		45		45		45	"
t_{PHL54} t_{PLH54}	196	"		15	8, 9	11	3, 5		45		45		45	"
t_{PHL55} t_{PLH55}	197	"		15	16, 21	11	13, 18		35		35		35	"

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals Case Q Input under test	Case Q Output under test	Case Z Input under test	Case Z Output under test	Test limits Subgroup 9 T_C = 25°C Min	Subgroup 9 T_C = 25°C Max	Subgroup 10 T_C = 125°C Min	Subgroup 10 T_C = 125°C Max	Subgroup 11 T_C = -55°C Min	Subgroup 11 T_C = -55°C Max	Unit
t_{PZL1} t_{PZH1}	198	7		40	36, 39	37	33-35		30		30		30	ns
t_{PZL2} t_{PZH2}	199	"		6	8, 9	1	3, 5		35		35		35	"
t_{PZL3} t_{PZH3}	200	"		6	16, 21	1	13, 18		35		35		35	"
t_{PLZ1} t_{PHZ1}	201	"		40	36-39	37	33-36		30		30		30	"
t_{PLZ2} t_{PHZ2}	202	"		6	8, 9	1	3, 5		34		34		34	"
t_{PLZ3} t_{PHZ3}	203	"		6	16, 21	1	13, 18		34		34		34	"

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals Case Q Input verified	Case Q Output under test	Case Z Input verified	Case Z Output under test	Test limits Subgroup 9 T_C = 25°C Min	Subgroup 9 T_C = 25°C Max	Subgroup 10 T_C = 125°C Min	Subgroup 10 T_C = 125°C Max	Subgroup 11 T_C = -55°C Min	Subgroup 11 T_C = -55°C Max	Unit
V_{OL}	204	"	t_{SHL1}	1-4	8,9,11, 31-39	38-41	3,5,7, 28-36				.08		.08	V
V_{OH}			t_{SLH1}							2.0	"	2.0	"	
V_{OL}	205	"	t_{SHL2}	1-4	8,9,11, 31-39	38-41	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH2}							"	"	"	"	
V_{OL}	206	"	t_{SHL3}	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH3}							"	"	"	"	
V_{OL}	207	"	t_{SHL4}	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH4}							"	"	"	"	

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals Case Q Input verified	Measurement terminals Case Q Output under test	Measurement terminals Case Z Input verified	Measurement terminals Case Z Output under test	Test limits Subgroup 9 T_C = 25°C Min	Subgroup 9 T_C = 25°C Max	Subgroup 10 T_C = 125°C Min	Subgroup 10 T_C = 125°C Max	Subgroup 11 T_C = -55°C Min	Subgroup 11 T_C = -55°C Max	Unit
V_{OL}	208	7	t_{SHL5}	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36			2.0	0.8	2.0	0.8	V
V_{OH}			t_{SLH5}							"	"	"	"	
V_{OL}	209	"	t_{SHL6}	22-25	8,9,11, 31-39	19-22	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH6}							"	"	"	"	
V_{OL}	210	"	t_{SHL7}	22-25	8,9,11, 31-39	19-22	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH7}							"	"	"	"	
V_{OL}	211	"	t_{SHL8}	29	8,9,11, 31-39	26	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH8}							"	"	"	"	
V_{OL}	212	"	t_{SHL9}	12-14	8,9,11, 31-39	8-10	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH9}							"	"	"	"	
V_{OL}	213	"	t_{SHL10}	26-28	8,9,11, 31-39	23-25	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH10}							"	"	"	"	
V_{OL}	214	"	t_{SHL11}	5-7	8,9,11, 31-39	1,2,42	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH11}							"	"	"	"	
V_{OL}	215	"	t_{SHL12}	16-21	11,16,21, 31-39	13,18	7,13,18, 28-36			"	"	"	"	"
V_{OH}			t_{SLH12}							"	"	"	"	
V_{OL}	216	"	t_{SHL13}	8, 9	8,9,11, 31-39	3, 5	3,5,7, 28-36			"	"	"	"	"
V_{OH}			t_{SLH13}							"	"	"	"	

See footnotes at end of table.

TABLE IIIB. Group A tests - (subgroups 9, 10, and 11) - Continued. 1/2/3/4/6/

Symbol	Test number	Waveform 5/ figure	Parameter verified	Measurement terminals Case Q Input verified	Case Q Output under test	Case Z Input verified	Case Z Output under test	Test limits Subgroup 9 T_C = 25°C Min	Subgroup 9 T_C = 25°C Max	Subgroup 10 T_C = 125°C Min	Subgroup 10 T_C = 125°C Max	Subgroup 11 T_C = -55°C Min	Subgroup 11 T_C = -55°C Max	Unit
V_{OL}	217	7	t_{HHL1}	1-4	3,9,11, 31-39	38-41	3,5,7, 28-36				0.5		0.5	V
V_{OH}			t_{HLH1}							2.4		2.4		
V_{OL}	218	"	t_{HHL2}	17-20	8,9,11, 31-39	14-17	3,5,7, 28-36				0.5		0.5	"
V_{OH}			t_{HLH2}							2.4		2.4		
V_{OL}	219	"	t_{HHL3}	22-25	8,9,11, 31-39	19-22	3,5,7, 28-36				0.5		0.5	"
V_{OH}			t_{HLH3}							2.4		2.4		
V_{OL}	220	"	t_{HHL4}	29	8,9,11, 31-39		3,5,7, 28-36				0.5		0.5	"
V_{OH}			t_{HLH4}							2.4		2.4		
V_{OL}	221	"	t_{HHL5}	5-7, 12-14, 26-38	11, 31-39	1,2, 8-10, 23-25,42	7,28-36				0.5		0.5	"
V_{OH}			t_{HLH5}							2.4		2.4		
V_{OL}	222	"	t_{HHL6}	16-21	11, 31-39	13-18	7,28-36				0.5		0.5	"
V_{OH}			t_{HLH6}							2.4		2.4		
V_{OL}	223	"	t_{HHL7}	8, 9	11, 31-39	3, 5	7,28-36				0.5		0.5	"
V_{OH}			t_{HLH7}							2.4		2.4		

1/ V_{CC} = 4.5 V and 5.5 V for subgroups 9, 10, and 11.

2/ Where propagation delay tests for subgroups 9, 10, and 11 indicate a group of pins and two or more propagation delays are specified for a test, only the readings for the pin(s) with the worst case minimum and maximum delays require recording.

3/ Variables data shall be taken for subgroups 9, 10, and 11, only during initial qualification and after process or design changes.

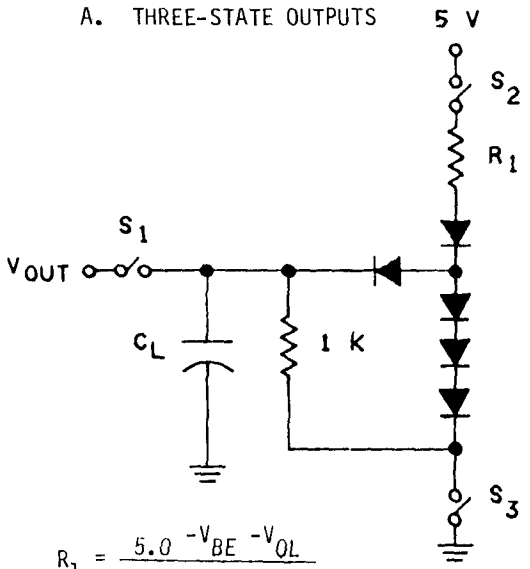
4/ Minimum and maximum limits for propagation delay tests are used only when taking variables data. Maximum limit only is used during 100 percent testing.

5/ Figure 7, represents the timing diagrams associated with subgroups 7, 8, 9, 10, and 11.

6/ All subgroups 9, 10, and 11 tests are run concurrently with subgroups 7 and 8.

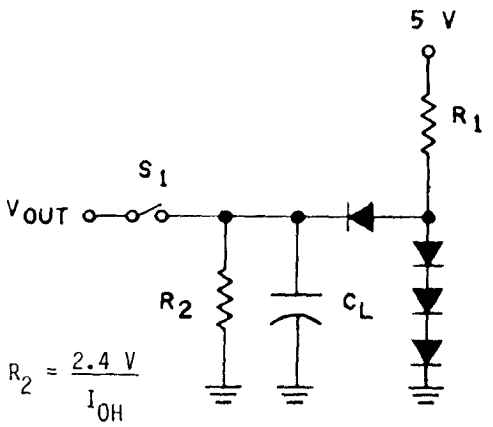
DEVICE TYPE 01

A. THREE-STATE OUTPUTS



$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1K}$$

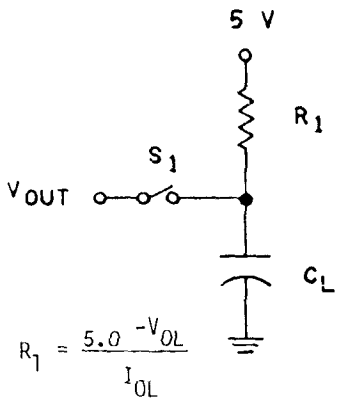
B. NORMAL OUTPUTS



$$R_2 = \frac{2.4\ V}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

C. OPEN-COLLECTOR OUTPUTS

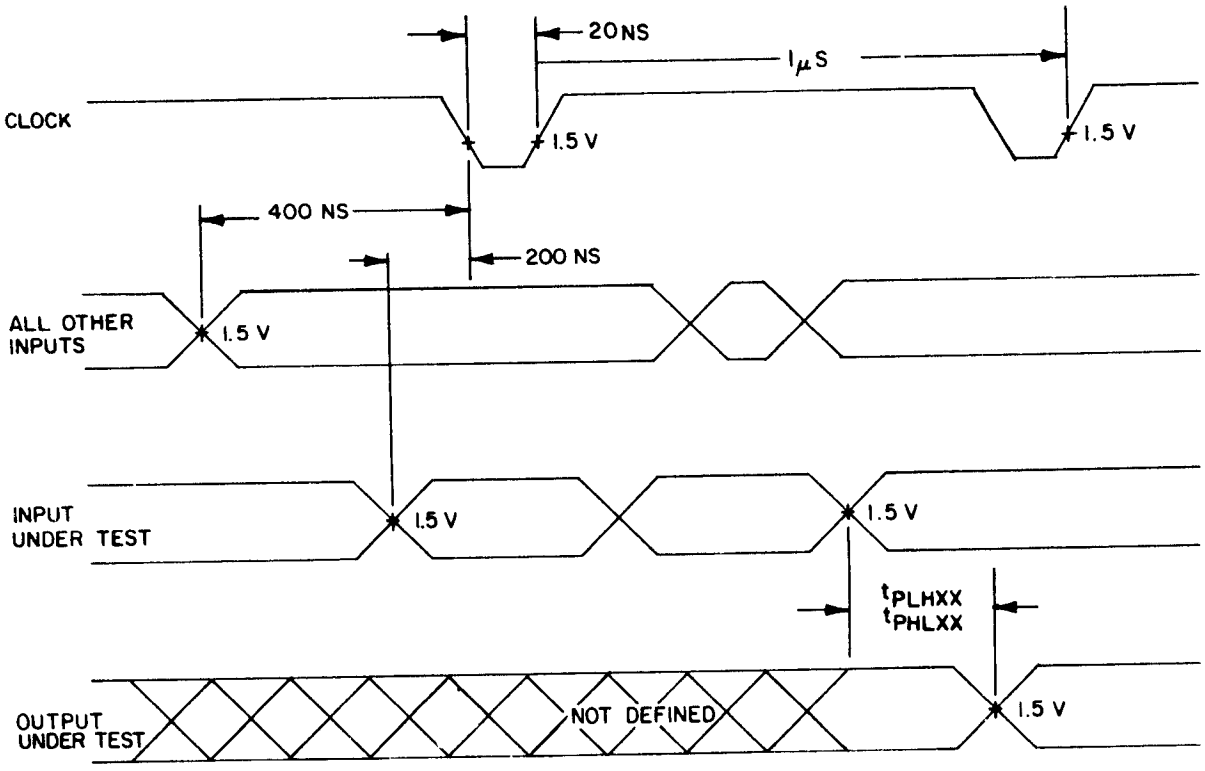


$$R_1 = \frac{5.0 - V_{OL}}{I_{OL}}$$

Functional Pin	Test Circuit	R_1	R_2
$\overline{RAM}_3$	A	560	1K
$\overline{RAM}_0$	A	560	1K
F = 0	C	270	--
Q_3	A	560	1K
Q_0	A	560	1K
F_3	B	620	3.9K
G	B	220	1.5K
C_{n+4}	B	360	2.4K
$\overline{OVR}$	B	470	3K
P	B	470	3K
Y_{0-3}	A	220	1K

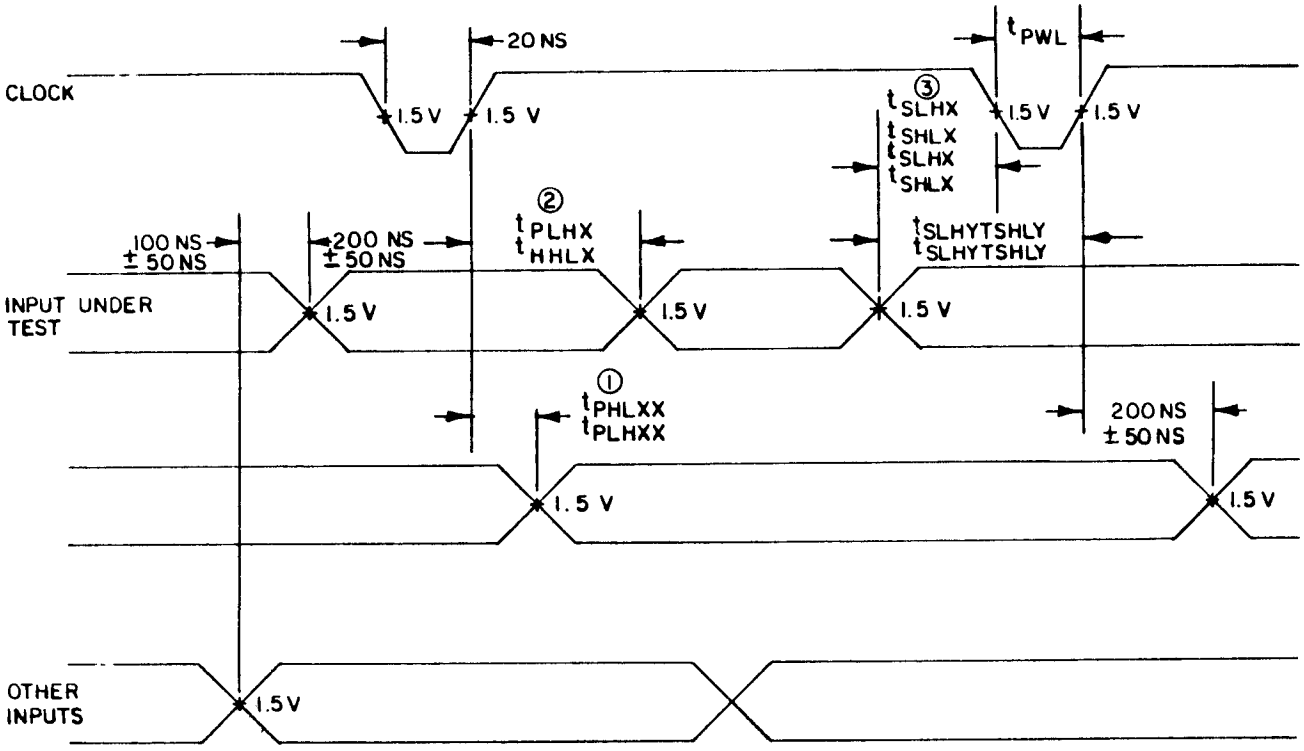
NOTES:
1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable test.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
   S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. C_L = 5.0 pF for output disable tests.

FIGURE 6. Switching time test circuit loads.



NOTE: For t_{PLHXX}, t_{PHLXX}, XX equals 01 through 47.

FIGURE 7. Timing waveforms.



NOTES:
1. For t_{PHLXX} and t_{PLHXX}, XX = 48 through 55. See table I for values.
2. For t_{HHLX} and t_{HLHX}, X = 1 through 7. See table I for values.
3. For $t_{SHLX \text{ or } Y}$ and $t_{SLHX \text{ or } Y}$, X = 2,4,5, Y = 1,3,6,7,8,9,10,11,12, and 13. See table I for values.

FIGURE 7. Timing waveforms - Continued.

4.3 Qualification inspection. Qualification inspection is not required.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Electrical test requirements shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Variables data shall be recorded and submitted to the qualifying activity for subgroups 9, 10, and 11 for initial qualifiction and after process or design changes only.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. Electrical test requirements shall be as specified in table II herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Constant acceleration use in test condition D of method 2001 of MIL-STD-883.

c. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition C, using the circuit shown on figure 5, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1,000 hours except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logisitic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

GND	Ground zero voltage potential.
I_{IN}	Current flowing into an input terminal.
V_{IC}	Input clamp voltage.
V_{IN}	Voltage level at an input terminal.

PIN DEFINITIONS

A_0-3 — The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_0-3 — The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_0-8 — The nine instruction control lines used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 — A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the processor. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 — Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_0-3 — Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the processor, D_0 is the LSB.

F_3 — This output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. It is noninverted with respect to the sign bit output Y_3.

Y_{0-3} — The four data outputs of the processor. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ — Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}$, $\overline{G}$ — The carry generate and propagate outputs of the ALU. These signals are used for carry-lookahead.

OVR — Overflow. This pin is logically the exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 — This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

C_n — The carry-in to the ALU.

C_{n+4} — The carry-out of the ALU.

CP — The clock input of the processor. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Functional pattern tests. Table IV is not printed herein because of its extreme length and pattern complexity. The test program output should be obtained in a form compatible with test system architecture. The device manufacturer may be consulted for information on obtaining such output.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	2901C

6.7 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

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