MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, N-CHANNEL, SILICON GATE MONOLITHIC 8 BIT MICROPROCESSOR (FIXED INSTRUCTION)

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for a monolithic N-channel, silicon gate microprocessor. Two product assurance classes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	8-bit fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
Q	D-5 (40-lead, 9/16" x 2-1/16"), dual-in-line package

1.3 Absolute maximum ratings.

V_{CC} supply voltage (with respect to V_{BB})	-0.3 V dc to +20 V dc
V_{DD} supply voltage (with respect to V_{BB})	-0.3 V dc to +20 V dc
V_{SS} supply voltage (with respect to V_{BB})	-0.3 V dc to +20 V dc
Input and output voltage (with respect to V_{BB})	-0.3 V dc to +20 V dc
Storage temperature range	-65°C to +150°C
Power dissipation:	
T_C = -55°C	1.7 W
T_C = 125°C	1.2 W
Lead temperature (soldering, 5 seconds)	270°C
Maximum junction temperature at T_C = 125°C 1/	T_J = 150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case Q	(See MIL-M-38510 appendix C)

1/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions per method 5009 of MIL-STD-883.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.4 Recommended operating conditions.

Supply voltage (V_{BB}) - - - - - - - - - - - - - - - - -	-4.5 V dc to -5.5 V dc
Supply voltage (V_{CC}) - - - - - - - - - - - - - - - - -	+4.5 V dc to +5.5 V dc
Supply voltage (V_{DD}) - - - - - - - - - - - - - - - - -	+10.8 V dc to 13.2 V dc
Supply voltage (V_{SS}) - - - - - - - - - - - - - - - - -	0 V dc
High level input voltage:	
(logic inputs) - - - - - - - - - - - - - - - - - -	3.0 V dc to (V_{CC} + 1.0 V dc)
(clock inputs) - - - - - - - - - - - - - - - - - -	8.5 V dc to (V_{DD} + 1.0 V dc)
Low level input voltage (logic and clock inputs) - -	(V_{SS} - 1.0 V dc) to 0.8 V dc
Minimum high-level output voltage (V_{OH}) - - - - - -	3.7 V dc
Maximum low-level output voltage (V_{OL}) - - - - - - -	0.45 V dc
Frequency of operation - - - - - - - - - - - - - - - - -	0.5 to 2 MHz
Case operating temperature range (T_C) - - - - - - - -	-55°C to +125°C

INDEX

		Page
TABLE I.	Electrical performance characteristics - - - -	3
II.	Electrical test requirements - - - - - - - - -	9
III.	Group A inspection - - - - - - - - - - - - - - -	20
IVA.	Input conditions for table III - - - - - - - - -	41
IVB.	Output conditions for table III- - - - - - - - -	43
V.	Vectors 00001 thru 11,761 - - - - - - - - - - -	56
VI.	Microprocessor instructions - - - - - - - - - -	59

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Departments of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Fig	Limits Min	Limits Max	Units
High-level output voltage, all outputs except SYNC	V_{OH}	V_{DD} = +10.8 V I_{OH} = -150 μA V_{BB} = -5.5, V_{CC} = +4.5		3.7		V
Low-level output voltage, all outputs	V_{OL}	V_{DD} = +10.8 V I_{OL} = 1.9 mA V_{BB} = -5.5, V_{CC} = 4.5			0.45	V
High-level high-impedance output current D_0-D_7, A_0-A_{15}	I_{ZH1}	V_O = +5.5 V T_C = +125°C, +25°C V_{BB} = -4.5, V_{CC} = +5.5 V_{DD} = +10.8			10	μA
Low-level high-impedance output current D_0-D_7, A_0-A_{15}	I_{ZL1}	V_O = 0.45 V T_C = +125°C, +25°C V_{BB} = -4.5, V_{CC} = +5.5 V_{DD} = 13.2			-100	μA
High-level input current for clock inputs, reset, hold, int, and ready	I_{IH1}	Logic Clock V_{IN} = 5.5, V_{IN} = 13.2 V_{IN} = GND V_{BB} = -4.5 V_{CC} = +5.5 V_{DD} = +13.2 T_C = +125°C, +25°C			10	μA
Low-level input current for clock inputs, reset, hold, int, and ready	I_{IL1}	V_{IN} = GND V_{BB} = -4.5, V_{CC} = +5.5 V_{DD} = +13.2 T_C = 125°C, +25°C			-10	μA
Low-level input current, data bus in input mode, D_0-D_7	I_{IL2}	V_{IN} = 0.8 V V_{BB} = -4.5, V_{CC} = +5.5 V_{DD} = +13.2 T_C = +125°C, +25°C			-100	μA
High-level input current, data bus in input mode D_0-D_7	I_{IH2}	V_{BB} = -4.5, V_{CC} = +5.5 V_{DD} = 13.2 V_{in} = 5.5, T_C = 125°, 25°C			+100	μA
Input clamp voltage	V_{IC}	(Pos.) V_{in} = 0.4 V			3.0	mA
		(Neg.) I_O = -100 μA			-2.0	V

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Fig	Limits Min	Limits Max	Units
Negative 5 V power supply current	I_{BB}	f = 2.0 MHz V_{BB} = -4.5 V V_{CC} = +5.5 V V_{DD} = +13.2 V			-1.0	mA
Positive 5 V power supply current	I_{CC}				120	mA
Positive 12 V power supply current	I_{DD}				85	mA
Input capacitance $Ø_1$, $Ø_2$	C_I	f = 1 MHz, T_C = 25°C From input pins to all other pins		2	30	pF
Input capacitance ready, hold, int. D_0-D_7, reset	C_I			2	15	pF
Output capacitance A_0-A_{15}, Sync, DBIN, WAIT, WR, HLDA, INTE	C_O			2	20	pF
Clock pulse width Ø1	$t_{Ø1}$		5	60		ns
Clock pulse width Ø2	$t_{Ø2}$		5	220		ns
Time between Ø1 leading edge and Ø2 leading edge	t_{SLH7}		5	80		ns
Time between Ø1 trailing edge and Ø2 leading edge	t_{SLH6}		5	0		ns
Time between Ø2 trailing edge and Ø1 leading edge	t_{SHL8}		5	80		ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Fig	Limits Min	Limits Max	Units
Ready setup time to Ø2	t_{SLH1}		10	120		ns
	t_{SHL1}		12,13	120		ns
Data setup time to Clock Ø1	t_{SLH2}		12	30		ns
	t_{SHL2}		12	30		ns
Data setup time to Clock Ø2	t_{SLH3}		12	130		ns
	t_{SHL3}		12	130		ns
INT input setup time during Ø1 or Ø2, INT not valid	t_{SLH4}		7,8	120		ns
	t_{SHL4}		7,8	120		ns
Hold input setup time to Ø2	t_{SHL5}		11	140		ns
	t_{SLH5}		9	140		ns
Reset input setup time to Ø1	t_{SLH9}		14	75		ns
Data hold time from Ø2	t_{HHL2}		12	1/ 50		ns
	t_{HLH2}		12	1/ 50		ns
Hold and ready hold time, INT input hold time during Ø1 or Ø2, INT valid	t_{HHL1}		7,8, 9,10	0		ns
Hold and ready hold time, INT input hold time during Ø1 or Ø2, INT not valid	t_{HLH1}		11, 7,8, 12,13	0		ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq TC \leq +125^{\circ}C$	Fig	Limits Min	Limits Max	Units
Reset input hold time to Ø1	t_{HHL3}		14		75	ns
Frequency of operation	F	See figure 15	5	0.500	2.08	MHz
Data and status output delay from Ø2: D_0-D_7 Data And Status Valid	t_{PLH1}		12,13		220	ns
	t_{PHL1}		12,13		220	ns
	t_{PZH1}		12,13		220	ns
	t_{PZL1}		12,13		220	ns
Delay for data bus to enter input mode D_0-D_7	t_{PHZ1}		12		150	ns
	t_{PLZ1}		12		150	ns
Delay to float during hold from Ø2 A_0-A_{15}, D_0-D_7	t_{PLZ2}		9		130	ns
	t_{PHZ2}		9		130	ns
DBIN output delay from Ø2	t_{PLH3}		12	25	150	ns
	t_{PHL3}		12	25	150	ns
Delay to float during hold from HLDA A_0-A_{15}, D_0-D_7	t_{PHZ3}		9,11	2/		ns
	t_{PLZ3}					
SYNC, $\overline{WR}$, WAIT, $\overline{HLDA}$ output delay	t_{PLH4}		12		140	ns
	t_{PHL4}		13		140	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$	Fig	Limits Min	Limits Max	Units
Address and data delay to float during mold from $\overline{WR}$ A_0-A_{15}, D_0-D_7	t_{PHZ4}		9	3/		ns
	t_{PLZ4}		9	3/		ns
INTE output delay from Ø2	t_{PHL5}		7		200	ns
	t_{PLH5}		16		200	ns
Address valid after DBIN during HLDA	t_{PHZ5}		11	-20		ns
	t_{PLZ5}		11	-20		ns
Address output delay from Ø2 address valid A_0-A_{15}	t_{PLH6}		13		200	ns
	t_{PHL6}		13		200	ns
Output data stable prior to $\overline{WR}$ 1 D_0-D_7	t_{PLH7}		13	4/		ns
	t_{PHL7}		13	4/		ns
Address stable prior to $\overline{WR}$ A_0-A_{15}	t_{PLH8}		13	5/		ns
	t_{PHL8}		13	5/		ns
Output data, address stable from $\overline{WR}$ (not HLDA) D_0-D_7, A_0-A_{15}	t_{PHL9}		13	6/		ns
	t_{PLH9}		13	6/		ns

Notes for table I. The following equations determine the minimum limits for the noted table I delay measurements (where $t_{TLHØ2}$ = rise time of Ø2 from 1.0 V to 7.0 V; refer to figure 5).

1/ 50 ns or t_{PHZ1}, whichever is less.

2/ t_{PHZ3} and $t_{PLZ3} = t_{SLH7} + t_{TLHØ2} - 50$ ns.

3/ t_{PHZ4} and $t_{PLZ4} = t_{SLH7} = t_{TLHØ2} - 10$ ns.

4/ t_{PHL7} and $t_{PLH7} = t_{period(clock)} - t_{SLH7} - t_{TLHØ2} - 170$ ns.

5/ t_{PHL8} and $t_{PLH8} = 2t_{period(clock)} - t_{SLH7} - t_{TLHØ2} - 140$ ns.

6/ t_{PHL9} and $t_{PLH9} = t_{SLH7} + t_{TLHØ2} + 10$ ns.

3.2. Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.3 Functional description, terms, and symbols. Functional description, terms, and symbols shall be as specified in 6.6.

3.2.4 Case outline. The case outline shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.4 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

3.7 Microprocessor instructions. The microprocessor instruction shall be as specified in table VI.

3.8 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 107 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) T_A = 125°C minimum.

(2) Use the circuit shown on figure 3, or equivalent.

b. Percent defective allowable (PDA) - The PDA shall be as specified in MIL-M-38510.

c. Interim and final electrical tests shall be as specified in table II, except interim electrical tests prior to burn-in are optional at the description of the manufacturer.

d. Constant acceleration (method 2001 of MIL-STD-883) shall be 20,000 G.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table IIIC) unless otherwise stated	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in) (method 5004) (optional)	1,2,3,7 - (tests 1 thru 72)	1,2,3,7 - (tests 1 thru 72)
Final electrical test parameters (method 5004)	*1,2,3 - (tests 1 thru 72 and 73 thru 159) *7,8	*1,2,3 - (tests 1 thru 72 and 73 thru 159) *7,8
Group A test requirements (method 5005)	*1,2,3,4 1/ 7,8,**12 -(tests 1 thru 159)	*1,2,3,4 1/ 7,8,**12 (tests 1 thru 159)
Group B test requirements	4.5.2	4.5.2
Group B, C, and D end-point electrical parameters (method 5005)	1,2,3 - (tests 1 thru 159) 7,8	1,2,3 - (tests 1 thru 159) 7,8

1/ Test numbers 152 through 186 constitute subgroup 4 and is used for initial qualificaion only (see 4.4.1).

* PDA applies to subgroups 2 (tests 1 thru 72 only) and 7A (see 4.3b).

** Subgroup 12 is defined - table III tests 196 thru 275 and is used for initial qualification only.

4.4.1 Group A inspection. Group A inspection shall consist of the test subgroups and LTPD values shown in table I of method 5005 of MIL-STD-883 and as follows:

a. Electrical test requirements shall be specified in table II.

b. Subgroup 4 (C_I, C_O measurement) shall be performed only for initial qualification and after process or design changes which may affect design capacitance. Tests 152 through 186 shall be performed on 5 devices. Test 10 additional devices with the exception that one test be chosen from each of the following two test groups and performed as representative of the test group. The representative tests that are chosen will be the worst case high measured values taken on the previous units. The two test groups are tests 153-160 (data bus outputs) and 152, 172-186, (address outputs).

c. Subgroup 12 shall be performed only during initial qualification and after process or design changes which may affect design capacitance. Variables data shall be submitted.

d. The LTPD's per subgroup 10 of MIL-STD-883, method 5005, table I shall apply to table III, subgroup 12. Variables data shall be recorded for initial qualification at 125°C as a minimum.

e. Subgroups 5, 6, 9, 10, and 11 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883 and as follows:

a. An additional subgroup shall be added to the group B inspection requirements for class S and B devices and shall consist of the test, conditions and limits specified in 4.5.2. The LTPD for this subgroup shall be 15 for all classes.

b. Constant acceleration (method 2001 of MIL-STD-883) shall be 20,000 G.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
(1) Test condition D, using the circuit shown on figure 3, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration, 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

c. Constant acceleration (method 2001 of MIL-STD-883) shall be 20,000 G.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical tests shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 High-voltage (V_{ZAP}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 600 V from a 50 pF source in the following test sequence.

a. Measure I_{IH} and I_{IL} at one input terminal of the device under test at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} and I_{IL} shall be as specified in table III.

b. Apply the test voltage (V_{ZAP} = 600 V) to the same terminal selected for leakage current measurements. Apply V_{ZAP} in a 2 pulse sequence as follows and in accordance with the test circuit of figure 4.

(1) Input (-) to V_{SS}.

(2) Input (+) to V_{SS}.

c. Within 24 hours repeat the I_{IH} and I_{IL} measurements on the same terminal is performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Computer generated table. Table V, which forms a part of this specification, is not printed herein because of its extreme length; and, even when presented as hard copy, requires conversion to on-line format. When the entire sequence of vector groups is needed for driving devices as part of inspection, a test program output should be obtained in a form compatible with test system architecture (magnetic tape format usually preferred). The preparing activity (or DESC, as its agent) may be consulted for information on obtaining such output. For reference purposes, Rome Air Development Center (RBE-2) and Defense Electronics Supply Center (DESC-ECS) each maintain a limited quantity of dated, hard copy printouts of this table.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.3 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

h. Requirements for "JAN" marking.

6.4 Logistic support. Lead material and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish "C" (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Handling. MOS microprocessors should be handled with certain precautions to avoid damage due to the accumulation of static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility of damage. However, the following handling practices are recommended.

a. Devices should be handled on benches with conductive and grounded surface.

b. Test equipment and tools should be grounded.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive carriers.

e. Avoid use of plastic, rubber, or silk in MOS area.

6.6 Functional description including terms and symbols of I/O and control pins. Abbbreviations, symbols and definitions used herein are defined in MIL-M-38510 and MIL-STD-1313 and as follows:

Clock inputs (Ø1, Ø2). These inputs are the two-phase non-overlapping clocks. They are not TTL compatible.

Address bus (A0-A15). These outputs are three-state bus drivers. This permits the microprocessor to be used in DMA applications. A0 is the least significant bit.

Data bus (D0-D7). The data bus provides bi-directional communication between the processor, memory, and I/O devices for instructions and data transfers. D0 is the least significant bit.

State. The state is the smallest unit of processor activity and is defined as the interval between two successive positive going transitions of the Ø1 clock pulse.

Machine cycle. Each machine cycle may consist of three, four or five states. The processor may require one, two, three, four, or five machine cycles for instruction execution.

SYNC (output). The SYNC output provides a signal to indicate the beginning of each machine cycle.

DBIN (output). The DBIN signal indicates to external circuits that the data bus is in the input mode. This signal should be used to enable the gating of data onto the data bus from memory or I/O.

READY (input). The READY signal indicates to the processor that valid memory or input data is available on the data bus. This signal is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, a READY input is not received, the processor will enter a WAIT state for as long as the READY line is low.

WAIT (output). The wait signal acknowledges that the processor is in a WAIT state.

$\overline{WR}$ (output). The $\overline{WR}$ signal is used for memory WRITE or I/O output control. The data on the data bus is stable while the WR signal is active low ($\overline{WR}$ = 0).

HOLD (input). The HOLD signal requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the address and data bus as soon as the processor has completed its use of these buses for the current machine cycles. It is recognized under the following conditions:

- The processor is in the HALT state
- The processor is in state 2 or state (wait) and the READY signal is active

As a result of entering the HOLD state the ADDRESS BUS (A15-A0) and DATA BUS (D7-D0) will be in their high impedance state. The processor acknowledges its state with the (HLDA) pin.

HLDA (output). The HLDA signal appears in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at:

- State 3 for READ memory or input
- The Clock Period following state 3 for WRITE memory or OUTPUT operation

Device type 01

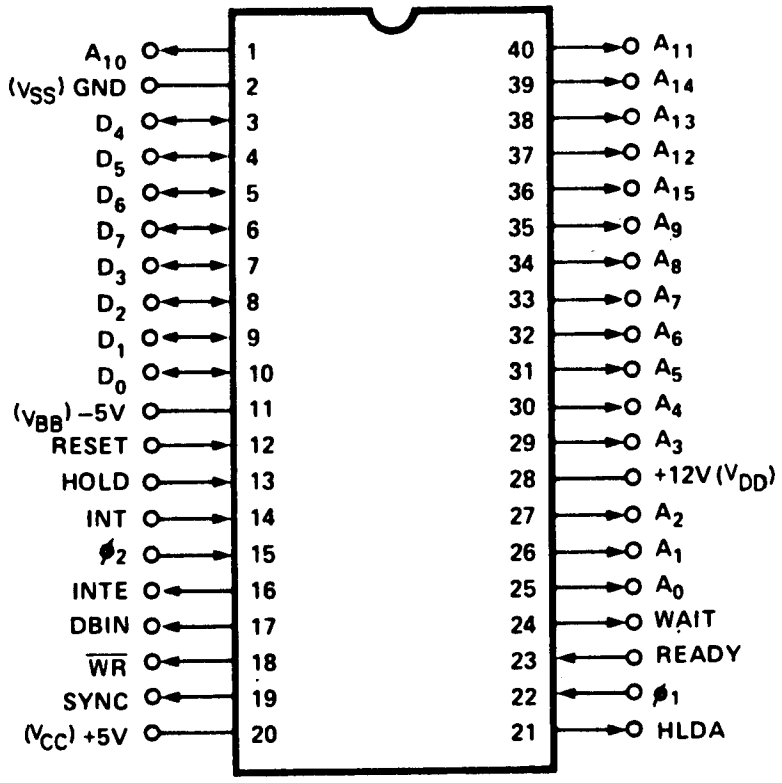


FIGURE 1. Terminal connections.

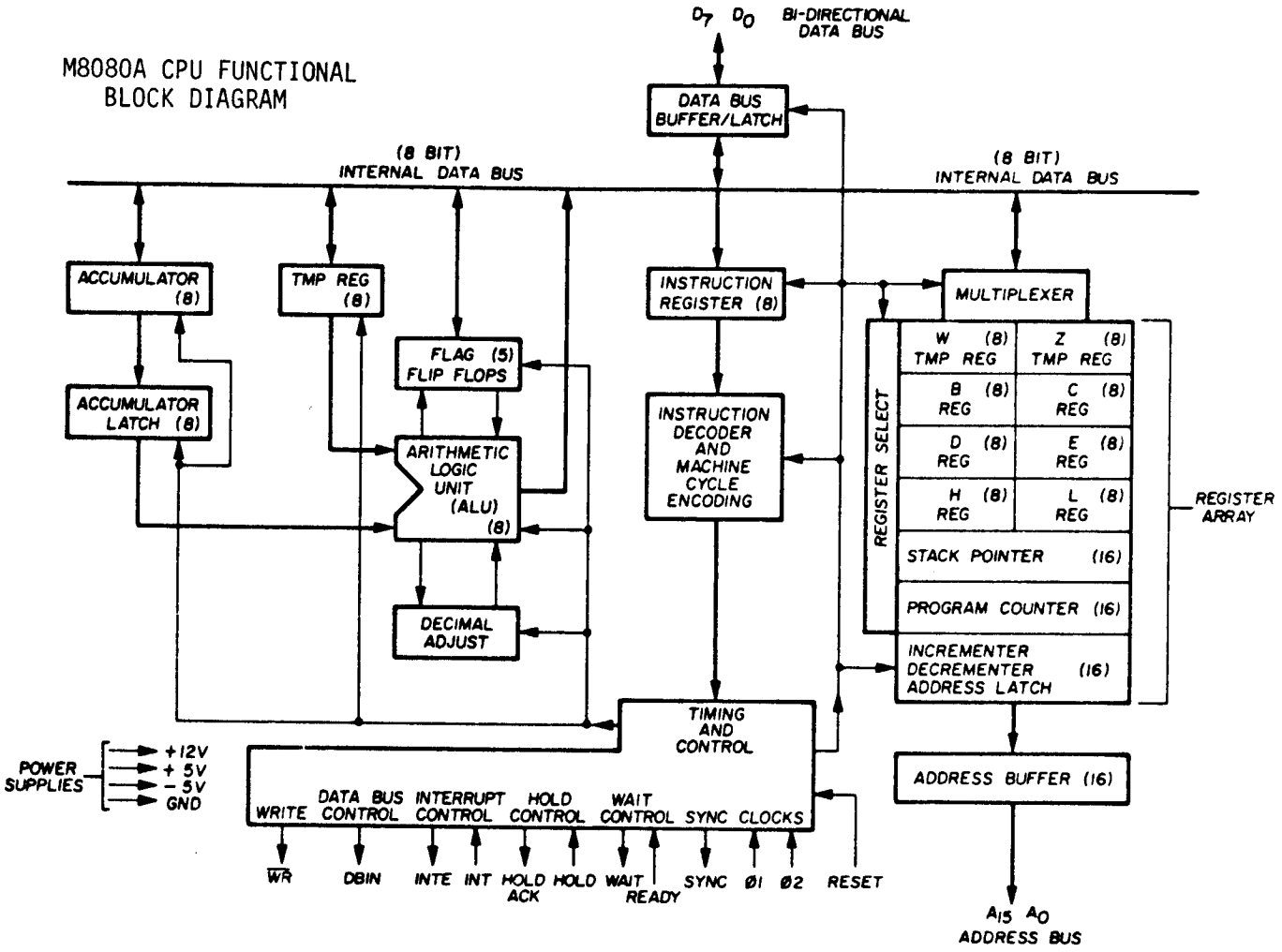
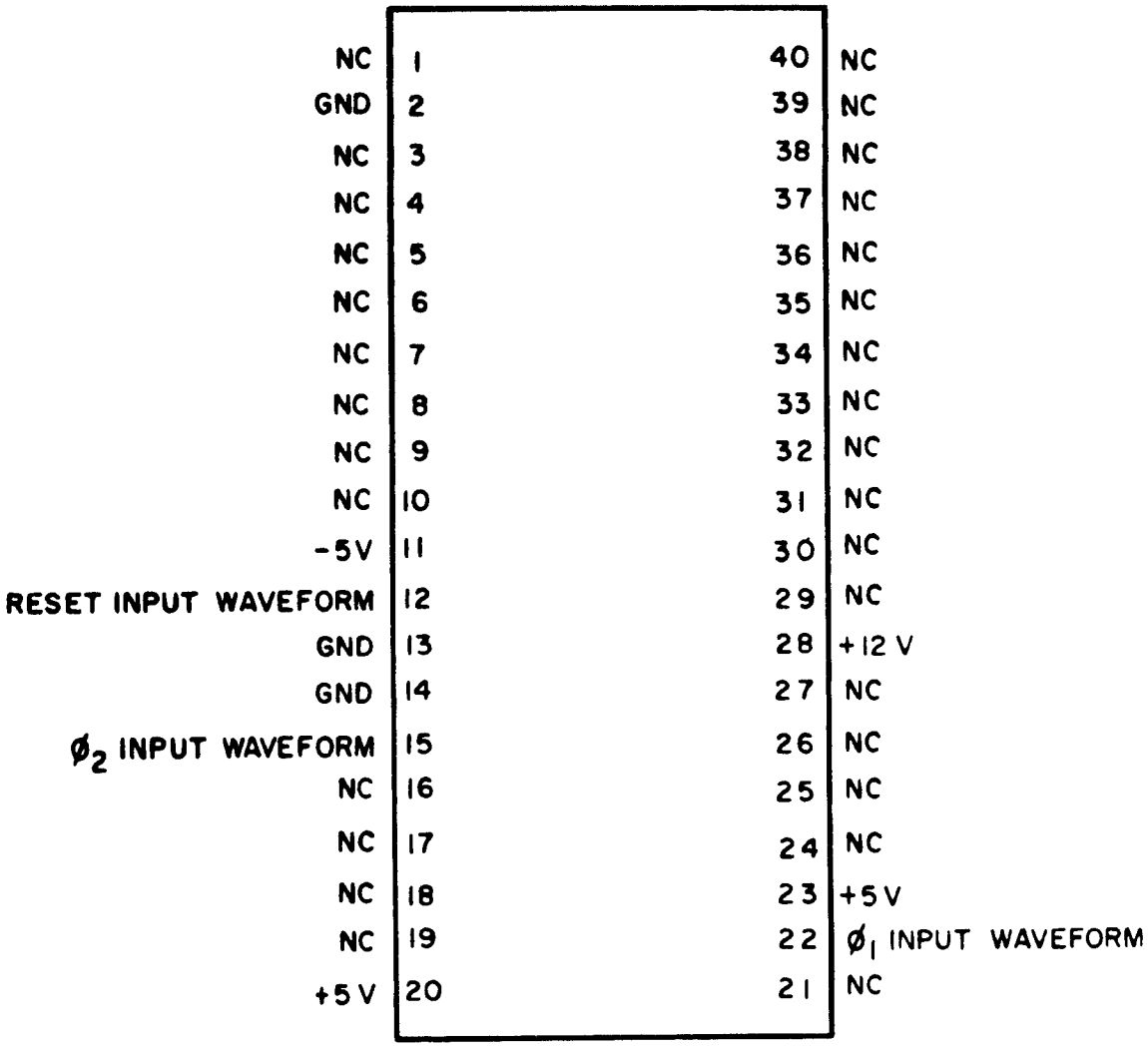
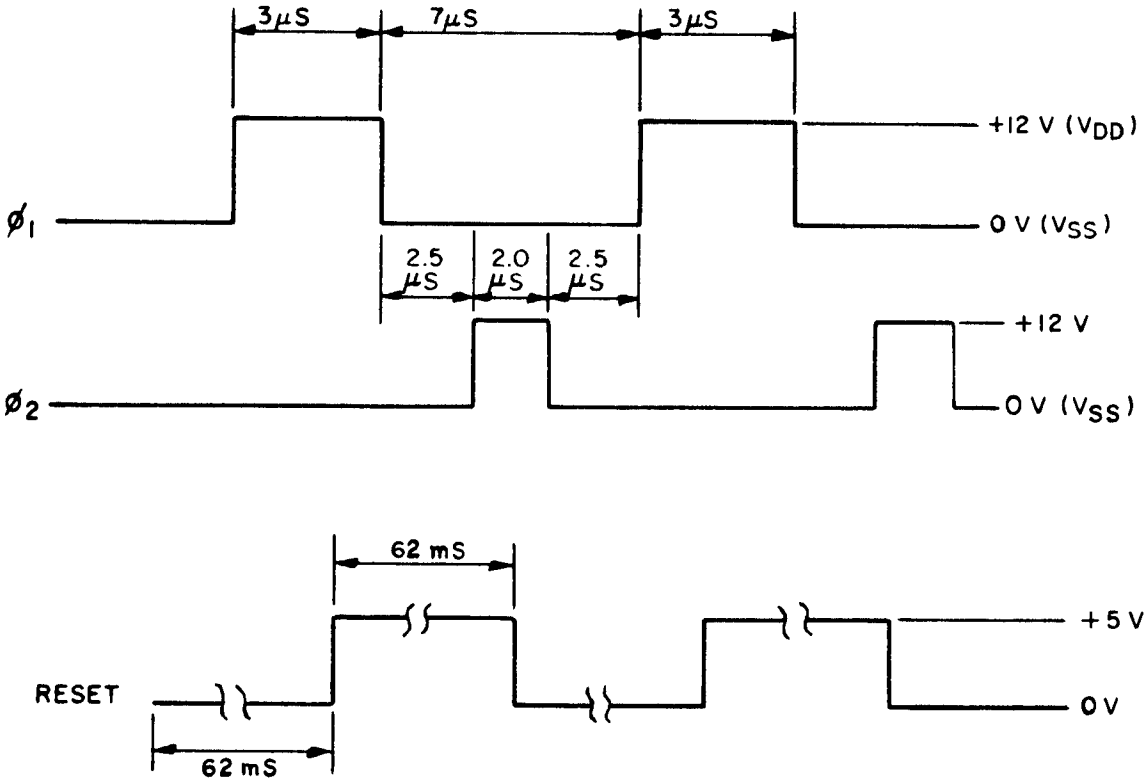


FIGURE 2. Functional block diagram device type 01.



NOTES:
1. CAUTION: All "NC" (no connection) pins should be isolated from device to device.
2. Power supply voltages are indicated in order of power-up sequence:
   V_{BB} = -5 V - 10%
   V_{CC} = +5 V + 10%
   V_{DD} = +12 V + 10%

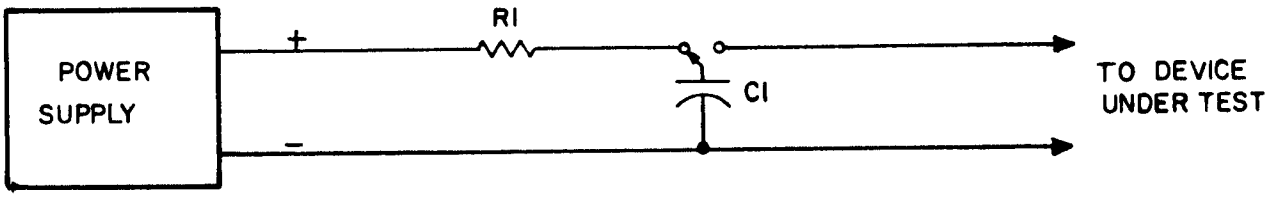
FIGURE 3. Burn-in and operating life test.



NOTES:
1. "RESET" is not synchronized with Ø1 and Ø2.
2. Waveform transition times, t_{TLH} and t_{THL}, are measured from 1.0 V to 8.0 V for clocks and from 0.5 V to 4.5 V for the RESET input. All measurements are with the device under test connected.

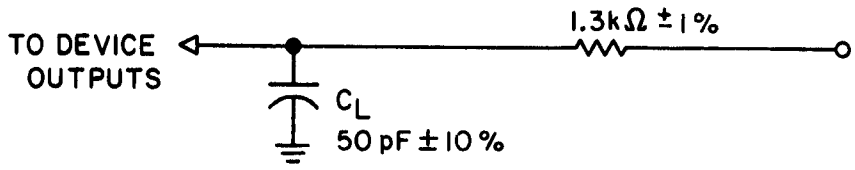
Ø1: $t_{TLH} = t_{THL}$ = 450 ns maximum.
Ø2: $t_{TLH} = t_{THL}$ = 750 ns maximum.
RESET: t_{TLH} = 600 ns maximum.
t_{THL} = 675 ns maximum.

FIGURE 3. Burn-in and operating life test (input waveform) - Continued.



R1 = Appropriate current limiting resistance.
C1 = 50 pF.
V_{zap} = 600 V measured at device input terminal.

FIGURE 4. High voltage (V_{zap}) test circuit.

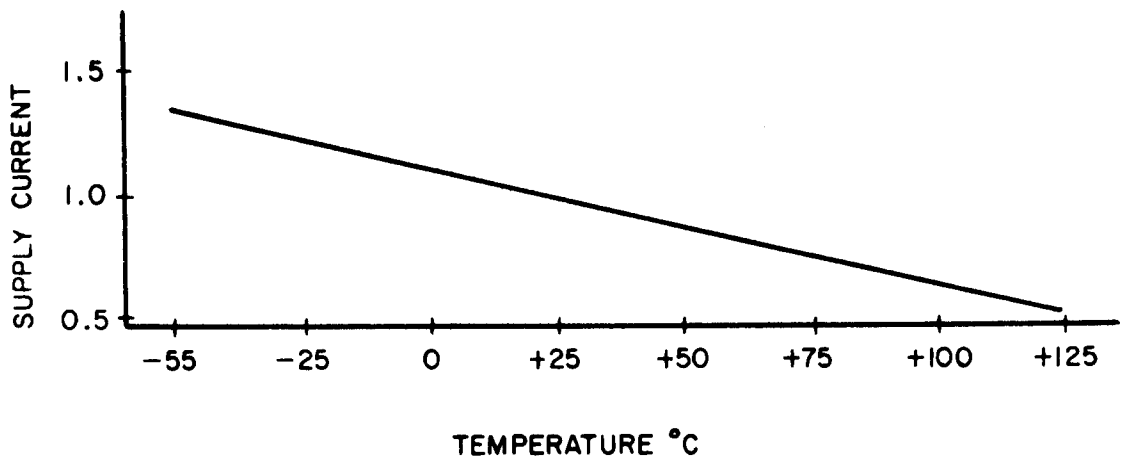


NOTES:

V_{LOAD}:

1. V_{OL} = 2.92 V
2. V_{OH} = 3.49 V
3. C_L = Load + tester + probe capacitance.
4. Diode = IN4533 or equivalent.

FIGURE 5. Dynamic functional load.



NOTE: $\Delta I_{supply} / \Delta T_C = -0.45\%/°C$.

FIGURE 6. Typical supply current versus temperature, normalized.

TABLE III. Group A inspection.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{10}	V_{SS}	D_4	D_5	D_6	D_7	D_3	D_2	D_1	D_0	V_{BB}	RSET	HOLD	INT	Ø2	INTE	DBIN	$\overline{WR}$	SYNC	V_{CC}
T_C=25°C[1]				Same tests, terminal conditions, and limits as for subgroup 2, except T_C = 25°C.																			
T_C=+125°C[2]	V_{IC} (NEG)		1	-100μA	GND									GND									
			2		"	-100μA								"									
			3		"		-100μA							"									
			4		"			-100μA						"									
			5		"				-100μA					"									
			6		"					-100μA				"									
			7		"						-100μA			"									
			8		"							-100μA		"									
			9		"								-100μA	"									
			10		"									"	-100μA								
			11		"									"		-100μA							
			12		"									"			-100μA						
			13		"									"				-100μA					
			14		"									"					-100μA				
			15		"									"						-100μA			
			16		"									"							-100μA		
			17		"									"								-100μA	
			18		"									"									
			19		"									"									
			20		"									"									
			21		"									"									
			22		"									"									
			23		"									"									
			24		"									"									
			25		"									"									
			26		"									"									
			27		"									"									
			28		"									"									
			29		"									"									
			30		"									"									
			31		"									"									
			32		"									"									
			33		"									"									
			34		"									"									
			35		"									"									
			36		"									"									

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Test no.	21 HLDA	22 Ø1	23 RDY	24 WAIT	25 A_0	26 A_1	27 A_2	28 V_{DD}	29 A_3	30 A_4	31 A_5	32 A_6	33 A_7	34 A_8	35 A_9	36 A_{15}	37 A_{12}	38 A_{13}	39 A_{14}	40 A_{11}	Measured terminal	Test Limits Min	Test Limits Max	Unit
1								GND													1		-2.0	V
2								"													3		"	"
3								"													4		"	"
4								"													5		"	"
5								"													6		"	"
6								"													7		"	"
7								"													8		"	"
8								"													9		"	"
9								"													10		"	"
10								"													12		"	"
11								"													13		"	"
12								"													14		"	"
13								"													15		"	"
14								"													16		"	"
15								"													17		"	"
16								"													18		"	"
17								"													19		"	"
18	-100μA							"													21		"	"
19		-100μA						"													22		"	"
20			-100μA					"													23		"	"
21				-100μA				"													24		"	"
22					-100μA			"													25		"	"
23						-100μA		"													26		"	"
24							-100μA	"													27		"	"
25								"	-100μA												29		"	"
26								"		-100μA											30		"	"
27								"			-100μA										31		"	"
28								"				-100μA									32		"	"
29								"					-100μA								33		"	"
30								"						-100μA							34		"	"
31								"							-100μA						35		"	"
32								"								-100μA					36		"	"
33								"									-100μA				37		"	"
34								"										-100μA			38		"	"
35								"											-100μA		39		"	"
36								"												-100μA	40		"	"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1 A_{10}	2 V_{SS}	3 D_4	4 D_5	5 D_6	6 D_7	7 D_3	8 D_2	9 D_1	10 D_0	11 V_{BB}	12 RSET	13 HOLD	14 INT	15 Ø2	16 INTE	17 DBIN	18 $\overline{WR}$	19 SYNC	20 V_{CC}
2 T_C=+125°C	V_{TC} (POS)		37	0.4V	GND									GND									GND
			38		"	0.4V								"									"
			39		"		0.4V							"									"
			40		"			0.4V						"									"
			41		"				0.4V					"									"
			42		"					0.4V				"									"
			43		"						0.4V			"									"
			44		"							0.4V		"									"
			45		"								0.4V	"									"
			46		"									"	0.4V								"
			47		"									"		0.4V							"
			48		"									"			0.4V						"
			49		"									"				0.4V					"
			50		"									"					0.4V				"
			51		"									"						0.4V			"
			52		"									"							0.4V		"
			53		"									"								0.4V	"
			54		"									"									"
			55		"									"									"
			56		"									"									"
			57		"									"									"
			58		"									"									"
			59		"									"									"
			60		"									"									"
			61		"									"									"
			62		"									"									"
			63		"									"									"
			64		"									"									"
			65		"									"									"
			66		"									"									"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measured terminal	Test Limits		Unit
Test no.	HLDA	Ø1	RDY	WAIT	A_0	A_1	A_2	V_{DD}	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{15}	A_{12}	A_{13}	A_{14}	A_{11}		Min	Max	
37								GND													1		3.0	mA
38								"													3		"	"
39								"													4		"	"
40								"													5		"	"
41								"													6		"	"
42								"													7		"	"
43								"													8		"	"
44								"													9		"	"
45								"													10		"	"
46								"													12		"	"
47								"													13		"	"
48								"													14		"	"
49								"													15		"	"
50								"													16		"	"
51								"													17		"	"
52								"													18		"	"
53								"													19		"	"
54	0.4V							"													21		"	"
55		0.4V						"													22		"	"
56			0.4V					"													23		"	"
57				0.4V				"													24		"	"
58					0.4V			"													25		"	"
59						0.4V		"													26		"	"
60							0.4V	"													27		"	"
61								"	0.4V												29		"	"
62								"		0.4V											30		"	"
63								"			0.4V										31		"	"
64								"				0.4V									32		"	"
65								"					0.4V								33		"	"
66								"						0.4V							34		"	"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{10}	V_{SS}	D_4	D_5	D_6	D_7	D_3	D_2	D_1	D_0	V_{BB}	RSET	HOLD	INT	Ø2	INTE	DBIN	$\overline{WR}$	SYNC	V_{CC}
2 T_C=+125°C	V_{IC} (POS)		67		GND									GND									GND
			68		"									"									"
			69		"									"									"
			70		"									"									"
			71		"									"									"
			72		"									"									"
	I_{IH1}	3010	73		"									-4.5	GND	GND	GND	13.2					5.5
		"	74		"									"	"	"	"	GND					"
		"	75		"									"	5.5	"	"	"					"
		"	76		"									"	GND	5.5	"	"					"
		"	77		"									"	"	GND	5.5	"					"
		"	78		"									"	"	"	GND	"					"
	I_{IL1}	3009	79		"									"	"	"	"	"					"
		"	80		"									"	"	"	"	13.2					"
		"	81		"									"	"	"	"	GND					"
		"	82		"									"	"	"	"	"					"
		"	83		"									"	"	"	"	"					"
		"	84		"									"	"	"	"	"					"
	I_{IH2}	3010	85		GND	5.5	GND	GND	GND	GND	GND	GND	GND	"									"
		"	86		"	GND	5.5	GND	"	"	"	"	"	"									"
		"	87		"	"	GND	5.5	"	"	"	"	"	"									"
		"	88		"	"	"	GND	5.5	"	"	"	"	"									"
		"	89		"	"	"	"	GND	5.5	"	"	"	"									"
		"	90		"	"	"	"	"	GND	5.5	"	"	"									"
		"	91		"	"	"	"	"	"	GND	5.5	"	"									"
		"	92		"	"	"	"	"	"	"	GND	5.5	"									"
	I_{IL2}	3009	93		"	0.8	"	"	"	"	"	"	GND	"									"
		"	94		"	GND	0.8	"	"	"	"	"	"	"									"
		"	95		"	"	GND	0.8	"	"	"	"	"	"									"
		"	96		"	"	"	GND	0.8	"	"	"	"	"									"
		"	97		"	"	"	"	GND	0.8	"	"	"	"									"
		"	98		"	"	"	"	"	GND	0.8	"	"	"									"
		"	99		"	"	"	"	"	"	GND	0.8	"	"									"
		"	100		"	"	"	"	"	"	"	GND	0.8	"									"
	I_{ZL1}		101	GND	"	.45	"	"	"	"	"	GND	GND	"									"
	I_{ZL1}		102	"	"	GND	.45	"	"	"	"	GND	GND	"									"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Test no.	21 HLDA	22 Ø1	23 RDY	24 WAIT	25 A_0	26 A_1	27 A_2	28 V_{DD}	29 A_3	30 A_4	31 A_5	32 A_6	33 A_7	34 A_8	35 A_9	36 A_{15}	37 A_{12}	38 A_{13}	39 A_{14}	40 A_{11}	Measured terminal	Test Limits Min	Test Limits Max	Unit
67								GND							0.4V						35		3.0	mA
68								"								0.4V					36		"	"
69								"									0.4V				37		"	"
70								"										0.4V			38		"	"
71								"											0.4V		39		"	"
72								"												0.4V	40		"	"
73		GND	GND					13.2													15		10	µA
74		13.2	"					"													22		"	"
75		GND	"					"													12		"	"
76		"	"					"													13		"	"
77		"	"					"													14		"	"
78		"	5.5					"													23		"	"
79		13.2	GND					"													15		-10	"
80		GND	"					"													22		"	"
81		"	"					"													12		"	"
82		"	"					"													13		"	"
83		"	"					"													14		"	"
84		"	"					"													23		"	"
85								"													3		+100	µA
86								"													4		"	"
87								"													5		"	"
88								"													6		"	"
89								"													7		"	"
90								"													8		"	"
91								"													9		"	"
92								"													10		"	"
93								"													3		-100	"
94								"													4		"	"
95								"													5		"	"
96								"													6		"	"
97								"													7		"	"
98								"													8		"	"
99								"													9		"	"
100								"													10		"	"
101					GND	GND	GND	"	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	3		"	"
102					GND	GND	GND	"	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	4		"	"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{10}	V_{SS}	D_4	D_5	D_6	D_7	D_3	D_2	D_1	D_0	V_{BB}	RSET	HOLD	INT	Ø2	INTE	DBIN	$\overline{WR}$	SYNC	V_{CC}
2 T_C=+125°C	I_{ZL1}		103	GND	GND	GND	GND	.45	GND	GND	GND	GND	GND	-4.5									5.5
			104	"	"	"	"	GND	.45	"	"	"	"	"									"
			105	"	"	"	"	"	GND	.45	"	"	"	"									"
			106	"	"	"	"	"	"	GND	.45	"	"	"									"
			107	"	"	"	"	"	"	"	GND	.45	"	"									"
			108	"	"	"	"	"	"	"	"	GND	.45	"									"
			109	.45	"	"	"	"	"	"	"	"	GND	"									"
			110	GND	"	"	"	"	"	"	"	"	"	"									"
			111	"	"	"	"	"	"	"	"	"	"	"									"
			112	"	"	"	"	"	"	"	"	"	"	"									"
			113	"	"	"	"	"	"	"	"	"	"	"									"
			114	"	"	"	"	"	"	"	"	"	"	"									"
			115	"	"	"	"	"	"	"	"	"	"	"									"
			116	"	"	"	"	"	"	"	"	"	"	"									"
			117	"	"	"	"	"	"	"	"	"	"	"									"
			118	"	"	"	"	"	"	"	"	"	"	"									"
			119	"	"	"	"	"	"	"	"	"	"	"									"
			120	"	"	"	"	"	"	"	"	"	"	"									"
			121	"	"	"	"	"	"	"	"	"	"	"									"
			122	"	"	"	"	"	"	"	"	"	"	"									"
			123	"	"	"	"	"	"	"	"	"	"	"									"
			124	"	"	"	"	"	"	"	"	"	"	"									"
	I_{ZH1}		125	GND	GND	5.5	GND	GND	GND	GND	GND	GND	GND	-4.5									5.5
			126	"	"	GND	5.5.	"	"	"	"	"	"	"									"
			127	"	"	"	GND	5.5	"	"	"	"	"	"									"
			128	"	"	"	"	GND	5.5	"	"	"	"	"									"
			129	"	"	"	"	"	GND	5.5	"	"	"	"									"
			130	"	"	"	"	"	"	GND	5.5	"	"	"									"
			131	"	"	"	"	"	"	"	GND	5.5	"	"									"
			132	"	"	"	"	"	"	"	"	GND	5.5	"									"
			133	5.5	"	"	"	"	"	"	"	"	GND	"									"
			134	GND	"	"	"	"	"	"	"	"	"	"									"
			135	"	"	"	"	"	"	"	"	"	"	"									"
			136	"	"	"	"	"	"	"	"	"	"	"									"
			137	"	"	"	"	"	"	"	"	"	"	"									"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Test no.	21 HLDA	22 ø1	23 RDY	24 WAIT	25 A_0	26 A_1	27 A_2	28 V_{DD}	29 A_3	30 A_4	31 A_5	32 A_6	33 A_7	34 A_8	35 A_9	36 A_{15}	37 A_{12}	38 A_{13}	39 A_{14}	40 A_{11}	Measured terminal	Test Limits Min	Test Limits Max	Unit
103					GND	GND	GND	13.2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5		-100	µA
104					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	6		"	"
105					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	7		"	"
106					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8		"	"
107					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	9		"	"
108					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	10		"	"
109					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1		"	"
110					.45	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	25		"	"
111					GND	.45	"	"	"	"	"	"	"	"	"	"	"	"	"	"	26		"	"
112					"	GND	.45	"	"	"	"	"	"	"	"	"	"	"	"	"	27		"	"
113					"	"	GND	"	.45	"	"	"	"	"	"	"	"	"	"	"	29		"	"
114					"	"	"	"	GND	.45	"	"	"	"	"	"	"	"	"	"	30		"	"
115					"	"	"	"	"	GND	.45	"	"	"	"	"	"	"	"	"	31		"	"
116					"	"	"	"	"	"	GND	.45	"	"	"	"	"	"	"	"	32		"	"
117					"	"	"	"	"	"	"	GND	.45	"	"	"	"	"	"	"	33		"	"
118					"	"	"	"	"	"	"	"	GND	.45	"	"	"	"	"	"	34			
119					"	"	"	"	"	"	"	"	"	GND	.45	"	"	"	"	"	35		"	"
120					"	"	"	"	"	"	"	"	"	"	GND	.45	"	"	"	"	36		"	"
121					"	"	"	"	"	"	"	"	"	"	"	GND	.45	"	"	"	37		"	"
122					"	"	"	"	"	"	"	"	"	"	"	"	GND	.45	"	"	38			
123					"	"	"	"	"	"	"	"	"	"	"	"	"	GND	.45	"	39		"	"
124					"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	.45	40		"	"
125					GND	GND	GND	10.8	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	3		10	µA
126					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	4		"	"
127					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5		"	"
128					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	6		"	"
129					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	7		"	"
130					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8		"	"
131					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	9		"	"
132					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	10		"	"
133					"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	1		"	"
134					5.5	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	25		"	"
135					GND	5.5	"	"	"	"	"	"	"	"	"	"	"	"	"	"	26		"	"
136					"	GND	5.5	"	"	"	"	"	"	"	"	"	"	"	"	"	27		"	"
137					"	"	GND	"	5.5	"	"	"	"	"	"	"	"	"	"	"	29		"	"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{10}	V_{SS}	D_4	D_5	D_6	D_7	D_3	D_2	D_1	D_0	V_{BB}	RSET	HOLD	INT	Ø2	INTE	DBIN	$\overline{WR}$	SYNC	V_{CC}
2 $T_C=125°C$	I_{ZH1}		138	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	-4.5									5.5
			139	"	"	"	"	"	"	"	"	"	"	"									"
			140	"	"	"	"	"	"	"	"	"	"	"									"
			141	"	"	"	"	"	"	"	"	"	"	"									"
			142	"	"	"	"	"	"	"	"	"	"	"									"
			143	"	"	"	"	"	"	"	"	"	"	"									"
			144	"	"	"	"	"	"	"	"	"	"	"									"
			145	"	"	"	"	"	"	"	"	"	"	"									"
			146	"	"	"	"	"	"	"	"	"	"	"									"
			147	"	"	"	"	"	"	"	"	"	"	"									"
			148	"	"	"	"	"	"	"	"	"	"	"									"
	I_{BB}	3005	149		"									"									"
	I_{CC}	3005	150		"									"									"
	I_{DD}	3005	151		"									"									"
3 $T_C=-55°C$				Same tests, terminal conditions, and limits as for subgroup 2, except T_C = -55°C										and test as shown below.									
	I_{CC}	3005			GND									-4.5									5.5
4 $T_C=+25°C$	C_O	3012	152	A	"	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
		"	153	GND	"	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	154	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	155	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	156	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	157	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	158	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"
		"	159	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"
		"	160	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"
	C_I	"	161	"	"	"	"	"	"	"	"	"	GND	"	A	"	"	"	"	"	"	"	"
		"	162	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"
		"	163	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"
		"	164	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"		"
	C_O	"	165	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A				"
		"	166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A		"	"
		"	167	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"
		"	168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Test no.	21 HLDA	22 Ø1	23 RDY	24 WAIT	25 A_0	26 A_1	27 A_2	28 V_{DD}	29 A_3	30 A_4	31 A_5	32 A_6	33 A_7	34 A_8	35 A_9	36 A_{15}	37 A_{12}	38 A_{13}	39 A_{14}	40 A_{11}	Measured terminal	Test Limits Min	Test Limits Max	Unit
138					GND	GND	GND	10.8	GND	5.5	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	30		10	µA
139					"	"	"	"	"	GND	5.5	"	"	"	"	"	"	"	"	"	31		"	"
140					"	"	"	"	"	"	GND	5.5	"	"	"	"	"	"	"	"	32		"	"
141					"	"	"	"	"	"	"	GND	5.5	"	"	"	"	"	"	"	33		"	"
142					"	"	"	"	"	"	"	"	GND	5.5	"	"	"	"	"	"	34		"	"
143					"	"	"	"	"	"	"	"	"	GND	5.5	"	"	"	"	"	35		"	"
144					"	"	"	"	"	"	"	"	"	"	GND	5.5	"	"	"	"	36		"	"
145					"	"	"	"	"	"	"	"	"	"	"	GND	5.5	"	"	"	37		"	"
146					"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5	"	"	38		"	"
147					"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5	"	39		"	"
148					"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	5.5	40		"	"
149								13.2													11		-1.0	mA
150								13.2													20		100	mA
151								13.2													28		85	mA
								13.2															120	mA
152	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	1	2	20	pF
153	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	3	"	"	"
154	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	4	"	"	"
155	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	5	"	"	"
156	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	6	"	"	"
157	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	7	"	"	"
158	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	8	"	"	"
159	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	9	"	"	"
160	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	10	"	"	"
161	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	12	"	15	"
162	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	13	"	15	"
163	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	14	"	15	"
164	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	15	"	30	"
165	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	16	"	20	"
166	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	17	"	"	"
167	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	18	"	"	"
168	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	19	"	"	"

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Subgroup	Symbol	MIL-STD-883 method	Test no.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				A_{10}	V_{SS}	D_4	D_5	D_6	D_7	D_3	D_2	D_1	D_0	V_{BB}	RSET	HOLD	INT	Ø2	INTE	DBIN	$\overline{WR}$	SYNC	V_{CC}
4	C_O	3012	169	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
T_C=+25°C	C_I	"	170	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_I	"	171	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	C_O	"	172	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	173	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	174	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	175	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	176	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	177	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	178	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	179	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	180	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	181	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	182	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	183	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	184	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	185	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	186	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
		"	187	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
7	Dynamic func-tional tests	3014	-	Subgroup (7): Table V input test condition A of table IV.																			
		3007 3006 3003	-	Subgroup (7): Table V input test condition B of table IV.																			
8			-	Subgroup (8): Repeat subgroup 7 at -55°C for both conditions A and B.																			
			-	Subgroup (8): Repeat subgroup 7 at +125°C for both conditions A and B.																			

TABLE III. Group A inspection - Continued.
Terminal conditions (pins not designated are open)

Test no.	21 HLDA	22 Ø1	23 RDY	24 WAIT	25 A_0	26 A_1	27 A_2	28 V_{DD}	29 A_3	30 A_4	31 A_5	32 A_6	33 A_7	34 A_8	35 A_9	36 A_{15}	37 A_{12}	38 A_{13}	39 A_{14}	40 A_{11}	Measured terminal	Test Limits Min	Test Limits Max	Unit
169	A	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	21	2	20	pF
170	GND	A	GND	GND	"	"	"	"	"		"	"	"	"	"	"	"	"	"	"	22	"	30	"
171	"	GND	A	GND	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	23	"	15	"
172	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	24	"	20	"
173	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	25	"	"	"
174	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	"	26	"	"	"
175	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	"	"	"	27	"	"	"
176	"	"	"	"	"	"	GND	"	A	"	"	"	"	"	"	"	"	"	"	"	29	"	"	"
177	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	"	30	"	"	"
178	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	"	31	"	"	"
179	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	"	32	"	"	"
180	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	"	33	"	"	"
181	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	"	34	"	"	"
182	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	"	35	"	"	"
183	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	"	36	"	"	"
184	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	"	37	"	"	"
185	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	"	38	"	"	"
186	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	"	39	"	"	"
187	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	GND	A	40	"	"	"

Notes for subgroups 2, 4, 7, and 8.

1. A = The capacitance measurements shall be made between the indicated terminal and the grounded terminals at a frequency of 1 MHz. The DC bias of the measuring instrument shall be less than +0.1 V. The AC signal amplitude shall be less than 50 mV rms.

2. I_O = -100 μA.

3. Test numbers 85 through 151 are performed during the functional tests of subgroup 7 and may be completed at any convenient place in the functional test provided the table requirements are met.

Test conditions 85 - 108 - These tests are completed while the microprocessor is in a read mode, wait state. Vector 20 of table V is a possible location where these measurements could be made. The tester should loop on this vector until all test conditions have been completed.

Test conditions 109 - 151 - These tests are completed while the microprocessor is in a hold state. Vector 40 of table V is a possible location where these measurements could be made. The tester should loop on this vector until all test conditions have been completed. Pins not designated for these test conditions (85 through 151) are not necessarily open. Pin conditions per the test vectors of subgroup 7 will apply. When these tests are performed during group A inspection, data will be recorded.

TABLE III. Group A inspection - Continued.

Symbol	Test number	MIL-STD-883 method	Waveform figure	Measured terminal	Test limits				Unit
					Subgroup 12 T_C = +25°C		Subgroup 12 T_C = +125°C		
					Min	Max	Min	Max	
V_{OH}	188	3006 3014		10			3.7		V
"	189	"		9			"		"
"	190	"		8			"		"
"	191	"		7			"		"
"	192	"		3			"		"
"	193	"		4			"		"
"	194	"		5			"		"
"	195	"		6			"		"
"	196	"		25			"		"
"	197	"		26			"		"
"	198	"		27			"		"
"	199	"		29			"		"
"	200	"		30			"		"
"	201	"		31			"		"
"	202	"		32			"		"
"	203	"		33			"		"
"	204	"		34			"		"
"	205	"		35			"		"
"	206	"		1			"		"
"	207	"		40			"		"
"	208	"		37			"		"
"	209	"		38			"		"
"	210	"		39			"		"
"	211	"		36			"		"
"	212	"		16			"		"
"	213	"		17			"		"

TABLE III. Group A inspection - Continued.

Symbol	Test number	MIL-STD-883 method	Waveform figure	Measured terminal	Test limits				Unit
					Subgroup 12 T_C = +25°C		Subgroup 12 T_C = +125°C		
					Min	Max	Min	Max	
V_{OH}	214	3006 3014		18			3.7		V
	215	"		19			"		"
	216	"		21			"		"
	217	"		24			"		"
V_{OL}	218	3007 3014		10				0.45	"
	219	"		9				"	"
	220	"		8				"	"
	221	"		7				"	"
	222	"		3				"	"
	223	"		4				"	"
	224	"		5				"	"
	225	"		6				"	"
	226	"		25				"	"
	227	"		26				"	"
	228	"		27				"	"
	229	"		29				"	"
	230	"		30				"	"
	231	"		31				"	"
	232	"		32				"	"
	233	"		33				"	"
	234	"		34				"	"
	235	"		35				"	"
	236	"		1				"	"
	237	"		40				"	"
	238	"		37				"	"
	239	"		38				"	"

TABLE III. Group A inspection - Continued.

Symbol	Test number	MIL-STD-883 method	Waveform figure	Measured terminal	Test limits Subgroup 12 T_C = +25°C Min	Subgroup 12 T_C = +25°C Max	Subgroup 12 T_C = +125°C Min	Subgroup 12 T_C = +125°C Max	Unit
V_{OL}	240	3007 3014		39				0.45	V
"	241	"		36				"	"
"	242	"		16				"	"
"	243	"		17				"	"
"	244	"		18				"	"
"	245	"		19				"	"
"	246	"		21				"	"
"	247	"		24				"	"
t_{PLH1} t_{PHL1} t_{PZH1} t_{PZL1}	248	3003 3014	13	3-10				200	ns
t_{PHZ1} t_{PLZ1}	249		12	3-10				150	ns
t_{PLZ2} t_{PHZ2}	250		9	3-10				150	ns
t_{PLZ2} t_{PHZ2}	251		9	1,25-27, 29-40				130	ns
t_{PLH3} t_{PHL3}	252		12	17			25	150	ns
t_{PLZ3} t_{PHZ3}	253		9,11	3-10			4/		
t_{PLZ3} t_{PHZ3}	254		9,11	1,25-27 29-40			4/		
t_{PLH4} t_{PHL4}	255	3003 3014	12	19				140	ns

TABLE III. Group A inspection - Continued.

Symbol	Test number	MIL-STD-883 method	Waveform figure	Measured terminal	Test limits				Unit
					Subgroup 12 T_C = +25°C		Subgroup 12 T_C = +125°C		
					Min	Max	Min	Max	
t_{PLH4} t_{PHL4}	256		13	18				140	ns
t_{PLH4} t_{PHL4}	257		12	24				140	ns
t_{PLH4} t_{PHL4}	258		9	21				140	ns
t_{PLZ4} t_{PHZ4}	259		9	3-10					
t_{PLZ4} t_{PHZ4}	260		9	1,25-27, 29-40					
t_{PHL5} t_{PLH5}	261		7,16	16				200	ns
t_{PLZ5} t_{PHZ5}	262		11	1,25-27, 29-40			-20		ns
t_{PLH6} t_{PHL6}	263		12	1,25-27, 29-40				200	ns
t_{PLH7} t_{PHL7}	264		13	3-10					ns
t_{PLH8} t_{PHL8}	265		13	1,25-27, 29-40					
t_{PLH9} t_{PHL9}	266		13	3-10					
t_{PLH9} t_{PHL9}	267		13	1,25-27, 29-40					

Notes for table III, subgroup 12.

1. Where propagation delay tests for subgroup 12 indicate a group of pins and where two or more propagation delays are specified for a test, only the reading for the pin with the worst delay requires recording. In some cases this will be a maximum reading while for others it will be a minimum reading as indicated in the table.

2. The table IV functional tests (subgroup 7) shall be repeated for input test conditions of table IIIA when making measurements for test conditions 256 through 275. Wherever valid throughout the functional tests, outputs shall be monitored.

3. Tests 196-255 may be performed during the functional tests of subgroup 7. If the functional tests are used, the measurements may be completed at any convenient spot where the outputs are at their proper logic levels. The tests are performed with the device placed in the "wait" state. Power supply voltages for these measurements are as follows:

$$V_{BB} = -5.50 \text{ V}$$

$$V_{CC} = +4.50 \text{ V}$$

$$V_{DD} = +10.8 \text{ V}$$

The following tabulation indicates possible measurement locations for these tests.

a. V_{OH}

Measurement Location			Measurement Location		
Symbol	Measured terminal	Vector no. in table V	Symbol	Measured terminal	Vector no. in table V
V_{OH}	10	140	V_{OH}	33	547
"	9	5	"	34	"
"	8	140	"	35	"
"	7	140	"	1	"
"	3	177	"	40	"
"	4	5	"	37	"
"	5	140	"	38	"
"	6	5	"	39	"
"	25	547	"	36	"
"	26	"	"	16	1118
"	27	"	"	17	547
"	29	"	"	18	547
"	30	"	"	19	5
"	31	"	"	21	37
"	32	"	"	24	17

b. V_{OL}

Measurement Location			Measurement Location		
Symbol	Measured terminal	Vector no. in table V	Symbol	Measured terminal	Vector no. in table V
V_{OL}	10	174	V_{OL}	33	6
"	9	"	"	34	"
"	8	"	"	35	"
"	7	"	"	1	"
"	3	"	"	40	"
"	4	"	"	37	"
"	5	"	"	38	"
"	6	"	"	39	"
"	25	6	"	36	"
"	26	"	"	16	5
"	27	"	"	17	5
"	29	"	"	18	140
"	30	"	"	19	6
"	31	"	"	21	5
"	32	"	"	24	5

TABLE IVA. Input conditions for table III.

Symbol	Terminals	Input conditions			
		A	B	Unit	Figure
V_{BB}	V_{BB}	-5.50	-5.50	V	
V_{CC}	V_{CC}	+4.50	+4.50	V	
V_{DD}	V_{DD}	+10.8	+10.8	V	
V_{IH1}	All logic inputs except clock	3.0	3.0	V	
V_{IH2}	clock inputs	8.5	8.5	V	
V_{IL1}	All logic inputs including clock	0.8	0.8	V	
t_{period}	Ø1	0.48	2.0	µs	5
$t_{Ø1}$	Ø1	80	60	ns	5
$t_{Ø2}$	Ø2	220	220	ns	5
t_{SLH6}	$\underline{0}2$	0	20	ns	5
t_{SLH7}	$\underline{0}2$	80	80	ns	5
t_{SLH8}	$\underline{0}2$	180	1700	ns	5
t_{SLH2}	D_0-D_7	130	130	ns	12
t_{SHL2}	D_0-D_7	130	130	ns	12
t_{SLH3}	D_0-D_7	130	130	ns	12
t_{SHL3}	D_0-D_7	130	130	ns	12

TABLE IVA. Input conditions for table III - Continued.

Symbol	Terminals	Input conditions			
		A	B	Unit	Figure
t_{HHL2}	D_0-D_7	50	50	ns	12
t_{HLH2}	D_0-D_7	50	50	ns	12
t_{SLH1}	Ready	120	120	ns	10
t_{SHL1}	Ready	120	120	ns	12,13
t_{HHL1}	Ready INT Hold	0	0	ns	7,8, 9,10
t_{HLH1}	Ready INT Hold	0	0	ns	7,8, 11,12, 13
t_{SLH4}	INT	120	120	ns	7,8
t_{SHL4}	INT	120	120	ns	7,8
t_{SHL5}	Hold	140	140	ns	11
t_{SLH55}	Hold	140	140	ns	9
t_{SLH9}	Reset	75	75	ns	14
t_{HHL3}	Reset	75	75	ns	14

TABLE IVB. Output conditions for table III.

Symbol	Measurement terminal	Figure	Test limits						Unit
			Subgroup 7 T_C = 25°C		Subgroup 8 T_C = -55°C		Subgroup 8 T_C = +125°C		
			Min	Max	Min	Max	Min	Max	
V_{OH}	All outputs	---	3.7		3.7		3.7		V
V_{OL}	All outputs	---		0.45		0.45		0.45	V
t_{PLH1}	D_0-D_7	12,13						220	ns
t_{PHL1}		12,13						220	ns
t_{PZH1}		12,13						220	ns
t_{PZL1}		12,13						220	ns
t_{PHZ1}		12						140	ns
t_{PLZ1}		12						140	ns
t_{PLZ2}	A_0-A_{15}	9						130	ns
t_{PHZ2}	D_0-D_7	9						130	ns
t_{PLH3}	DBIN	12					25	150	ns
t_{PHL3}		12					25	150	ns
t_{PHZ3}	A_0-A_{15}	11	See table I, note 2						ns
t_{PLZ3}	D_0-D_7	11							ns
t_{PLH4}	SYNC, $\overline{WR}$, HLDA WAIT	9,10,11 12,13						140	ns
t_{PHL4}		9,10,11 12,13,17						140	ns
t_{PHZ4}	A_0-A_{15}	11	See table I, note 3						ns
t_{PLZ4}	D_0-D_7	11							ns
t_{PHL5}	INTE	7						200	ns
t_{PLH5}		16						200	ns

TABLE IVB. Output conditions for table III - Continued.

Symbol	Measurement terminal	Figure	Test limits						Unit
			Subgroup 7 $T_C = 25°C$		Subgroup 8 $T_C = -55°C$		Subgroup 9 $T_C = +125°C$		
			Min	Max	Min	Max	Min	Max	
t_{PHZ5}	A_0-A_{15}	11					-20		ns
t_{PLZ5}		11					-20		ns
t_{PLH6}		13						200	ns
t_{PHL6}		13						200	ns
t_{PLH7}	D_0-D_7	13	See table I, note 4						ns
t_{PHL7}		13							ns
t_{PLH8}	A_0-A_{15}	13	See table I, note 5						ns
t_{PHL8}		13							ns
t_{PHL9}	A_0-A_{15}	13	See table I, note 6						ns
t_{PLH9}	D_0-D_7	13							ns

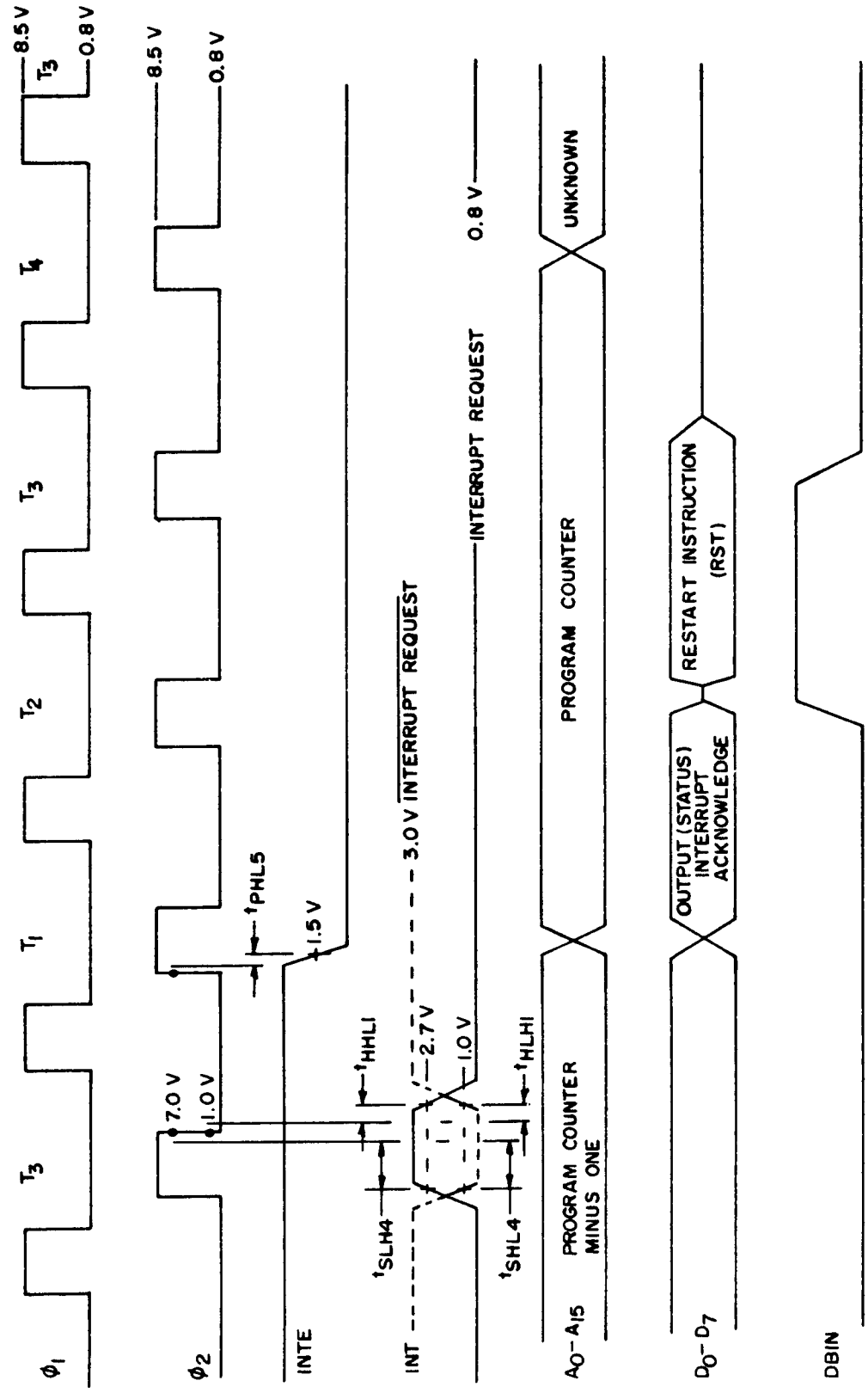


FIGURE 7. Interrupt timing.

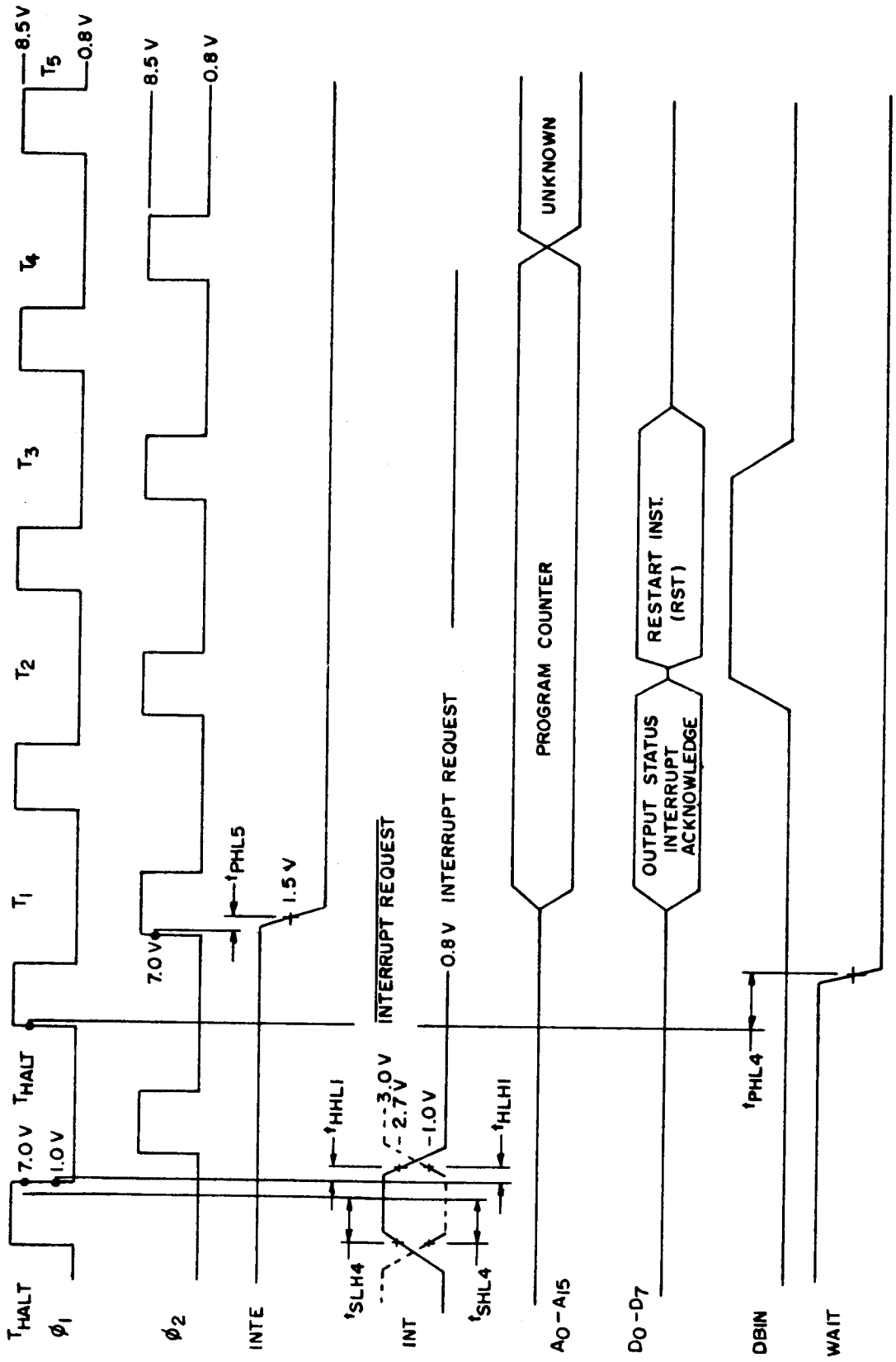


FIGURE 8. Interrupt timing in halt mode.

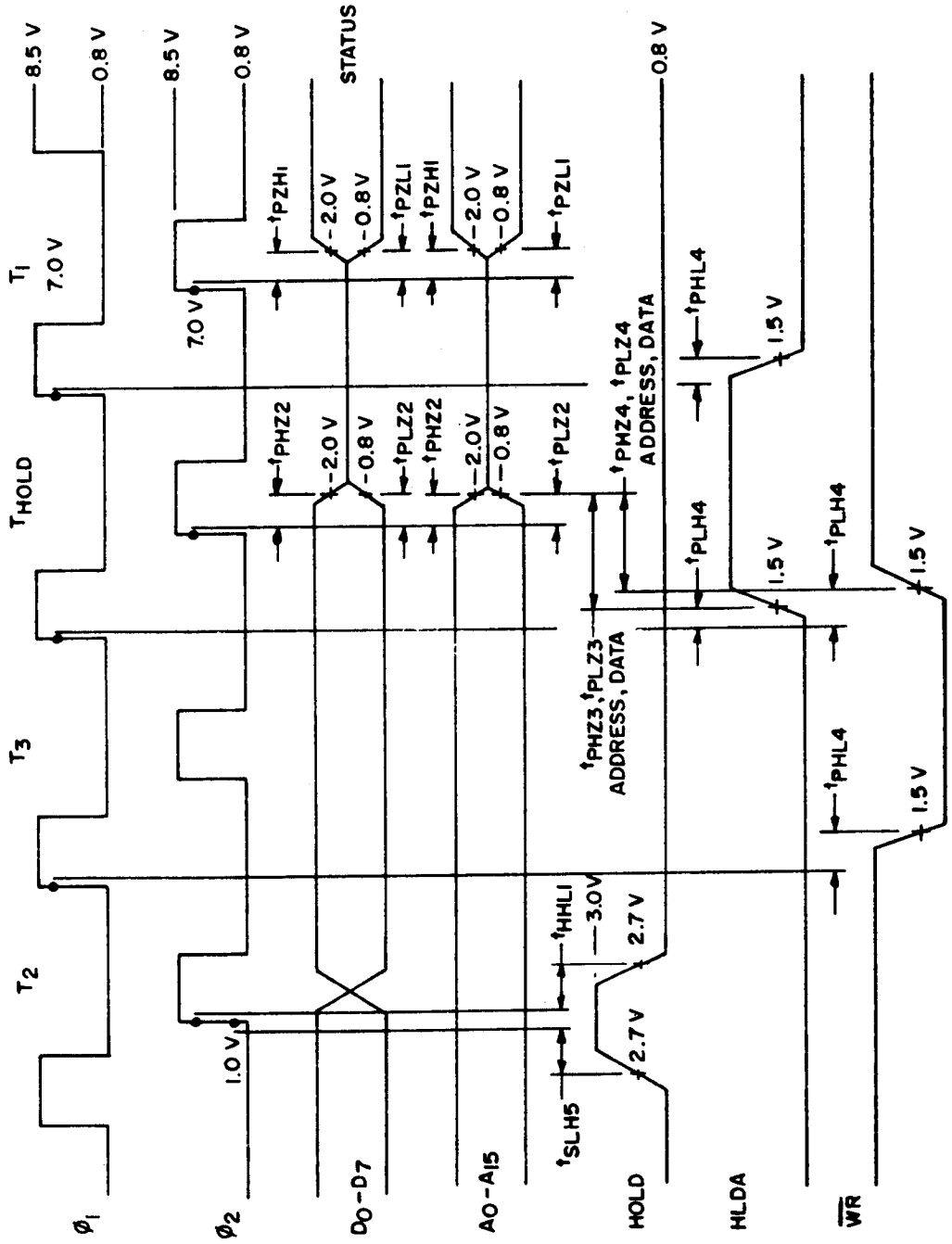


FIGURE 9. Hold sequence - single cycle hold (write cycle).

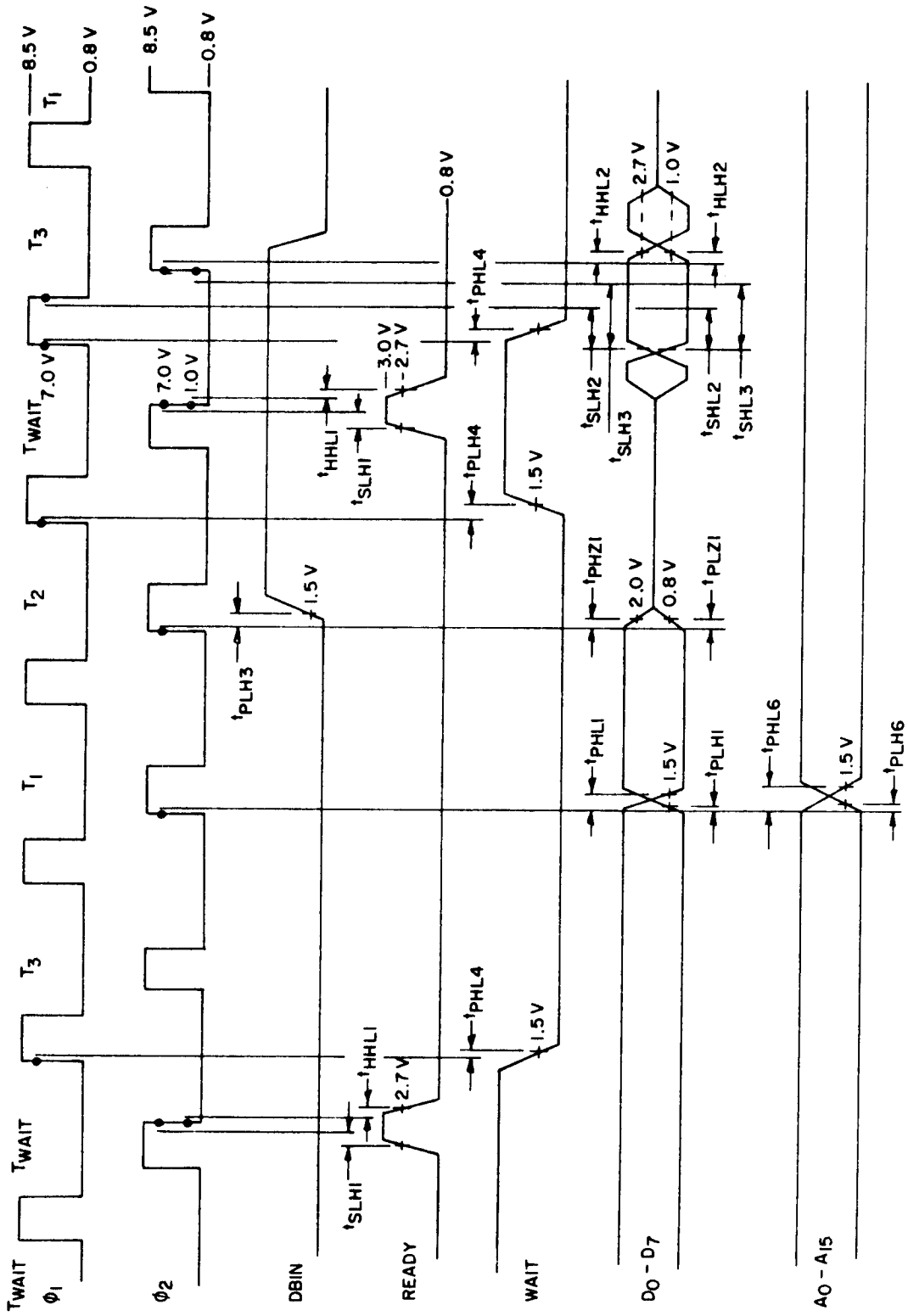


FIGURE 10. Wait - machine cycle execute.

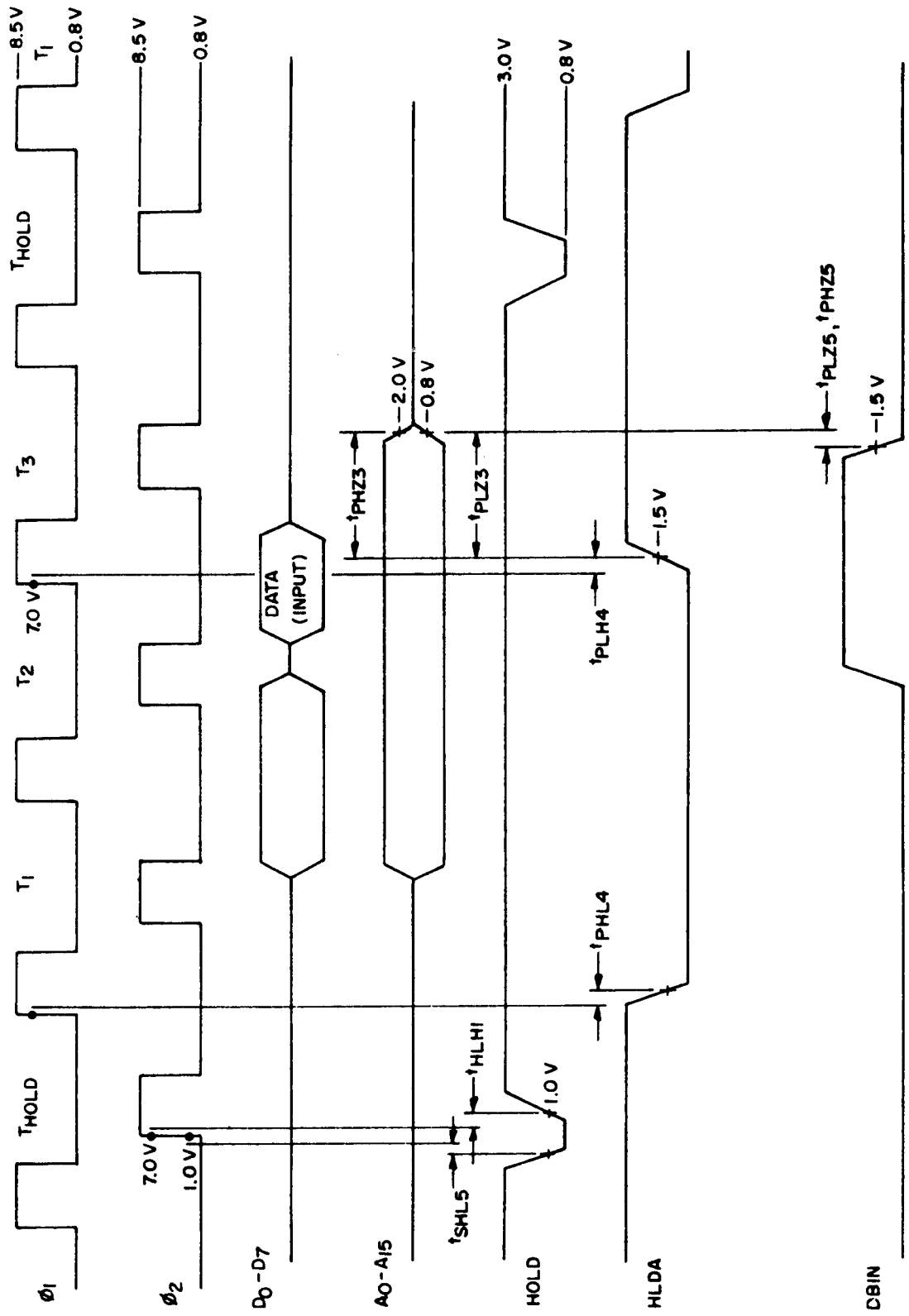
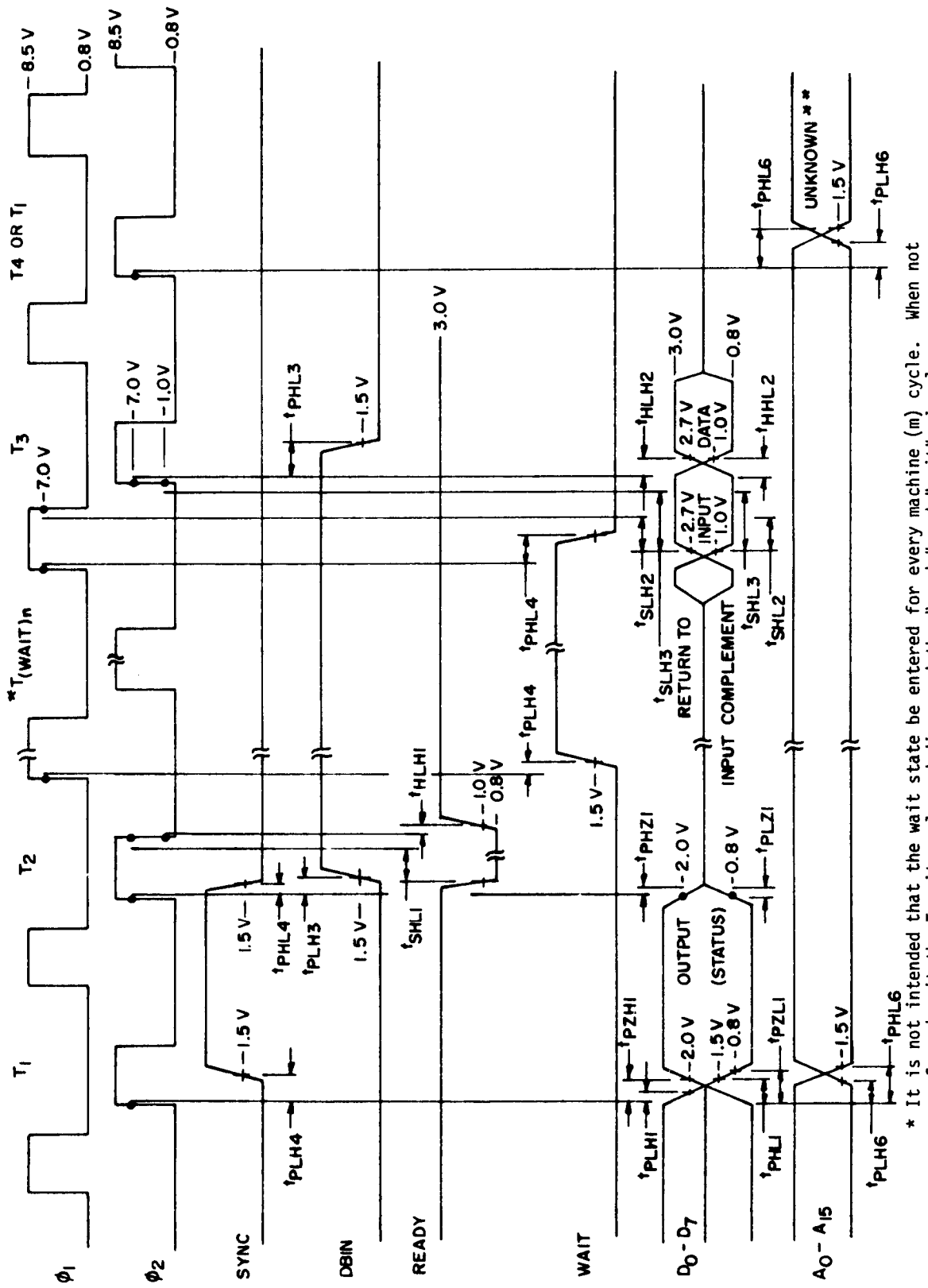


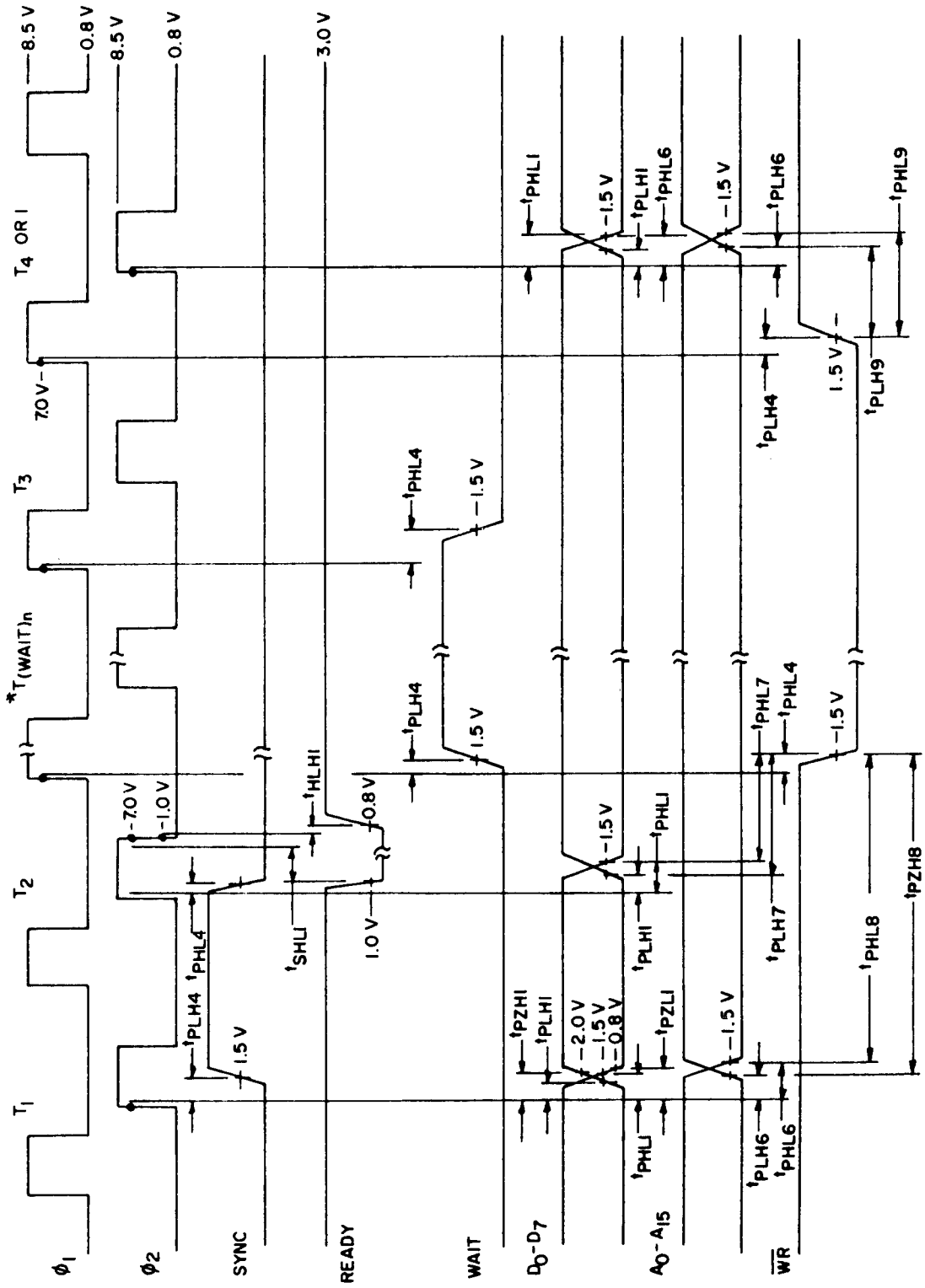
FIGURE 11. Hold sequence - single machine cycle execute (read mode).



* It is not intended that the wait state be entered for every machine (m) cycle. When not performed omit the T wait cycle and disregard the "ready" and "wait" signals.

** Unknown for T_4 cycle.

FIGURE 12. Read cycle with single or multiple wait cycles.



* It is not intended that the wait state be entered for every machine cycle (T_1-T_4 or T_1-T_3). When not performed, omit $T_{(wait)}$ cycle and disregard the "READY" and "WAIT" signals.

FIGURE 13. Write cycle with single or multiple wait cycles.

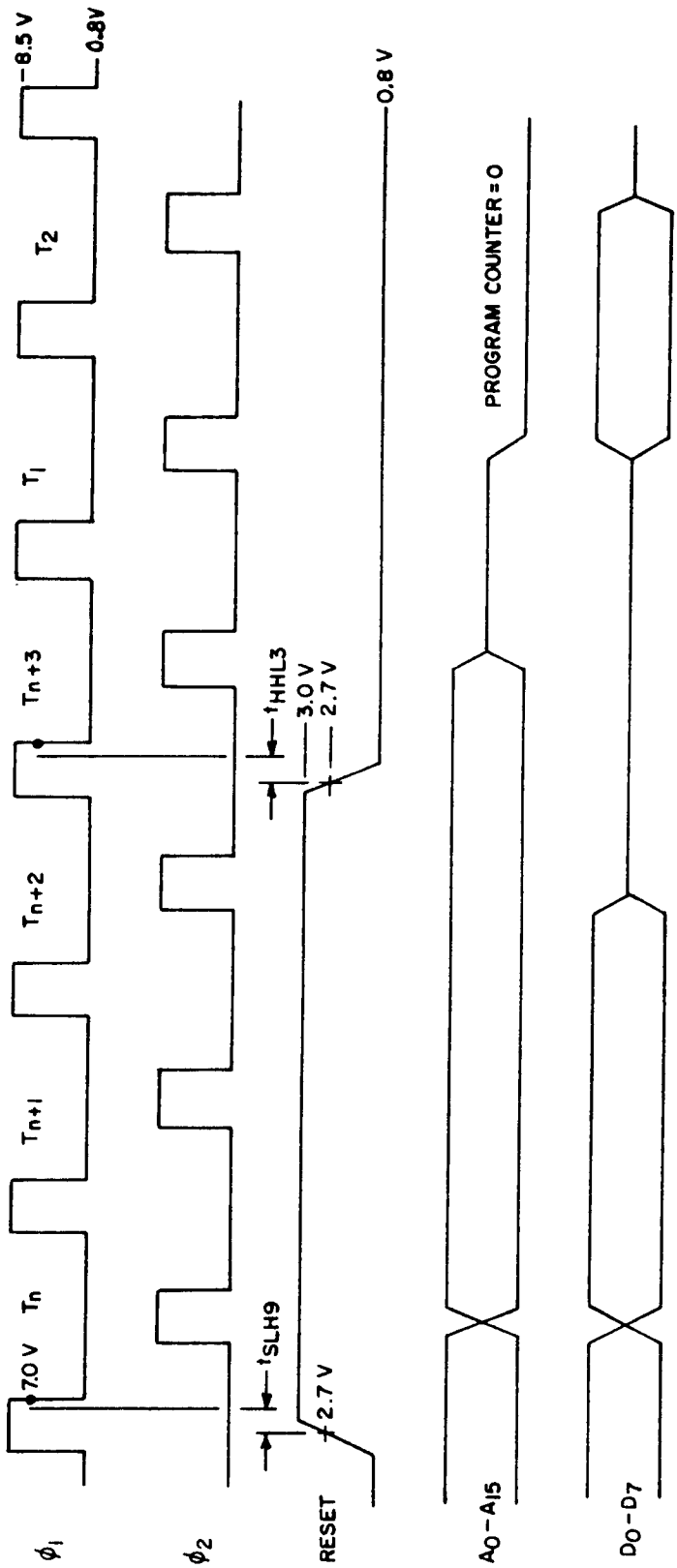
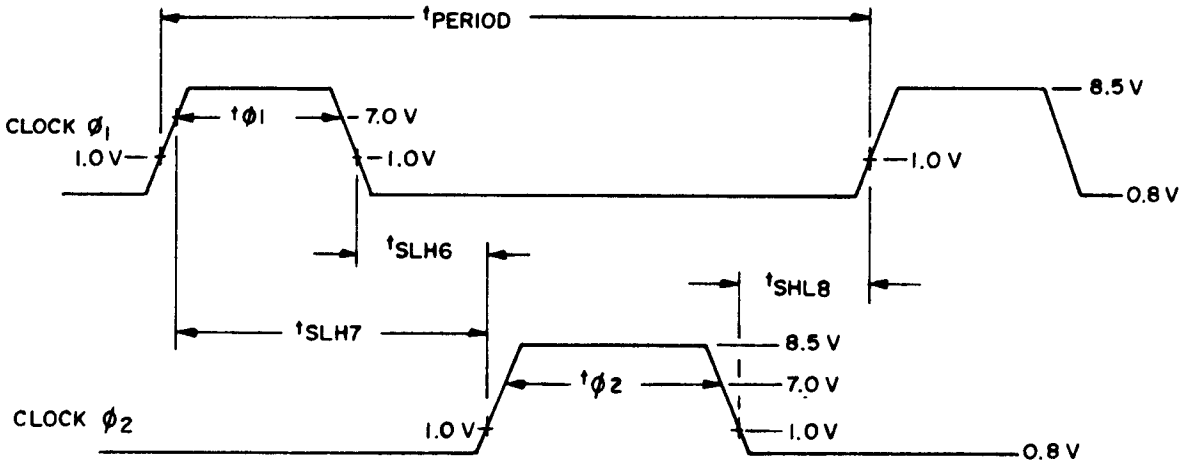


FIGURE 14. Reset timing.



NOTE: Clock $t_{TLH} = t_{THL}$ = 0 to 50 ns maximum; measured from 1.0 V to 7.0 V.

FIGURE 15. Clock waveforms.

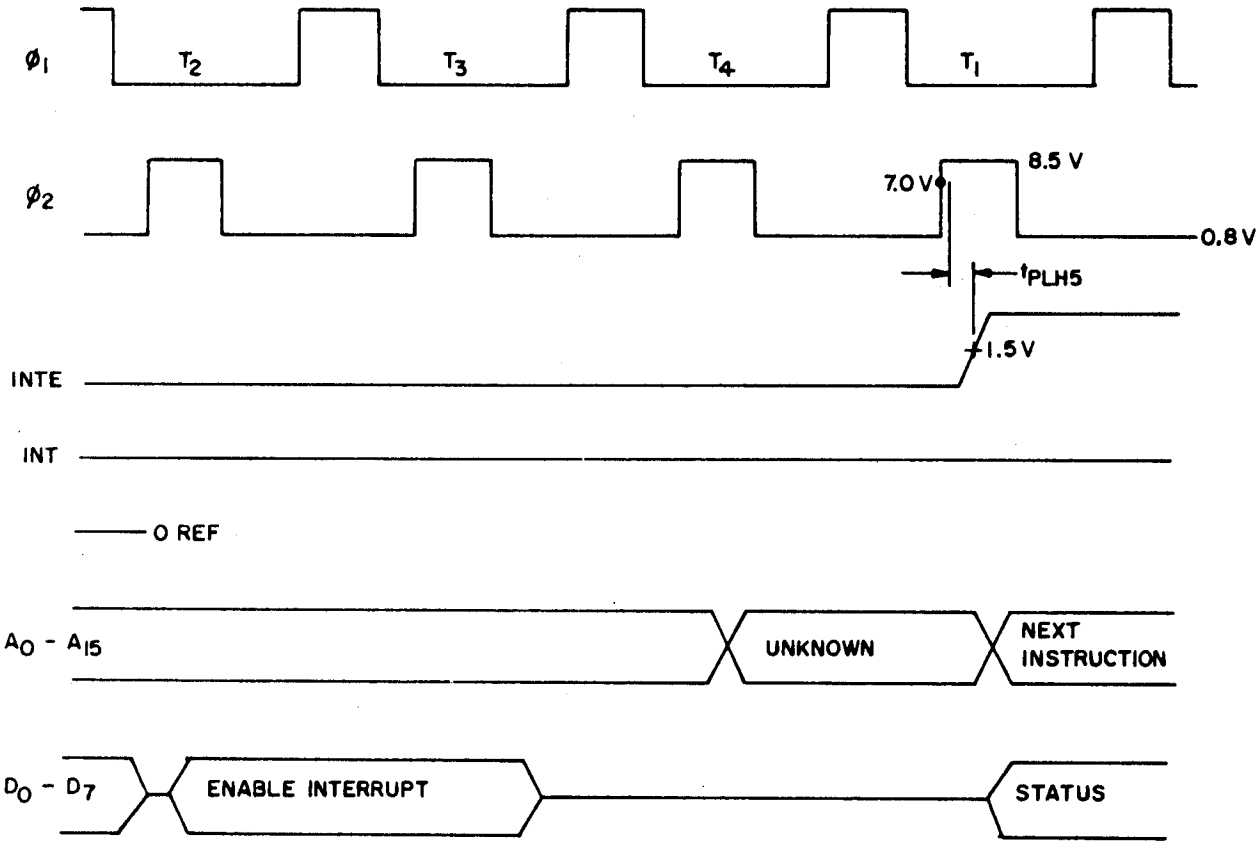


FIGURE 16. Interrupt enable output - set inte flip-flop.

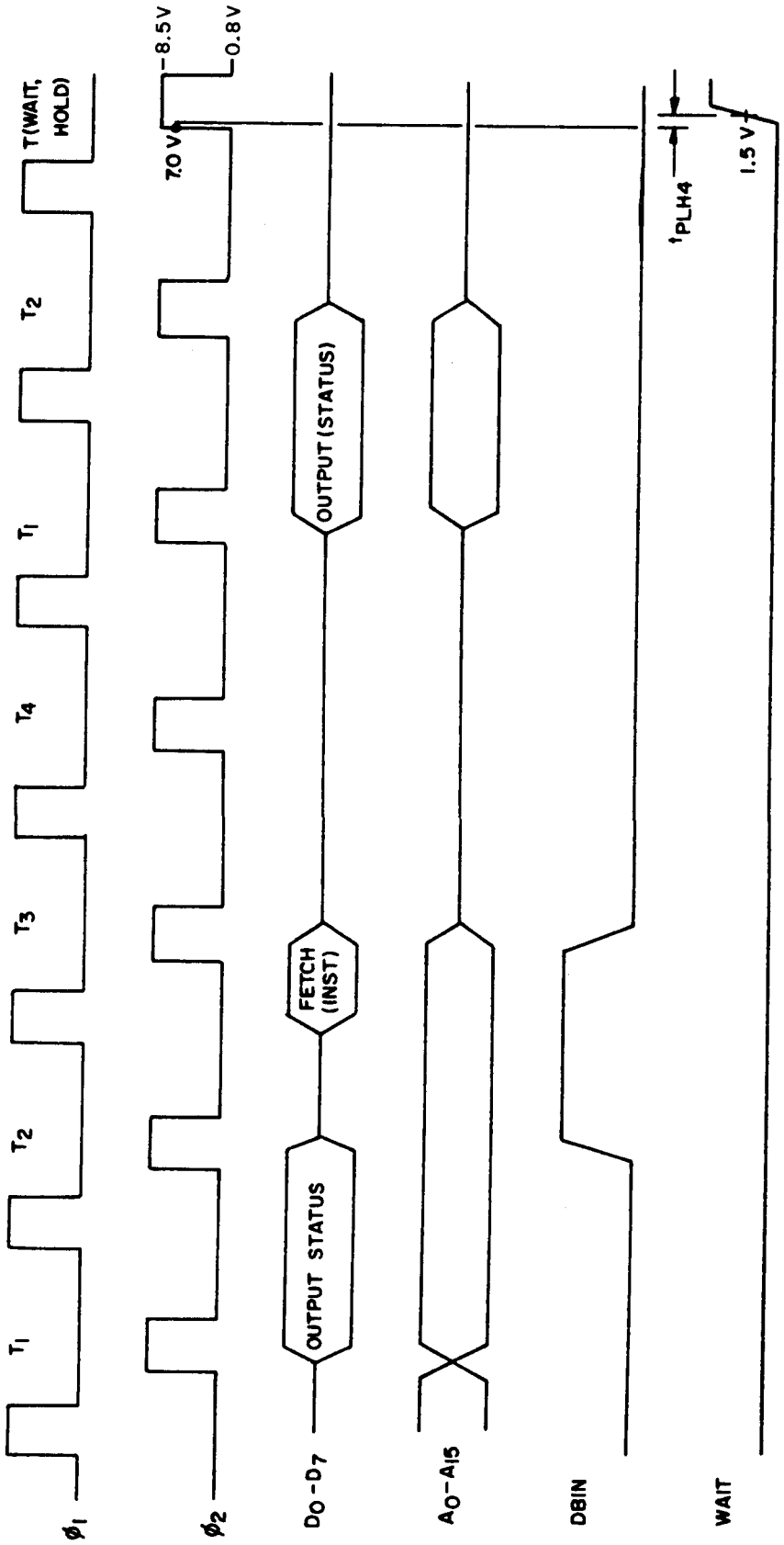


FIGURE 17. Halt timing.

TABLE V. Vectors 1 through 11,761.

Table V, not printed herein, is a computer-generated listing for use with table III. Each vector identifies activity states by pin number. See section 6 for information on obtaining the complete table in compatible output format.

NOTES:

1. Vectors 1 through 11,761, when performed as specified in table III for subgroup 7 verifies the dynamic, functional, output level, threshold, and switching parameters at 25°C.

2. Vectors 1 through 11,761, when performed as specified in table III for subgroup 8 at -55°C verifies the dynamic, functional, output level, threshold, and switching parameters at -55°C.

3. Vectors 1 through 11,761, when performed as specified in table III for subgroup 8 at +125°C verifies the dynamic, functional, output level, threshold, and switching parameters at +125°C.

4. The vector set is organized in groups where each group is less than or equal to 1,024 vectors. This enables the use of this vector set on testers with a local memory greater than or equal to 1,024 locations. Each group of vectors must be applied in the order shown, without pauses, as specified in subgroup 7 or 8. The last vector of each group is as follows:

Group number	Last vector number
1	1,024
2	1,837
3	2,861
4	3.883
5	4,905
6	5,927
7	6,949
8	7,484
9	8,508
10	9,530
11	10,552
12	10,768
13	11,761

The groups must be run consecutively in the order shown. Between application of any two groups, the user has the option of:

a. No pause between the groups or,

b. Repeated application of the last vector of the group at test speed until the tester is ready with the next group. The outputs need not be monitored after the first application of the last vector in each group until the next group is ready.

5. Input levels shall be:

A = 3.0 V

B = 0.8 V

C = Positive pulse from 0.8 V to 8.5 V to 0.8 V as shown on figure 5.

G = Ground (0 V)

V = The power supply voltages as specified in table III.

TABLE V. Vectors 1 through 11,761 - Continued.

6. Output levels shall be monitored at:

   H = 3.7 V minimum.

   L = 0.45 V maximum.

   Z = High impedance; 1.0 V minimum to 1.5 V maximum with the load shown on figure 15.

   X = Don't care; these pins must not be driven when indicated by an X, as damage may occur to the device under test.

7. Inputs shall be applied for the setup and hold times specified in table III and as shown in the applicable figures below:

Signal name	Figure number	Applicable vectors
D_0 - D_7 (input mode)	12	Any with DBM = 0
Reset	14	All
Hold	9,11	All
INT	7,8,16	All
Ø,Ø2	5	All
Ready	12,13	All

8. Outputs shall be monitored for the entire time for which they are valid as stated by the propogation times in table III and as graphically shown in the waveform figures indicated below:

Signal name	Figure number	Applicable vectors
A_0 - A_{15}	12,13	Any with ADM = 0
A_0 - A_{15}	8,9,11,14,17	Any with ADM = 1
D_0 - D_7 (output mode)	13	Any with DBM = 0
INTE	7,8,16	All
DBIN	12	All
$\overline{WR}$	13	All
SYNC	12,13	All
HLDA	9,11	All
WAIT	12,13,17	All

9. Address outputs shall be monitored for logic 1 and logic 0 levels when ADM = 0. Address outputs shall be monitored for high impedance when the value = "Z" in table IV.

TABLE V. Vectors 1 through 11,761 - Continued.

10. Data outputs shall be monitored for logic 1 and logic 0 when DBM = 0 as shown on figure 12. Data outputs shall be monitored for high impedance when the value = "Z" in table V.

11. Data inputs shall be driven as shown on figure 13 when DBI = 0.

12. Data inputs, interupt, hold, and ready signals shall be applied as a "return to complement signal". That is, the signals will be driven to the levels shown in table V only during that part of each cycle specified in the appropriate figures. The signals shall be driven to the opposite level for the remainder of the cycle.

TABLE VI. Microprocessor instructions.

Mnemonic	Description	Instruction Code 1/ D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock 2/ Cycles
$MOV_{r1,r2}$	Move register to register	0	1	D	D	D	S	S	S	6
MOV M r	Move register to memory	0	1	1	1	0	S	S	S	7
MOV r M	Move memory to register	0	1	D	D	D	1	1	0	7
HLT	Halt	0	1	1	1	0	1	1	0	7
MVI r	Move immediate register	0	0	D	D	D	1	1	0	7
MVI M	Move immediate memory	0	0	1	1	0	1	1	0	10
INR r	Increment register	0	0	D	D	D	1	0	0	5
DCR r	Decrement register	0	0	D	D	D	1	0	1	5
INR M	Increment memory	0	0	1	1	0	1	0	0	10
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10
ADD r	Add register to A	1	0	0	0	0	S	S	S	4
ADC r	Add register to A with carry	1	0	0	0	1	S	S	S	4
SUB r	Subtract register from A	1	0	0	1	0	S	S	S	4
SBB r	Subtract register from A with borrow	1	0	0	1	1	S	S	S	4
ANA r	And register with A	1	0	1	0	0	S	S	S	4
XRA r	Exclusive Or register with A	1	0	1	0	1	S	S	S	4
ORA r	Or register with A	1	0	1	1	0	S	S	S	4
CMP r	Compare register with A	1	0	1	1	1	S	S	S	4
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7
ANA M	And memory with A	1	0	1	0	0	1	1	0	7
XRA M	Exclusive Or memory with A	1	0	1	0	1	1	1	0	7
ORA M	Or memory with A	1	0	1	1	0	1	1	0	7

See footnotes at end of table.

TABLE VI. Microprocessor instructions - Continued.

Mnemonic	Description	Instruction Code 1/ D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock 2/ Cycles
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7
ADI	Add immediate to A	1	1	0	0	0	1	1	0	7
ACI	Add immediate to A with carry	1	1	0	0	1	1	1	0	7
SUI	Subtract immediate from A	1	1	0	1	0	1	1	0	7
SBI	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7
ANI	And immediate with A	1	1	1	0	0	1	1	0	7
XRI	Exclusive or immediate with A	1	1	1	0	1	1	1	0	7
ORI	Or immediate with A	1	1	1	1	0	1	1	0	7
CPI	Compare immediate with A	1	1	1	1	1	1	1	0	7
RLC	Rotate A left	0	0	0	0	0	1	1	1	4
RRC	Rotate A right	0	0	0	0	1	1	1	1	4
RAL	Rotate A left through carry	0	0	0	1	0	1	1	1	4
RAR	Rotate A right through carry	0	0	0	1	1	1	1	1	4
JMP	Jump unconditional	1	1	0	0	0	0	1	1	10
JC	Jump on carry	1	1	0	1	1	0	1	0	10
JNC	Jump on no carry	1	1	0	1	0	0	1	0	10
JZ	Jump on zero	1	1	0	0	1	0	1	0	10
JNZ	Jump on no zero	1	1	0	0	0	0	1	0	10
JP	Jump on positive	1	1	1	1	0	0	1	0	10
JM	Jump on minus	1	1	1	1	1	0	1	0	10
JPE	Jump on parity even	1	1	1	0	1	0	1	0	10
JPO	Jump on parity odd	1	1	1	0	0	0	1	0	10
CALL	Call unconditional	1	1	0	0	1	1	0	1	17
CC	Call on carry	1	1	0	1	1	1	0	0	11/17
CNC	Call on no carry	1	1	0	1	0	1	0	0	11/17

See footnotes at end of table.

TABLE VI. Microprocessor instructions - Continued.

Mnemonic	Description	Instruction Code 1/ D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock 2/ Cycles
CZ	Call on zero	1	1	0	0	1	1	0	0	11/17
CNZ	Call on no zero	1	1	0	0	0	1	0	0	11/17
CP	Call on positive	1	1	1	1	0	1	0	0	11/17
CM	Call on minus	1	1	1	1	1	1	0	0	11/17
CPE	Call on parity even	1	1	1	0	1	1	0	0	11/17
CPO	Call on parity odd	1	1	1	0	0	1	0	0	11/17
RET	Return	1	1	0	0	1	0	0	1	10
RC	Return on carry	1	1	0	1	1	0	0	0	5/11
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11
RZ	Return on zero	1	1	0	1	0	0	0	0	5/11
RNZ	Return on no zero	1	1	0	0	0	0	0	0	5/11
RP	Return on positive	1	1	1	1	0	0	0	0	5/11
RM	Return on minus	1	1	1	1	1	0	0	0	5/11
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11
RST	Restart	1	1	A	A	A	1	1	1	11
IN	Input	1	1	0	1	1	0	1	1	10
OUT	Output	1	1	0	1	0	0	1	1	10
LXI B	Load immediate register Pair B and C	0	0	0	0	0	0	0	1	10
LXI D	Load immediate register Pair D and E	0	0	0	1	0	0	0	1	10
LXI H	Load immediate register Pair H and L	0	0	1	0	0	0	0	1	10
LXI SP	Load immediate stack pointer	0	0	1	1	0	0	0	1	10
PUSH B	Push register Pair B and C on stack	1	1	0	0	0	1	0	1	11
PUSH D	Push register Pair D and E on stack	1	1	0	1	0	1	0	1	11

TABLE VI. Microprocessor instructions - Continued.

Mnemonic	Description	Instruction Code 1/ D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock 2/ Cycles
PUSH H	Push register Pair H and L on stack	1	1	1	0	0	1	0	1	11
PUSH PSW	Push A and Flags on stack	1	1	1	1	0	1	0	1	11
POP B	Pop register Pair B and C off stack	1	1	0	0	0	0	0	1	10
POP D	Pop register Pair D and E off stack	1	1	0	1	0	0	0	1	10
POP H	Pop register Pair H and L off stack	1	1	1	0	0	0	0	1	10
POP PSW	Pop A and Flags off stack	1	1	1	1	0	0	0	1	10
STA	Store A direct	0	0	1	1	0	0	1	0	13
LDA	Load A direct	0	0	1	1	1	0	1	0	13
XCHG	Exchange D and E, H and L	1	1	1	0	1	0	1	1	4
XCHG	Registers	1	1	1	0	1	0	1	1	4
XTHL	Exchange top of stack, H and L	1	1	1	0	0	0	1	1	18
SPHL	H and L to stack pointer	1	1	1	1	1	0	0	1	5
PCHL	H and L to program counter	1	1	1	0	1	0	0	1	5
DAD B	Add B and C to H and L	0	0	0	0	1	0	0	1	10
DAD D	Add D and E to H and L	0	0	0	1	1	0	0	1	10
DAD H	Add H and L to H and L	0	0	1	0	1	0	0	1	10
DAD SP	Add stack pointer to H and L	0	0	1	1	1	0	0	1	10
STAX B	Store A indirect	0	0	0	0	0	0	1	0	7
STAX D	Store A indirect	0	0	0	1	0	0	1	0	7
LDAX B	Load A indirect	0	0	0	0	1	0	1	0	7
LDAX D	Load A indirect	0	0	0	1	1	0	1	0	7
INX B	Increment B and C registers	0	0	0	0	0	0	1	1	5
INX D	Increment D and E registers	0	0	0	1	0	0	1	1	5
INX H	Increment H and L registers	0	0	1	0	0	0	1	1	5
INX SP	Increment stack pointer	0	0	1	1	0	0	1	1	5
DCX B	Decrement B and C	0	0	0	0	1	0	1	1	5
DCX D	Decrement D and E	0	0	0	1	1	0	1	1	5

See footnotes at end of table.

TABLE VI. Microprocessor instructions - Continued.

Mnemonic	Description	Instruction Code 1/ D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock 2/ Cycles
DCX H	Decrement H and L	0	0	1	0	1	0	1	1	5
DCX SP	Decrement stack pointer	0	0	1	1	1	0	1	1	5
CMA	Complement A	0	0	1	0	1	1	1	1	4
STC	Set carry	0	0	1	1	0	1	1	1	4
CMC	Complement carry	0	0	1	1	1	1	1	1	4
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4
SHLD	Store H and L direct	0	0	1	0	0	0	1	0	16
LHLD	Load H and L direct	0	0	1	0	1	0	1	0	16
EI	Enable interrupts	1	1	1	1	1	0	1	1	4
DI	Disable interrupt	1	1	1	1	0	0	1	1	4
NOP	No-operation	0	0	0	0	0	0	0	0	4

1/ DDD or SSS - 000 B-001 C - 010 D - 011 E - 100 H - 101 L - 110 Memory - 111 A.

2/ Two possible cycle times, (5/11) indicate instruction cycles dependent on condition flags.

In either case, the HLDA signal appears after the rising edge of Ø1 and high impedance occurs after the rising edge of Ø2.

INT (input). The processor recognizes an interrupt request on this line at the end of the current instruction or while halted. If the CPU is in the HOLD state or if the Interrupt Enable flip/flop is reset it will not honor the request.

RESET (input). While the RESET signal is activated, the content of the program counter is cleared. After RESET, the program will start at location 0 in memory. The INTE and HLDA flip/flops are also reset. Note that the flags, accumulator, stack pointer, and registers are not cleared.

V_{SS} Ground Reference
V_{DD} +12 Volts ±10%
V_{CC} +5 Volts ±10%
V_{BB} -5 Volts ±10%

6.7 Substitutability. Microcircuits covered by this specification are substitutable for the following commercial device types:

Device type	Commercial type
01	8080A

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Agent:
DLA - ES

Preparing activity:
Air Force - 17

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