QUALIFICATION REQUIREMENTS REMOVED

MIL-M-38510/400A
30 September 1983
SUPERSEDING
MIL-M-38510/400(USAF)
25 August 1977

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, N-CHANNEL, SILICON-GATE MONOLITHIC 8 BIT MICROPROCESSOR (FIXED INSTRUCTION)

INACTIVE FOR NEW DESIGN AFTER DATE OF THIS REVISION

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic N-channel, silicon gate microprocessor. One product assurance class and a choice of case outline and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, except the "JAN" or "J" certification mark shall not be used.

1.2.1 Device type. The device type shall be as follows:

Device type	Circuit
01	8-bit fixed instruction microprocessor

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
Q	D-5 (40-lead, 9/16" X 2 1/16"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage, (V_{CC})	-0.3 to +7.0 V dc
Input voltage range	-0.3 to +7.0 V dc
Storage temperature range	-55°C to +150°C
Power dissipation	1.0 W
Lead temperature (soldering, 5 seconds)	270°C
Maximum junction temperature (T_J)	150°C
Thermal resistance, junction-to-case	50°C/W

1.4 Recommended operating conditions.

Supply voltage	4.75 V dc minimum to 5.25 V dc maximum
Minimum high-level input voltage (V_{IH}):	
Logic inputs	2.0 V dc
Clock inputs	V_{CC} - 0.6 V
Maximum low-level input voltage (V_{IL}):	
Logic inputs	0.8 V dc
Clock inputs	0.4 V dc
Clock overlap	0 ns
Frequency of operation	0.1 to 1 MHZ
Case operating temperature range (T_C)	-55°C to +125°C

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. Terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The functional diagram shall be as specified on figure 2.

3.2.3 Functional description, terms, and symbols. Functional description, terms, and symbols shall be as specified in 6.5.

3.2.4 Case outline. Case outline shall be as specified in MIL-M-38510 and in 1.2.3 herein.

3.3 Lead material and finish. Lead material and finish shall be in accordance with MIL-M-38510.

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. Electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, marking of the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container. The "JAN" or "J" certification mark shall not be used.

3.7 Manufacturer eligibility. To be eligible to supply microcircuits to this specification, a manufacturer shall have a manufacturer certification in accordance with MIL-M-38510 for at least one line. Not necessarily the line producing the device type described herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Figure	Limits		Units
				Min	Max	
High-level output voltage D_0 - D_7	V_{OH}	V_{CC} = 4.75 V; I_{OH} = -205 µA	-	2.4	-	V
High-level output voltage A_0-A_{15}, R/W, VMA	V_{OH}	V_{CC} = 4.75 V; I_{OH} = -145 µA	-	2.4	-	V
High-level output voltage BA	V_{OH}	V_{CC} = 4.75 V; I_{OH} = -100 µA	-	2.4	-	V
Low-level output voltage D_0-D_7, A_0-A_{15}, R/W, VMA, BA	V_{OL}	V_{CC} = 4.75 V; I_{OL} = 1.6 mA	-	-	0.4	V
High-level high-impedance output current D_0-D_7	I_{ZH2}	V_{CC} = 5.25 V; V_O = 2.4 V; T_C = 125°C, 25°C	-	-	10	µA
High-level high-impedance output current A_0-A_{15}, R/W	I_{ZH1}	V_{CC} = 5.25 V; V_O = 2.4 V; T_C = 125°C, 25°C	-	-	100	µA
Low-level high-impedance output current D_0-D_7	I_{ZL2}	V_{CC} = 5.25 V; V_O = 0.4 V; T_C = 125°C, 25°C	-	-	-10	µA
Low-level high-impedance output current A_0-A_{15}, R/W	I_{ZL1}	V_{CC} = 5.25 V; V_O = 0.4 V; T_C = 125°C, 25°C	-	-	-100	µA
High-level input current $\overline{HALT}$, $\overline{RESET}$, TSC, $\overline{IRQ}$, $\overline{NMI}$, DBE	I_{IH1}	V_{IN} = 5.25 V; V_{CC} = 0 V; All other pins = 0 V; T_C = 125°C, 25°C	-	-	2.5	µA
High-level input current ϕ_1, ϕ_2	I_{IH2}	V_{IN} = 5.25 V; V_{CC} = 0 V; All other pins = 0 V, T_C = 125°C, 25°C	-	-	100	µA
Input clamp voltage	V_{IC}	(Pos) V_{IN} + 5.25 V	-	-	2.5	µA
		(NEG) I_O = 10 µA	-	-	-0.9	V
Input high threshold-all logic inputs	V_{IH1}	V_{CC} = 4.75 V; V_{CC} = 5.25 V	-	2.0	-	V
Input low threshold-all logic inputs	V_{IL1}		-	-	0.8	V
Clock input high threshold-clock inputs	V_{IH2}		-	V_{CC} -0.6	-	V

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions	Figure	Limits		Units
					Min	Max	
Clock input low threshold-clock inputs		V_{IL2}	V_{CC} = 4.75 V, V_{CC} = 5.25 V	-	-	0.4	V
Power supply current		I_{CC}		-	-	190	mA
Clock pulse width ϕ_1		$t_{\phi 1}$	-	7	430	9,500	ns
Clock pulse width ϕ_2		$t_{\phi 2}$	-	7	450	9,500	ns
Time between ϕ_1 trailing edge and ϕ_2 leading edge		t_{D1}	-	7	0	9,100	ns
Time between ϕ_2 trailing edge and ϕ_1 leading edge		t_{D2}	-	7	0	9,100	ns
Total time ϕ_1 and ϕ_2 are high		$t_{(\overline{DBE})W}$	-	7	940	-	ns
$\overline{DBE}$ pulse width (DBE down time)		$t_{(\overline{DBE})W}$	DBE must be at 0.8 V or less for at least T_{WL1} while ϕ_1 is at V_{CC} - 0.6 V level or higher	7	150	-	ns
ϕ_1 to $\overline{DBE}$ timing		t_{SLH1}	-	7	0	-	ns
ϕ_1 to $\overline{DBE}$ timing		t_{SHL1}	-	7	0	-	ns
TSC pulse width		$t_{(TSC)W}$	-	17,18	-	9.5	µs
$\overline{HALT}$ pulse width (setup)		$t_{(\overline{HALT})W1}$	$t_{(\overline{HALT})W1} \geq t_{SHL2}$	14	200	-	ns
		$t_{(\overline{HALT})W2}$	$t_{(\overline{HALT})W2} \geq t_{SLH2}$	15	200	-	ns
Processor controls setup times	$\overline{DRE}$ to ϕ_1	t_{SHL1}	-	7	300	-	ns
	$\overline{HALT}$ to ϕ_1	t_{SHL2}	$t_{SHL2} \leq t_{(\overline{HALT})W1}$	14	200	-	ns
		t_{SLH2}	$t_{SLH2} \leq t_{(\overline{HALT})W2}$	15	200	-	ns
		t_{SHL3}	-	15	200	-	ns
		t_{SLH3}	-	14	200	-	ns
	$\overline{Reset}$, $\overline{IRQ}$, $\overline{NMI}$ to ϕ_2	t_{SHL4}	-	12,13	200	-	ns
		t_{SLH4}	-	11,12, 13	200	-	ns

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Figure	Limits		Units
				Min	Max	
Processor control hold time TCS to ϕ_1	t_{HLH1}	-	17,18	-	40	ns
Read cycle data setup time D_0 - D_7 to ϕ_2	t_{SLH5}	-	8	100	-	ns
	t_{SHL5}	-	8	100	-	ns
Read cycle data hold time D_0-D_7 to ϕ_2	t_{HLH2}	-	8	10	-	ns
	t_{HHL2}	-	8	10	-	ns
Frequency of operation for ϕ_1 and ϕ_2	f	R_L = 2.2 k	5,7	0.1	1.0	MHz
Propagation delay time ① Read cycle for ϕ_1 to R/W ② Read and write cycles for ϕ_1 to VMA (A_0-A_{15})	t_{PLH1}	BA, R/W VMA D_0-D_7, A_0-A_{15} R = 24 kΩ; BA R = 11.7 kΩ; D_0-D_7	8,9	-	300	ns
Propagation delay time ① Write cycle for ϕ_1 to R/W ② Read or write cycles for ϕ_1 to (A_0-A_{15})	t_{PHL1}	R = 16.5 kΩ; A_0-A_{15}, R/W, VMA C = 30 pF; BA C = 130 pF; D_0-D_7 C = 90 pF; A_0-A_{15}, R/W, VMA	8,9	-	300	ns
Propagation delay time ① Write cycle for ϕ_1 to R/W ② Read and write cycles for ϕ_1 to (A_0-A_{15})	t_{PLH2}		8,9	10	-	ns
Propagation delay time ① Read cycle for ϕ_1 to R/W ② Read and write cycles for ϕ_1 to VMA or (A_0-A_{15})	t_{PHL2}		8,9	10	-	ns
Propagation delay time TSC to VMA or BA	t_{PLH3}		17,18	-	300	ns
	t_{PHL3}		17,18	-	300	ns

TABLE I. Electrical performance characteristics - Continued.

Test		Symbol	Conditions	Figure	Limits		Units
					Min	Max	
Propagation delay times during $\overline{HALT}$ mode	ϕ_1 to BA	t_{PHL4}	R_L = 2.2 k BA, R/W, VMA D_0-D_7, A_0-A_{15} R = 24 kΩ; BA R = 11.7 kΩ; D_0-D_7 R = 16.5 kΩ; A_0-A_{15}, R/W, VMA C = 30 pF; BA C = 130 pF; D_0-D_7 C = 90 pF; A_0-A_{15}, R/W, VMA	15	-	300	ns
	ϕ_2 to BA	t_{PLH4}		14,15	-	300	ns
Write cycle propagation delay times from a high-impedance state, DBE to (D_0-D_7)		t_{PZH2}		10	-	225	ns
		t_{PZL2}		10	-	225	ns
Write cycle propagation delay times to a high-impedance state, DBE to (D_0-D_7)		t_{PHZ1}		10	10	-	ns
		t_{PLZ1}		10	10	-	ns
Propagation delay times to a high-impedance state from TSC to R/W and (A_0-A_{15})		t_{PHZ2}		17	-	300	ns
		t_{PLZ2}		17	-	300	ns
A_0-A_{15}, R/W: $\overline{HALT}$, WAIT propagation delay timing		t_{PHZ3}		15,16	10	---	ns
		t_{PLZ3}		15,16	10	---	ns
A_0-A_{15}, R/W: propagation delay timing (in response to coming out of $\overline{HALT}$, WAIT, or TSC)		t_{PZH3}		15,16, 17	-	300	ns
		t_{PZL3}		15,16, 17	-	300	ns

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III, unless otherwise specified) 1/
	Class B devices
Interim electrical parameters (pre burn-in) (method 5004) (OPTIONAL)	1, 7B
Final electrical test parameters (method 5004)	*1- (test conditions 1-123) 2, 3, *7, 8A, 8B
Group A test requirements (method 5005)	1, 2, 3, 7, 8
Group B zap test	See 4.5.2
Group C and D end-point electrical parameters (method 5005)	1, 2, 7B, 8B
Additional electrical subgroups for group C periodic inspection	None

*PDA applies to subgroups 1 and 7A
1/ The letters "A" or "B" immediately following a specified subgroup refer to the respective input condition letter of table IIIA.

3.8 Certification. Certification in accordance with MIL-M-38510 is not required for this device.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Qualification inspection. Qualification inspection is not required.

4.3 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition D or E, using the circuit shown on figure 6, or equivalent.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

c. The percent defective allowable (PDA) for class B devices shall be 10 percent based on failures from group A, subgroup 1 test after cooldown as final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.3). Generic test data (see 6.7) may be used to satisfy the requirements for group C and D inspections. Quality conformance inspection shall be completed on the specific devices covered by this specification before they are shipped.

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group B inspection. Group B inspection shall consist of the test subgroups and LTPD values shown in table II of method 5005 of MIL-STD-883.

4.4.3 Groups C and D inspections. Groups C and D inspections shall consist of the test subgroups and LTPD values shown in tables III and IV of method 5005 of MIL-STD-883. Endpoint electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 High-voltage (V_{zap}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 400 V from a 100 pF source in the following test sequence. The internal protection network is shown on figure 3.

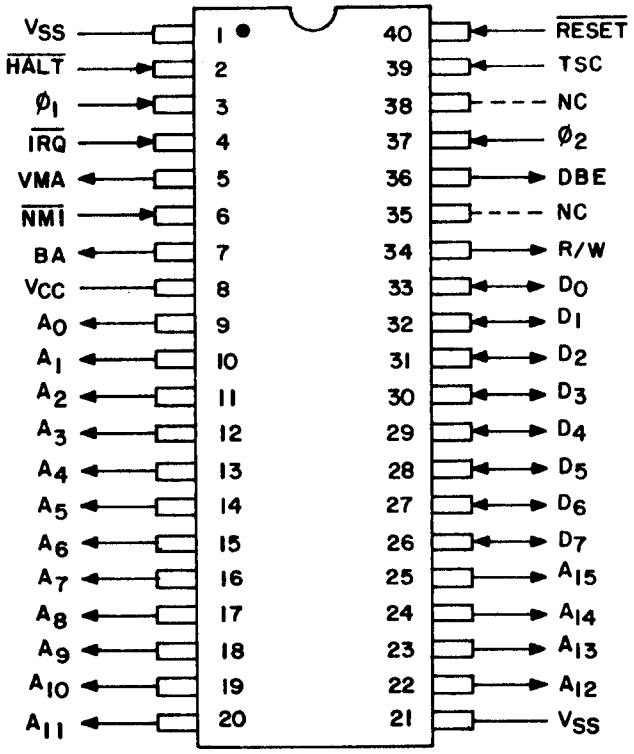
a. Measure I_{IH} at one input terminal of the device under test at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} shall be as specified in table III.

b. Apply the test voltage (V_{zap} = 400 V) to the same terminal selected for leakage current measurements. Apply V_{zap} in a 2 pulse sequence as follows and in accordance with the test circuit of figure 4.

1. Input (-) to V_{SS}.

2. Input (+) to V_{SS}.

c. Within 24 hours repeat the I_{IH} measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.



NOTE: Pin 1 is marked for orientation.

DEVICE TYPE 01, TOP VIEW

FIGURE 1. Terminal connections.

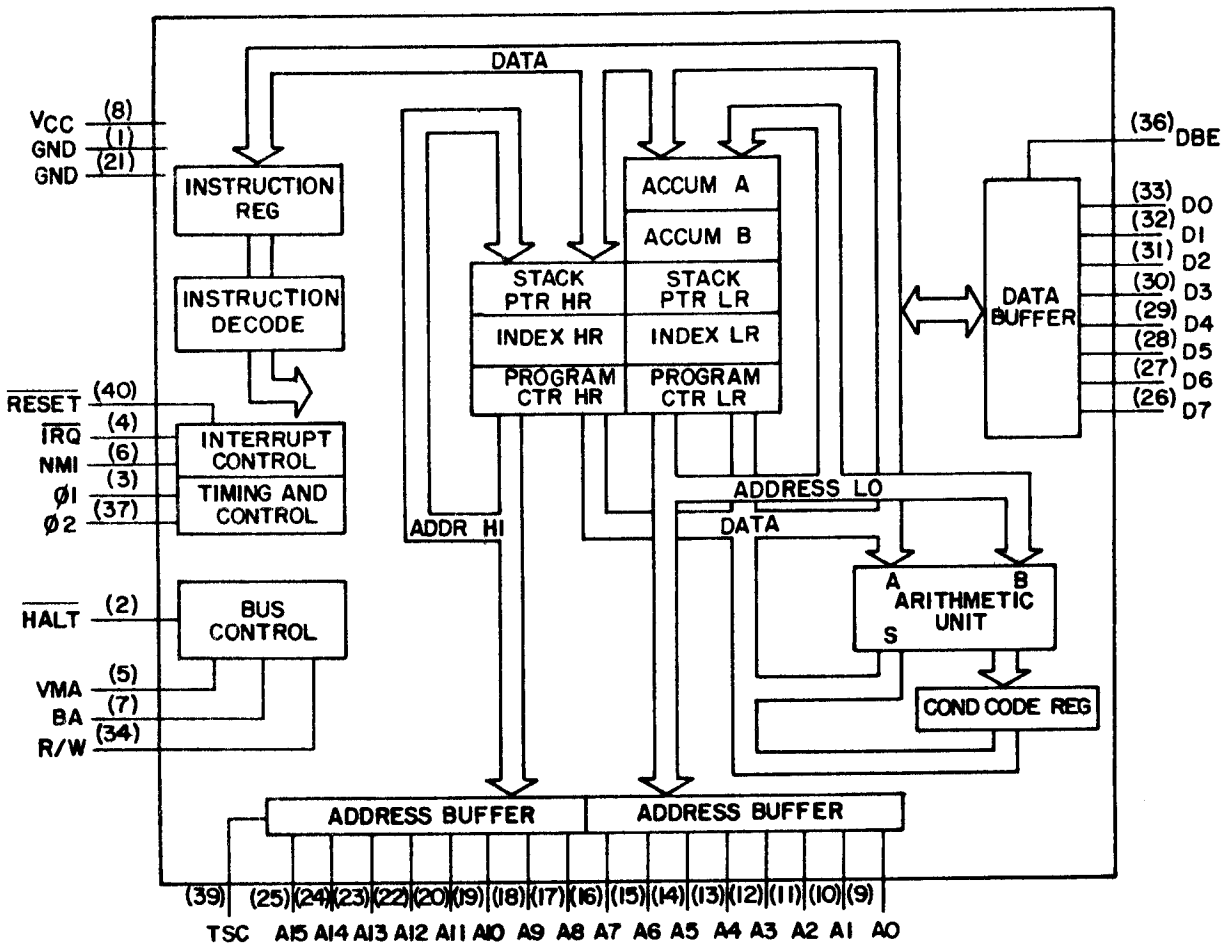


FIGURE 2. Functional block diagram.

TABLE IIIA. Input conditions for table IIIC.

Symbol	Terminals	Input conditions 1/					Unit	Figure
		A	B	C	D	E		
V_{CC}	V_{CC}	5.25	4.75	4.75	4.75	4.75	V dc	-
V_{IH1}	Logic inputs	2.0	2.0	2.0	2.0	2.0	"	"
V_{IL1}	Logic inputs	0.8	0.8	0.8	0.8	0.8	"	"
V_{IH2}	ø1, ø2	4.65	4.15	4.15	4.15	4.15	"	"
V_{IL2}	ø1, ø2	0.4	0.4	0.4	0.4	0.4	"	"
t_{Period}	ø1	1	1	10	10	10	µs	7
$t_{ø1}$	ø1	430	430	430	430	430	ns	"
$t_{ø2}$	ø2	450	450	450	450	9,500	"	"
t_{D1}	ø2	0	0	0	---	0	"	"
t_{D2}	ø2	---	---	---	0	---	"	"
$t_{\overline{(DBE)}W}$	DBE	150	150	150	DBE	DBE	"	"
t_{SHL1}	DBE	---	0	0	Equals	Equals	"	"
t_{SLH1}	DBE	0	---	---	ø2	ø2	"	"
t_{SLH5}	Data (In)	100	100	100	100	100	"	8
t_{SHL5}	"	100	100	100	100	100	"	"
t_{HHL2}	"	10	10	10	10	10	"	"
t_{HLH2}	"	10	10	10	10	10	"	"
$t_{\overline{(HALT)}W2}$	$\overline{HALT}$	200	---	200	---	---	"	15
$t_{\overline{(HALT)}W1}$	$\overline{HALT}$	200	---	200	---	---	"	14

See footnote at end of table.

TABLE IIIA. Input conditions for table IIIC - Continued.

Symbol	Terminals	Input conditions 1/						Figure
		A	B	C	D	E	Unit	
t_{SHL3}	$\overline{HALT}$	---	200	---	200	200	ns	15
t_{SLH3}	$\overline{HALT}$	---	"	---	"	"	"	14
t_{SLH4}	$\overline{Reset}$, $\overline{NMI}$, $\overline{IRQ}$	200	"	200	"	"	"	11,12,13, 16
t_{SHL4}	$\overline{Reset}$, $\overline{NMI}$, and $\overline{IRQ}$	200	"	200	"	"	"	12,13,16
t_{HLH1}	TSC	40	40	40	40	400	"	17, 18
$t_{(TSC)W}$	TSC	560	560	9,560	9,560	2,000	"	17, 18

1/ Rise and fall times (t_{TLH}, t_{THL}) for all input signals except for clock inputs and DBE (see figure 7) shall be 5 ns to 100 ns when measured from 0.9 to 1.9 V.

TABLE IIIB. Functional test output conditions for subgroups 7 and 8 for table IIIC.

Symbol	Measurement terminal	Figure	Test limits						Unit
			Subgroup 7 T_C = 25°C		Subgroup 8 T_C = -55°C		Subgroup 8 T_C = +125°C		
			Min	Max	Min	Max	Min	Max	
V_{OH}	All outputs	---	2.4	---	2.4	---	2.4	---	V
V_{OL}	All outputs	---	---	0.4	---	0.4	---	0.4	V
t_{PLH1}	R/W, A_0-A_{15}, VMA	8, 9	---	300	---	300	---	300	ns
t_{PHL1}	R/W, A_0-A_{15}	"	---	300	---	300	---	300	"
t_{PLH2}	R/W, A_0-A_{15}	"	10	---	10	---	10	---	"
t_{PHL2}	R/W, A_0-A_{15}, VMA	"	10	---	10	---	10	---	"

TABLE IIIB. Functional test output conditions for subgroups 7 and 8 for table IIIC - Continued.

Symbol	Measurement terminal	Figure	Test limits						Unit
			Subgroup 7 T_C = 25°C		Subgroup 8 T_C = -55°C		Subgroup 8 T_C = +125°C		
			Min	Max	Min	Max	Min	Max	
t_{PZH2} 1/	D_0-D_7	10	---	225	---	225	---	225	ns
t_{PZL2} 1/	D_0-D_7	"	---	225	---	225	---	225	"
t_{PHZ1}	D_0-D_7	"	10	---	10	---	10	---	"
t_{PLZ1}	D_0-D_7	"	10	---	10	---	10	---	"
t_{PHZ2}	A_0-A_{15},	17	---	300	---	300	---	300	"
t_{PLZ2}	R/W	17	"	"	"	"	"	"	"
t_{PLH3}	VMA, BA	17,18	"	"	"	"	"	"	"
t_{PHL3}	VMA, BA	17,18	"	"	"	"	"	"	"
t_{PLH4}	BA	14,15	"	"	"	"	"	"	"
t_{PHL4}	BA	15	"	"	"	"	"	"	"
t_{PZH3}	R/W, A_0-A_{15}	15,16	"	"	"	"	"	"	"
t_{PZL3}	A_0-A_{15}	"	"	"	"	"	"	"	"
t_{PLZ3}	R/W, A_0-A_{15}	"	10	---	10	---	10	---	"
t_{PHZ3}	R/W, A_0-A_{15}	"	10	---	10	---	10	---	"

1/ Conditions t_{PZH2} and t_{PZL2} shall be measured for only input condition (E) of table IIIA.

TABLE IIIC. Group A inspection.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		Min	Max	
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
1 T_C = 25°C	V_{IC} (Neg)		1	GND	I_0	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	2		-0.9	V
			2		GND	I_0	GND																	3			
			3			GND	I_0	GND																4			
			4				GND	I_0	GND															5			
			5					GND	I_0	GND														6			
			6						GND	I_0		GND												7			
			7							GND		I_0	GND											9			
			8									GND	I_0	GND										10			
			9										GND	I_0	GND									11			
			10											GND	I_0	GND								12			
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			12													GND	I_0	GND						14			
			13														GND	I_0	GND					15			
			14															GND	I_0	GND				16			
			15																GND	I_0	GND			17			
			16																	GND	I_0	GND		18			
			17																		GND	I_0	GND	19			
1 T_C = 25° C	V_{IC} (Neg)		18	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I_0	20		-0.9	V

See footnote at end of table.

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TABLE IIIC. Group A inspection.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/ 21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measurement terminal	Test limits Min	Test limits Max	Unit
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	ϕ_2	N.C.	TSC	$\overline{RST}$				
1 T_C = 25°C	V_{IC} (Neg)		1	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	2		-0.9	V
			2																					3			
			3																					4			
			4																					5			
			5																					6			
			6																					7			
			7																					9			
			8																					10			
			9																					11			
			10																					12			
			11																					13			
			12																					14			
			13																					15			
			14																					16			
			15																					17			
			16																					18			
			17																					19			
1 T_C = 25°C	V_{IC} (Neg)		18	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	20		-0.9	V

See footnote at end of table.

TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																		Measurement terminal	Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		Min	Max	
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
1 T_C = 25°C	V_{IC} (Neg)		19	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	22		-0.9	V
			20																				23			
			21																				24			
			22																				25			
			23																				26			
			24																				27			
			25																				28			
			26																				29			
			27																				30			
			28																				31			
			29																				32			
			30																				33			
			31																				34			
			32																				36			
			33																				37			
			34																				39			
1 T_C=25°C	V_{IC} (Neg)		35	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	40		-0.9	V

See footnote at end of table.

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TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
			Test No.	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		Min	Max	
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	ϕ_2	N.C.	TSC	$\overline{RST}$				
1 T_C = 25°C	V_{IC} (Neg)		19	GND	I_0	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	22		-0.9	V
			20		GND	I_0	GND	GND																23			
			21			GND	I_0	GND																24			
			22				GND	I_0	GND															25			
			23					GND	I_0	GND														26			
			24						GND	I_0	GND													27			
			25							GND	I_0	GND												28			
			26								GND	I_0	GND											29			
			27									GND	I_0	GND										30			
			28										GND	I_0	GND									31			
			29											GND	I_0	GND								32			
			30												GND	I_0	GND							33			
			31													GND	I_0	GND						34			
			32														GND		I_0	GND				36			
			33																GND	I_0		GND		37			
			34																GND	GND		I_0	GND	39			
1 T_C=25°C	V_{IC} (Neg)		35	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	I_0	40		-0.9	V

See footnote at end of table.

TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		Min	Max	
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
1 T_C=25°C	V_{IC} (Pos)		36	GND	GND	GND	GND	5.25	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5		2.5	µA
			37					GND		5.25		GND	GND											7			
			38							GND		5.25	GND											9			
			39									GND	5.25	GND										10			
			40										GND	5.25	GND									11			
			41											GND	5.25	GND								12			
			42												GND	5.25	GND							13			
			43													GND	5.25	GND						14			
			44														GND	5.25	GND					15			
			45															GND	5.25	GND				16			
			46																GND	5.25	GND			17			
			47																	GND	5.25	GND		18			
			48																		GND	5.25	GND	19			
			49																			GND	5.25	20			
			50																				GND	22			
			51																					23			
			52																					24			
1 T_C=25°C	V_{IC} (Pos)		53	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	25		2.5	µA

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TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		Min	Max	
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	ϕ_2	N.C.	TSC	$\overline{RST}$				
1 T_C=25°C	V_{IC} (Pos)		36	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5		2.5	µA
			37																					7			
			38																					9			
			39																					10			
			40																					11			
			41																					12			
			42																					13			
			43																					14			
			44																					15			
			45																					16			
			46																					17			
			47																					18			
			48																					19			
			49		GND																			20			
			50		5.25	GND																		22			
			51		GND	5.25	GND																	23			
			52		GND	GND	5.25	GND																24			
1 T_C=25°C	V_{IC} (Pos)		53	GND	GND	GND	GND	5.25	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	25		2.5	µA

See footnote at end of table.

TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																			Measurement terminal	Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		Min	Max	
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
1 T_C = 25°C	V_{IC} (Pos)		54	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	26		2.5	µA
			55																				27			
			56																				28			
			57																				29			
			58																				30			
			59																				31			
			60																				32			
			61																				33			
1 T_C=25°C	V_{IC} (Pos)		62		GND																		34			
2 T_C=125°C	I_{IH_1}	3010	63		5.25	GND																	2		2.5	
	I_{IH_2}		64		GND	5.25	GND																3		100	
	I_{IH_1}		65			GND	5.25		GND														4		2.5	
	I_{IH_1}		66				GND		5.25														6		2.5	
	I_{IH_1}		67						GND														36		2.5	
	I_{IH_2}		68																				37		100	
	I_{IH_1}		69																				39		2.5	
2 T_C=125°C	I_{IH_1}	3010	70	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	40		2.5	µA

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TABLE IIIC. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		Min	Max	
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	ϕ_2	N.C.	TSC	$\overline{RST}$				
1 T_C=25°C	V_{IC} (Pos)		54	GND	GND	GND	GND	GND	5.25	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	26		2.5	µA
			55						GND	5.25	GND	GND											27			
			56							GND	5.25	GND											28			
			57								GND	5.25	GND										29			
			58									GND	5.25	GND									30			
			59										GND	5.25	GND								31			
			60											GND	5.25	GND							32			
			61												GND	5.25	GND						33			
1 T_C=25°C	V_{IC} (Pos)		62													GND	5.25						34			
2 T_C=125°C	I_{IH1}	3010	63														GND						2		2.5	
	I_{IH_2}		64																				3		100	
	I_{IH_1}		65																				4		2.5	
	I_{IH_1}		66																GND				6		2.5	
	I_{IH_1}		67																5.25	GND			36		2.5	
	I_{IH_2}		68																GND	5.5		GND	37		100	
	I_{IH_1}		69																GND	GND		5.25	GND	39		2.5	
2 T_C=125°C	I_{IH_1}	3010	70	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	5.25	40		2.5	µA

See footnote at end of table.

TABLE IIIC. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/ 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measurement terminal	Test limits Min	Test limits Max	Unit
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
2 T_C=125°C	I_{IL_1}	3009	71	GND	GND	GND	0.4	GND	GND	GND	5.25	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	4	-10	-60	µA
	I_{IL_1}	3009	72	GND	GND	GND	GND	GND	0.4	GND	5.25	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	6	-10	-60	
	I_{ZL_1}		73		2.4	B	2.4	NC	0.4	NC	5.25	0.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	9		-100	
			74									2.4	0.4	2.4	2.4									10			
			75										2.4	0.4	2.4									11			
			76											2.4	0.4	2.4								12			
			77												2.4	0.4	2.4							13			
			78													2.4	0.4	2.4						14			
			79														2.4	0.4	2.4					15			
			80															2.4	0.4	2.4				16			
			81																2.4	0.4	2.4			17			
			82					NC		NC										2.4	0.4	2.4		18			
			83																		2.4	0.4	2.4	19			
			84																			2.4	0.4	20			
			85																				2.4	22			
			86																					23			
			87																					24			
T_C =125°C	I_{ZL_1}		88	GND	2.4	B	2.4		0.4		5.25	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	25		-100	µA

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TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/ 21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	Measurement terminal	Test limits Min	Test limits Max	Unit
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	ϕ_2	N.C.	TSC	$\overline{RST}$				
2 T_C=125°C	I_{IL_1}	3009	71	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	4	-10	-60	µA
	I_{IL_1}	3009	72	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	6	-10	-60	
	I_{ZL_1}		73		2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	0.4	B	2.4	2.4	2.4	9		-100	
			74																					10			
			75																					11			
			76																					12			
			77																					13			
			78																					14			
			79																					15			
			80																					16			
			81																					17			
			82															2.4			2.4			18			
			83		2.4																			19			
			84		0.4	2.4																		20			
			85		2.4	0.4	2.4																	22			
			86		2.4	2.4	0.4	2.4																23			
			87	GND	2.4	2.4	2.4	0.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4		0.4	B		2.4	2.4	24		-100	
2 T_C=125°C	I_{ZL_1}		88																					25			µA

See footnote at end of table.

TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/ 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	Measurement terminal	Test limits Min	Test limits Max	Unit
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
2 T_C=125°C	I_{ZL_2}		89	GND	2.4	B	2.4		0.4		5.25	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	26		-10	µA
			90																					27			
			91																					28			
			92																					29			
			93																					30			
			94																					31			
			95																					32			
	I_{ZL_2}		96																					33		-10	
	I_{ZL_1}		97										2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	34		-100	
	I_{ZH_1}		98									2.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	9		100	
			99									0.4	2.4	0.4	0.4									10			
			100										0.4	2.4	0.4									11			
			101											0.4	2.4	0.4								12			
			102											2.4	0.4	2.4	0.4							13			
			103											0.4		0.4	2.4	0.4						14			
			104														0.4	2.4	0.4					15			
			105														0.4	0.4	2.4	0.4				18			
2 T_C=125°C	I_{ZH_1}		106	GND	2.4	B	2.4		0.4		5.25	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	2.4	0.4	0.4	0.4	17		100	µA

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TABLE IIIC. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		Min	Max	
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	ϕ_2	N.C.	TSC	$\overline{RST}$				
T_C=125°C 2	I_{ZL_2}		89	GND	2.4	2.4	2.4	2.4	0.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4		0.4	B		2.4	2.4	26		-10	µA
			90						2.4	0.4	2.4	2.4												27			
			91							2.4	0.4	2.4												28			
			92								2.4	0.4	2.4											29			
			93									2.4	0.4	2.4										30			
			94										2.4	0.4	2.4									31			
			95											2.4	0.4	2.4								32			
	I_{ZL_2}		96		2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	0.4	2.4							33		-10	
	I_{ZL_1}		97		2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	2.4	0.4							34		-100	
	I_{ZH_1}		98		0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4								9		100	
			99																					10			
			100																					11			
			101																					12			
			102																			2.4	2.4	13			
			103																			0.4	0.4	14			
			104																					15			
			105																					18			
T_C=125°C 2	I_{ZH_1}		106	GND	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4		0.4	B		0.4	0.4	17		100	µA

See footnote at end of table.

TABLE IIIC. Group A inspection - Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/ 1 V_{SS}	2 $\overline{HLT}$	3 ϕ_1	4 $\overline{IRQ}$	5 VMA	6 $\overline{NMI}$	7 BA	8 V_{CC}	9 A_0	10 A_1	11 A_2	12 A_3	13 A_4	14 A_5	15 A_6	16 A_7	17 A_8	18 A_9	19 A_{10}	20 A_{11}	Measurement terminal	Test limits Min	Test limits Max	Unit
2 T_C=125°C	I_{ZH_1}		107	GND	2.4	B	2.4		0.4		5.25	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	2.4	0.4	0.4	18		100	µA
			108																		0.4	2.4	0.4	19			
			109																			0.4	2.4	20			
			110																				0.4	22			
			111																					23			
			112																					24			
	I_{ZH_1}		113																					25		100	
	I_{ZH_2}		114																					26		10	
			115																					27			
			116																					28			
			117																					29			
			118																					30			
			119																					31			
			120																					32			
	I_{ZH_2}		121																					33		10	
	I_{ZH_1}		122																					34		100	µA
2 T_C =125°C	I_{CC}	3005	123	GND	2.4	B	2.4		0.4		5.25	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	8		190	mA

PINS 21 THRU 40 ON NEXT PAGE

See footnote at end of table.

TABLE III. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		Min	Max	
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	$Ø_2$	N.C.	TSC	$\overline{RST}$				
2 T_C=125°C	I_{ZH_1}		107	GND	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4		0.4	B		0.4	0.4	18		100	µA
			108		0.4																			19			
			109		0.4																			20			
			110		2.4	0.4																		22			
			111		0.4	2.4	0.4																	23			
			112			0.4	2.4	0.4																24			
	I_{ZH_1}		113				0.4	2.4	0.4															25		100	
	I_{ZH_2}		114					0.4	2.4	0.4														26		10	
			115						0.4	2.4	0.4													27			
			116							0.4	2.4	0.4												28			
			117								0.4	2.4	0.4											29			
			118									0.4	2.4	0.4										30			
			119										0.4	2.4	0.4									31			
			120											0.4	2.4	0.4								32			
	I_{ZH_2}		121												0.4	2.4	0.4							33		10	
	I_{ZH_1}		122												0.4	0.4	2.4							34		100	µA
2 T_C=125°C	I_{CC}	3005	123	GND	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4	2.4		0.4	B		0.4	0.4	8		190	mA
3 T_C= -55°C	-	-	-	Repeat Subgroup 2 at -55°C.																							

See footnote at end of table.

TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																		Measurement terminal	Test limits		Unit
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20		Min	Max	
				V_{SS}	$\overline{HLT}$	ϕ_1	$\overline{IRQ}$	VMA	$\overline{NMI}$	BA	V_{CC}	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	A_8	A_9	A_{10}	A_{11}				
7 T_C =25°C ↓ 7 T_C=25°C	DYNAMIC FUNCTIONAL TESTS	3014, 3007, 3006, 3003 ↓	-	Input test condition A of table IIIA.																					
			-	Input test condition B of table IIIA.																					
			-	Input test condition C of table IIIA.																					
			-	Input test condition D of table IIIA.																					
			-	Input test condition E of table IIIA.																					
8		3014, 3007, 3006, 3003	-	Repeat subgroup 7 at +125°C.																					
8			-	Repeat subgroup 7 at -55°C.																					

PINS 21 THRU 40 ON NEXT PAGE

NOTE:

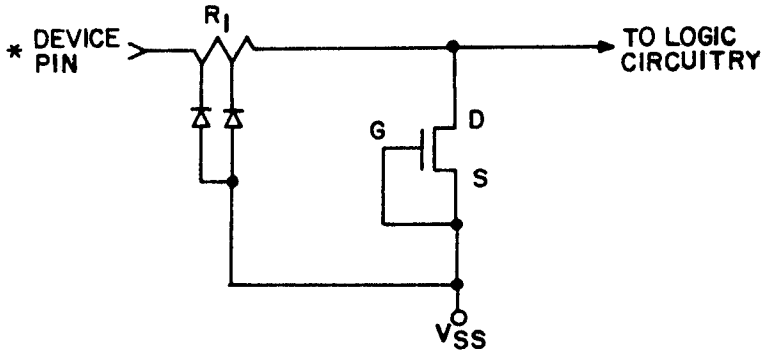
1/ I_O = -10 µA.

TABLE IIIC. Group A inspection -Continued.

Subgroup	Symbol	MIL-STD-883 method	Test No.	Terminal conditions (pins not designated are open) 1/																				Measurement terminal	Test limits		Unit
				21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40		Min	Max	
				V_{SS}	A_{12}	A_{13}	A_{14}	A_{15}	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	R/W	N.C.	DBE	$\emptyset_2$	N.C.	TSC	$\overline{RST}$				
7 T_C=25°C ↓ 7 T_C=25°C	DYNAMIC FUNCTIONAL TESTS	3014, 3007, 3006, 3003 ↓	-	Input test condition A of table IIIA.																						
			-	Input test condition B of table IIIA.																						
			-	Input test condition C of table IIIA.																						
			-	Input test condition D of table IIIA.																						
			-	Input test condition E of table IIIA.																						
8		3014, 3007, 3006, 3003	-	Repeat subgroup 7 at +125°C.																						
8			-	Repeat subgroup 7 at -55°C.																						

NOTE:

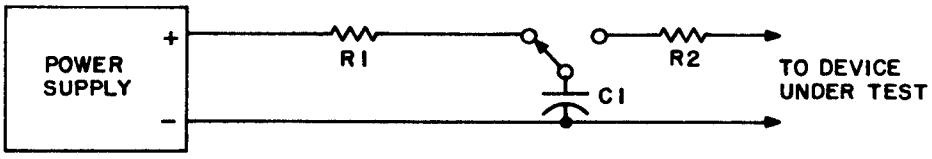
1/ I_O = -10 µA.



NOTES:
1. RI = 100Ω typical for clocks; 1 kΩ to 2 kΩ typical for all other inputs.
2. $B_{V_{DSS}}$ = 20 V to 30 V typical.

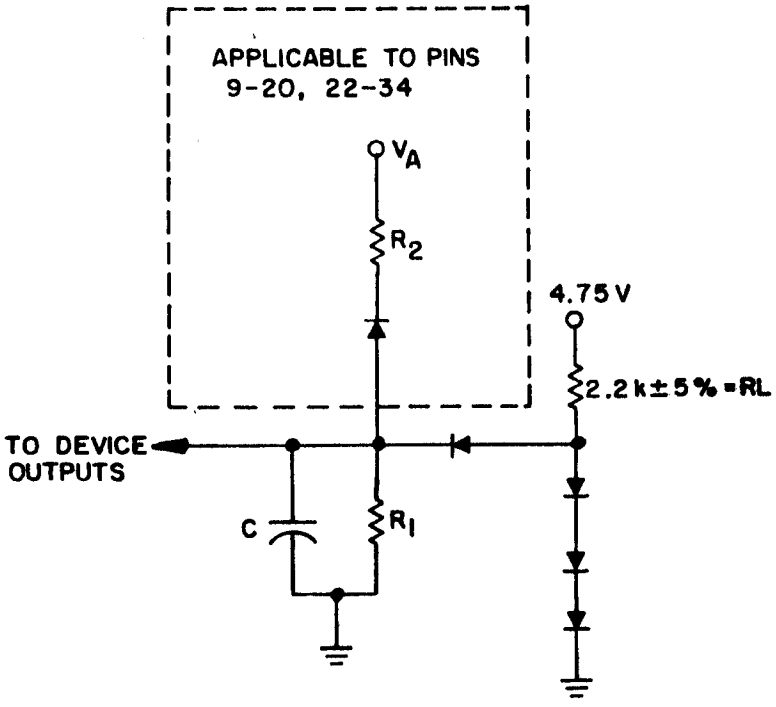
* Each device input pin excluding V_{CC}, V_{SS} and N. C. has an input protection device.

FIGURE 3. Device pin protection circuitry.



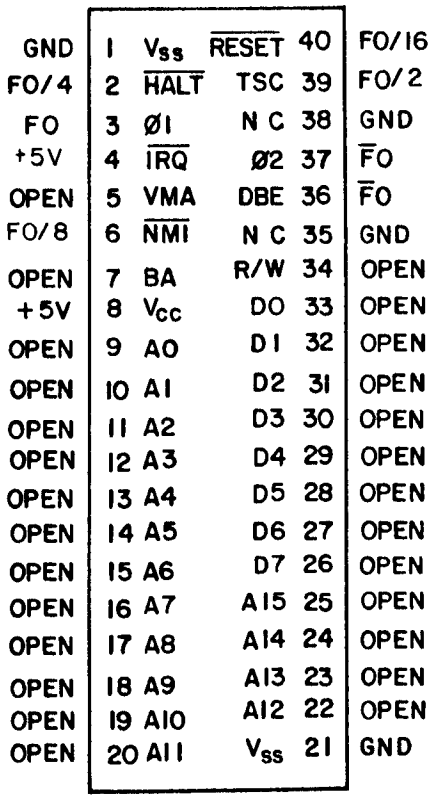
NOTES:
1. R1 = appropriate current limiting resistance.
2. R2 = 1.5 kΩ ±10%.
3. C1 = 100 pF ±20%.
4. V_{ZAP} = 400 V, measured at device input terminal.

FIGURE 4. High voltage (V_{ZAP}) test circuits.



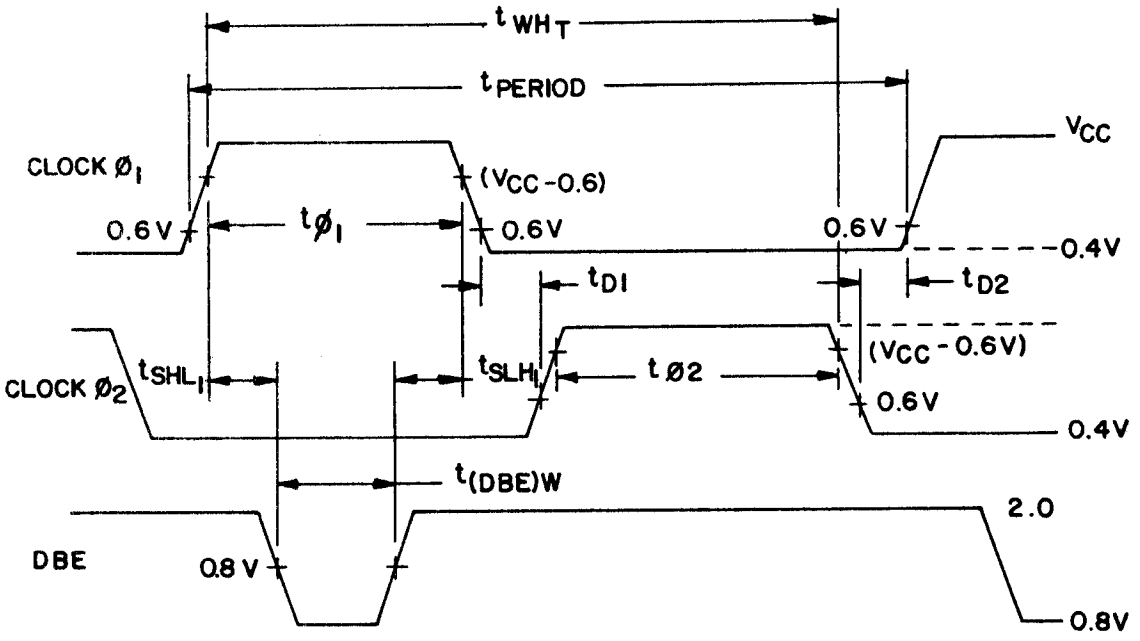
NOTES:
1. C = 30 pF ±5% for pin 7.
2. C = 90 pF ±5% for pins 5, 34, 9-20, 22-25.
3. C = 130 pF ±5% for pins 26-33.
4. C includes fixture capacitance.
5. R_1 = 24K ±5% for pin 7.
6. R_1 = 16.5K ±5% for pins 5, 34, 9-20, 22-25.
7. R_1 = 11.7K ±5% for pins 26-33.
8. Diodes - 1N4533 or equivalent.
9. R_2 = 1.1K ±5%.
10. V_A = +5.00 V for all functional tests except tristate tests.
11. V_A = -0.6 V for tristate tests.

FIGURE 5. Dynamic-functional load circuit.



NOTES:
1. V_{CC} = +5.0 V dc.
2. V_{SS} = 0 V dc.
3. FO = 100 kHz.
4. FO/2 = 50 kHz.
5. FO/4 = 25 kHz.
6. FO/8 = 12.5 kHz.
7. FO/16 = 6.25 kHz.

FIGURE 6. Burn-in and operating life-test circuit.



NOTES:
1. Clock, $t_{TLH} = t_{THL}$ = 30 ns; measured from 0.4 V to V_{CC} - 0.6 V.
2. DBE, $t_{TLH} = t_{THL}$ = 20 ns; measured from 0.9 V to 1.9 V.
3. t_{WHT} = total time $\emptyset_1$ and $\emptyset_2$ are high (includes delay between $\emptyset_1$ and $\emptyset_2$) = 940 ns minimum.
4. DBE must be at 0.8 V or less for at least $t_{(DBE)W}$ while $\emptyset_1$ is at V_{CC} - 0.6 volts or greater.

FIGURE 7. Clock waveforms.

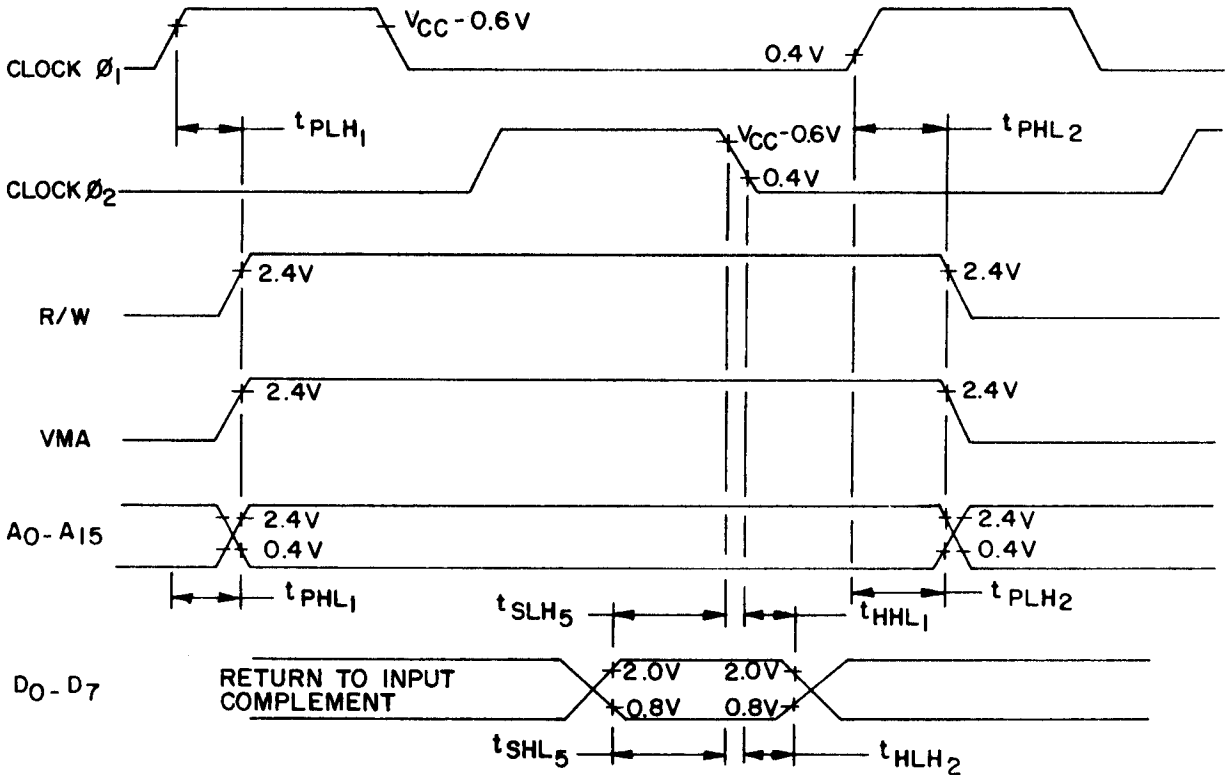


FIGURE 8. Read cycle timing.

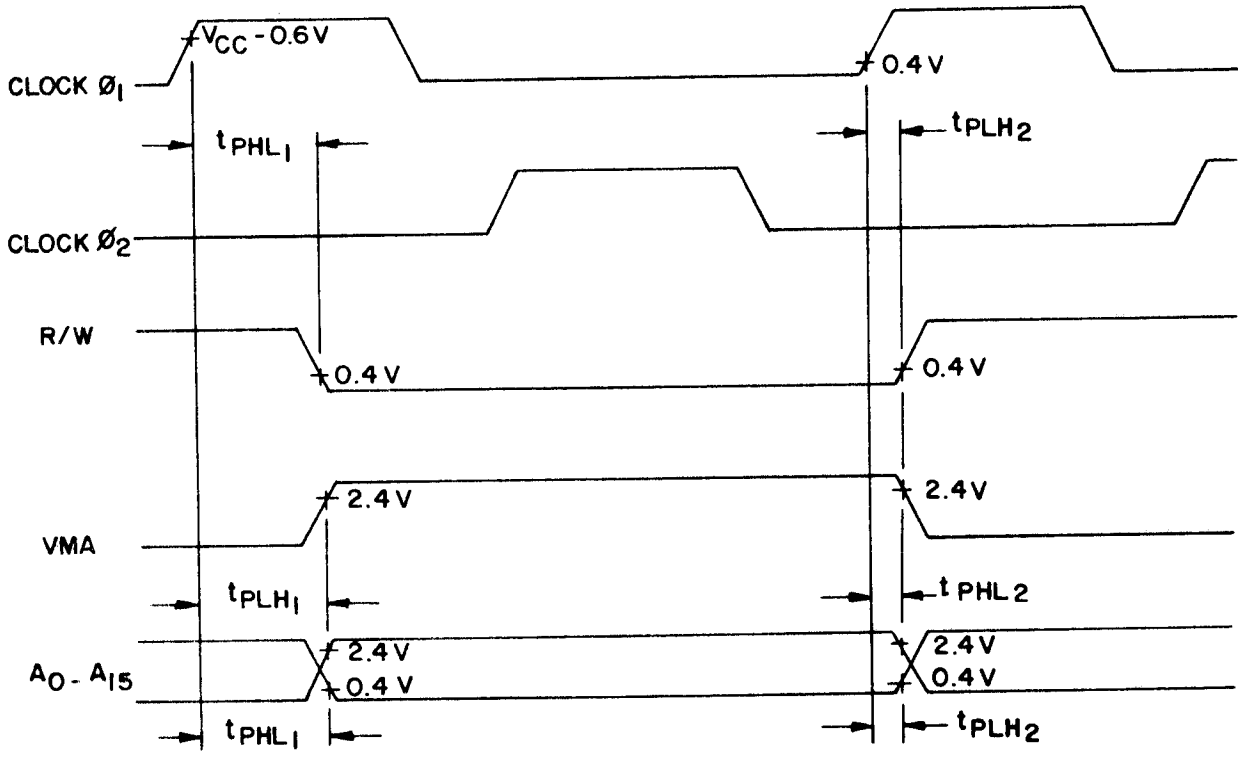


FIGURE 9. Write cycle timing.

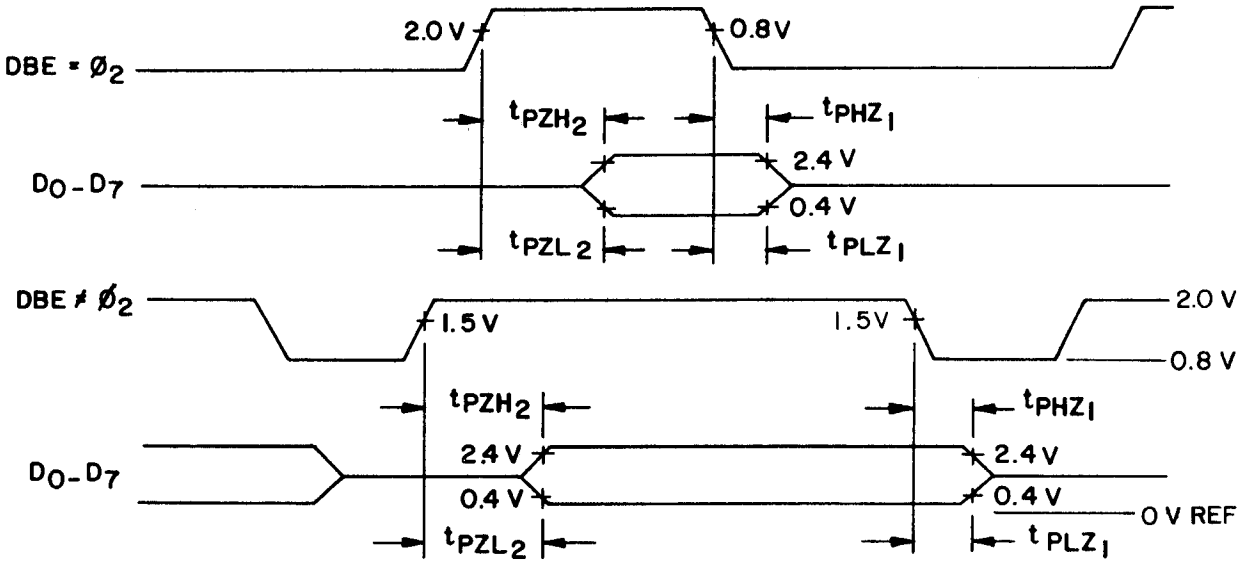


FIGURE 10. Write cycle timing.

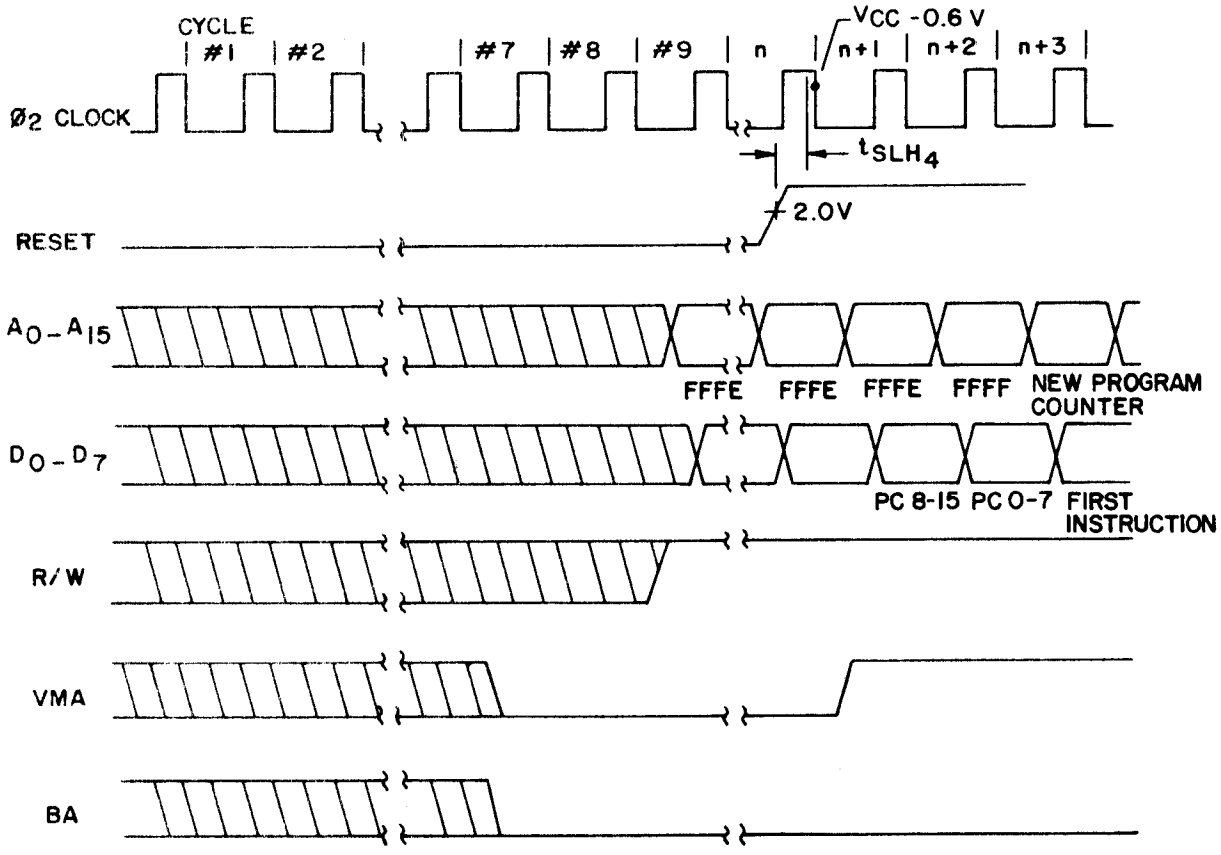


FIGURE 11. Power up-reset timing.

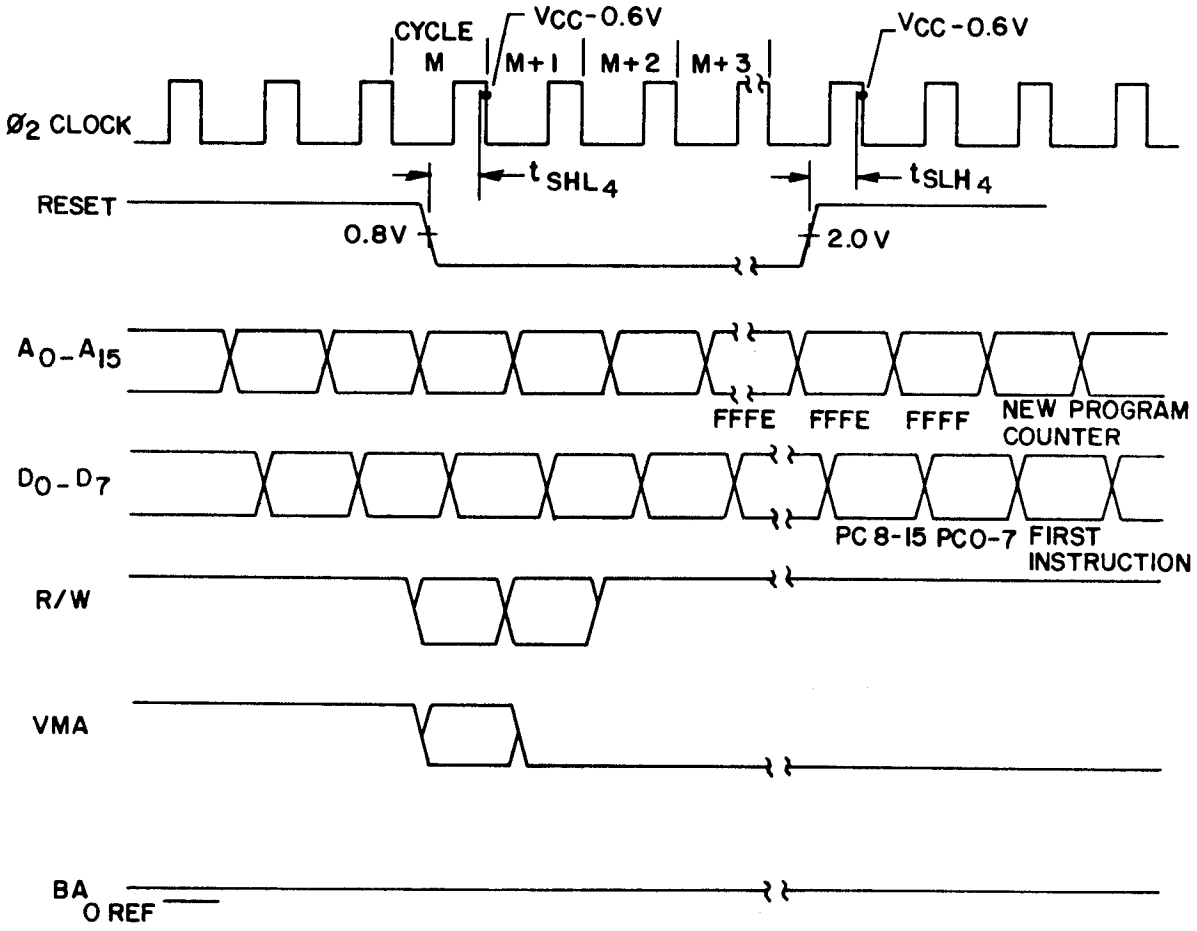


FIGURE 12. Processor reinitialization - reset timing.

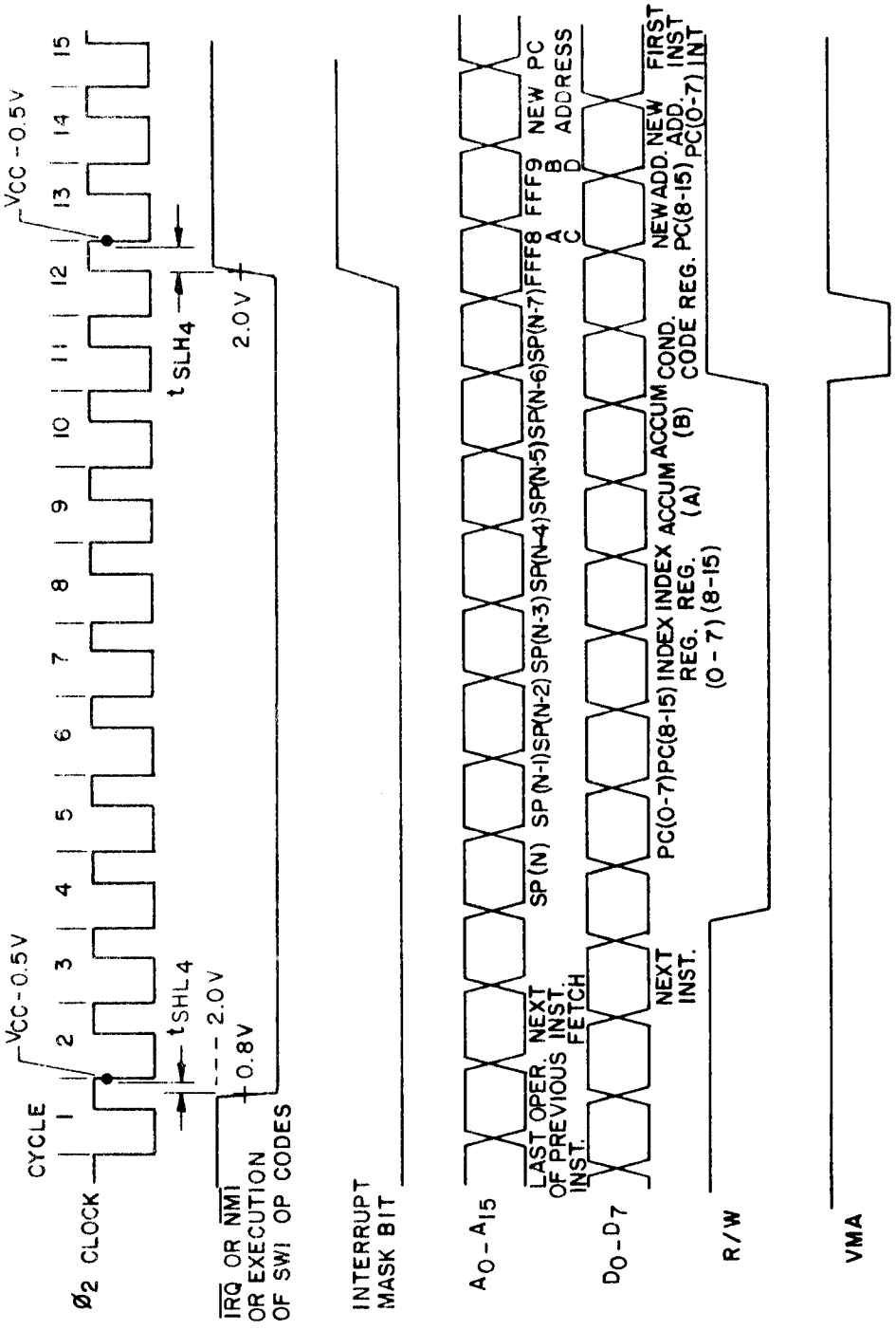


FIGURE 13. Interrupt timing $\overline{IRQ}$, $\overline{NMI}$ and execution of SWI OP code.

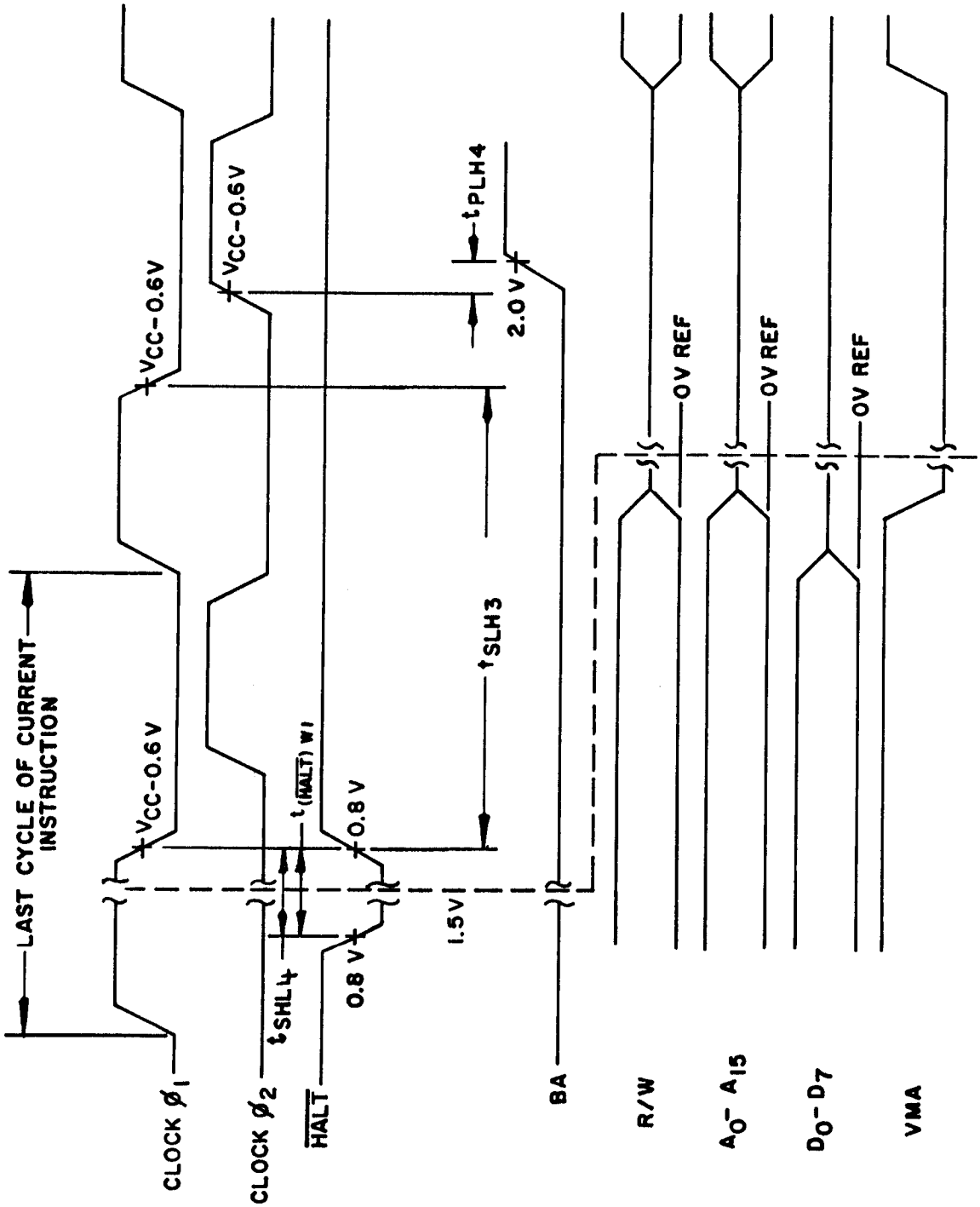


FIGURE 14. Normal HALT cycle.

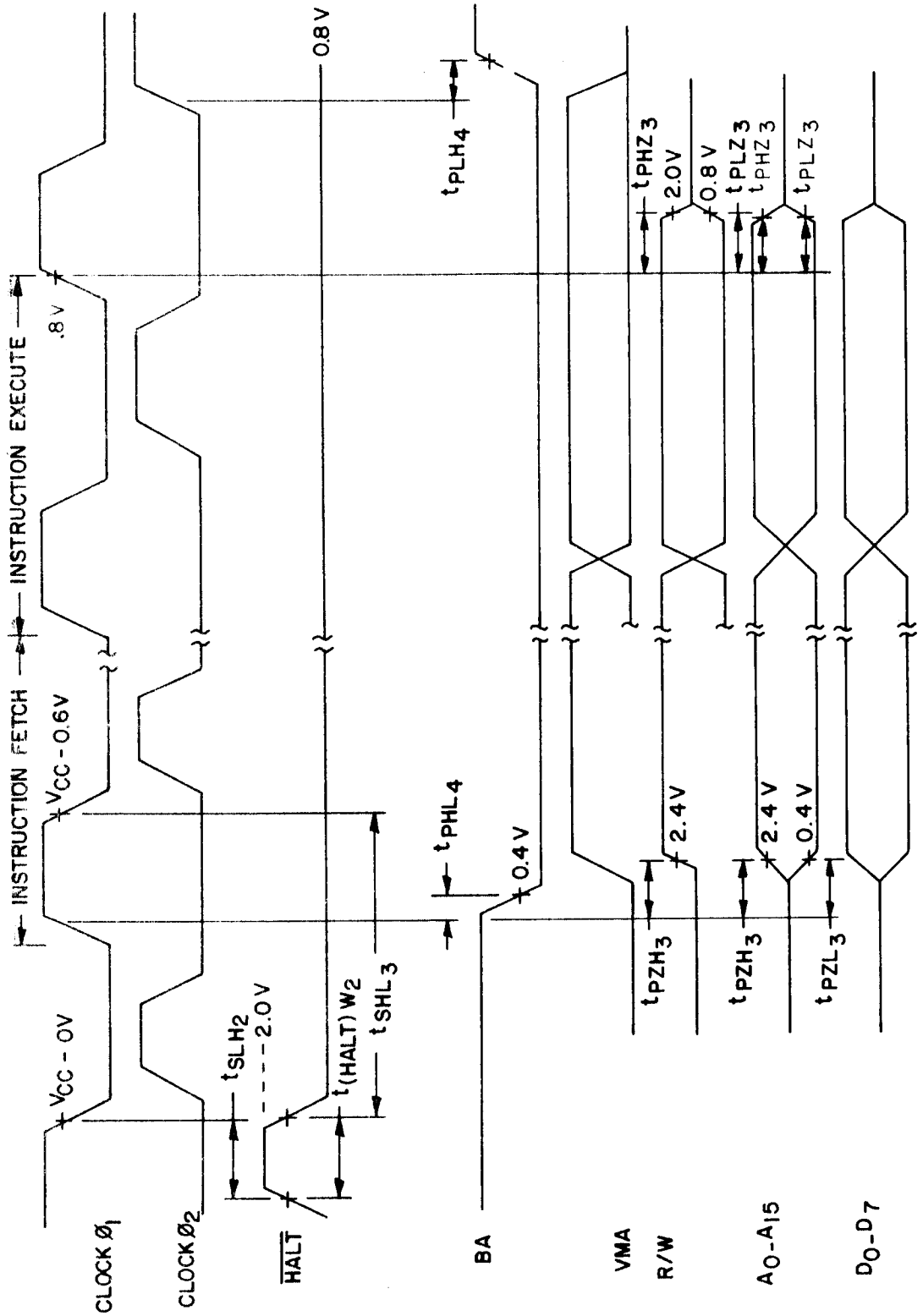


FIGURE 15. HALT - single instruction execute.

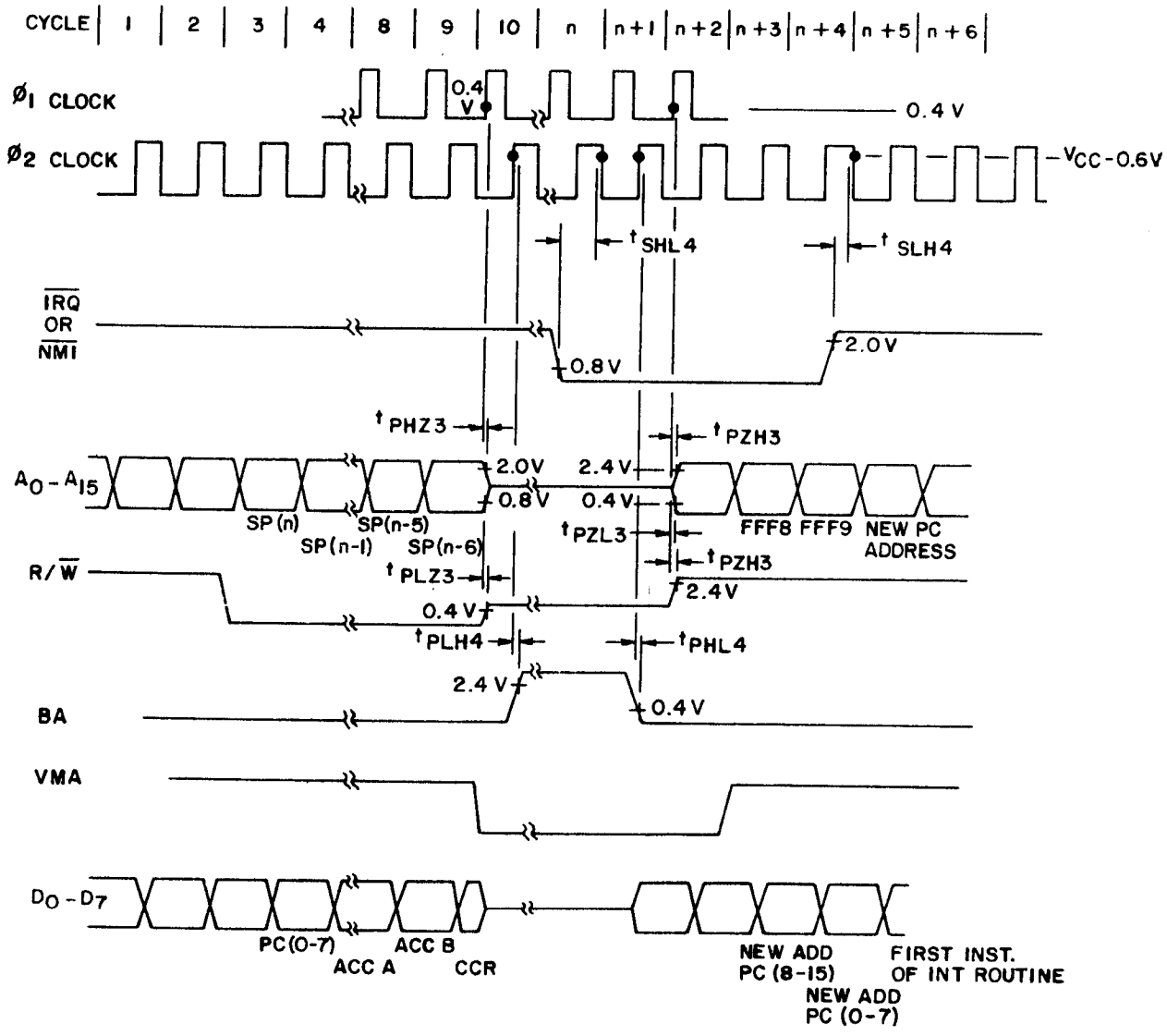


FIGURE 16. Wait for interrupt instruction timing.

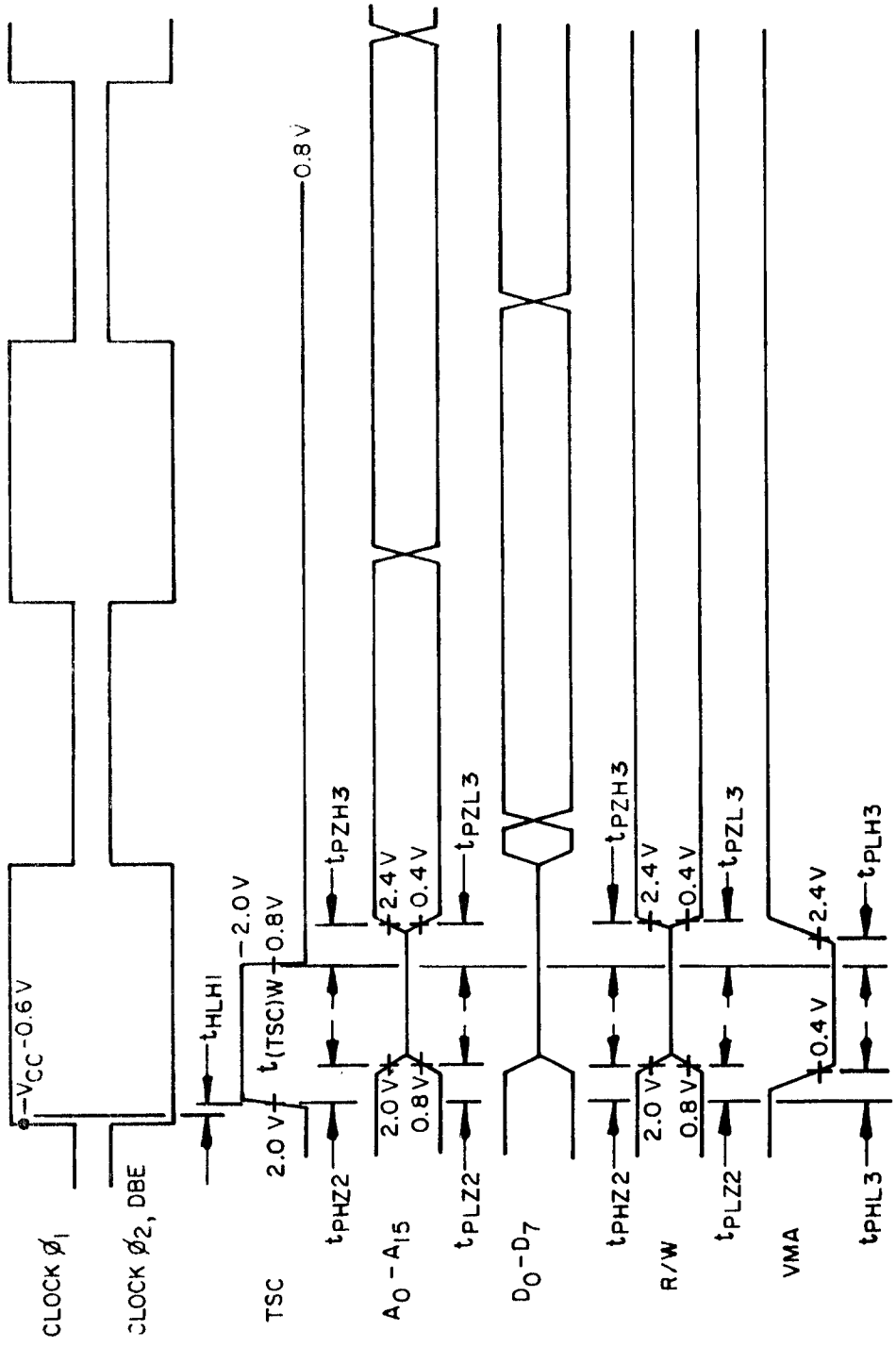


FIGURE 17. TSC timing conditions.

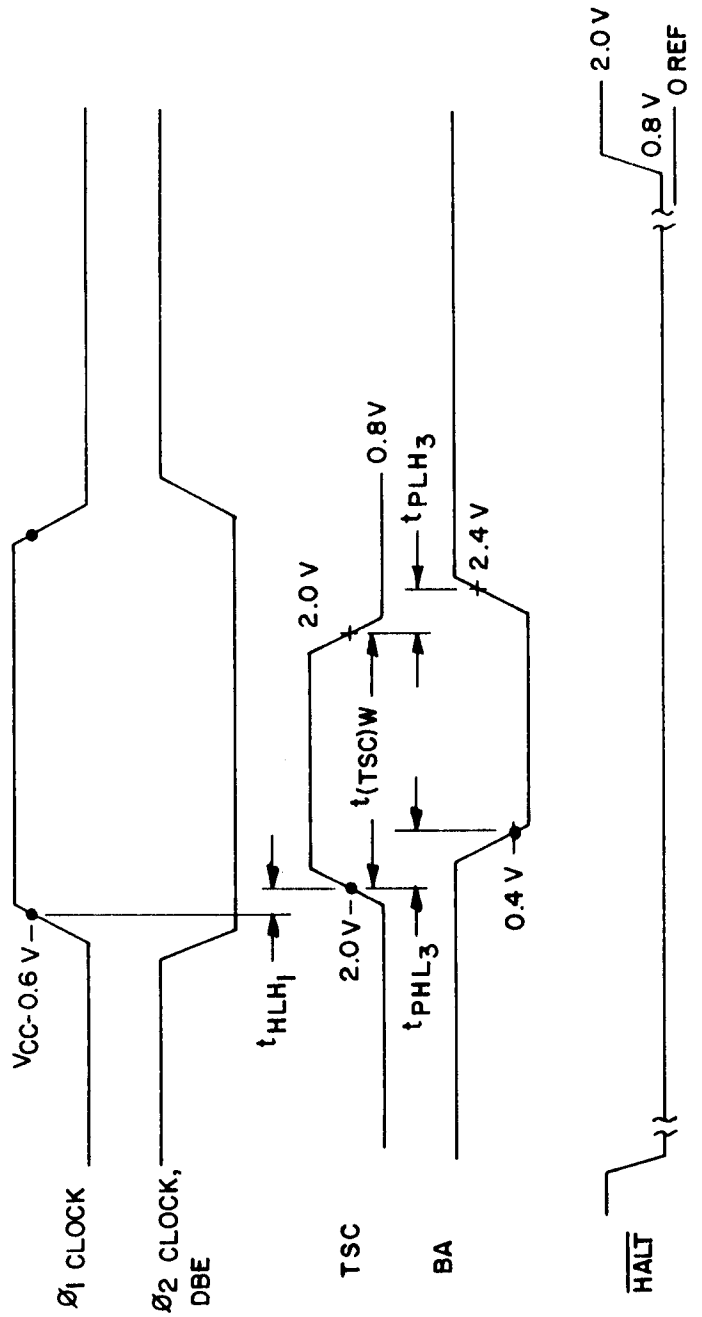


FIGURE 18. TSC timing.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging of microcircuits shall be in accordance with MIL-M-38510. In addition, all devices shall be in contact with a conductive material which shorts all leads together to prevent electrostatic damage.

6. NOTES

6.1 Notes. The notes specified in MIL-M-38510 are applicable to this specification.

6.2 Computer generated table. Table V, which forms a part of this specification, is not printed herein because of its extreme length; and, even when presented as hard copy requires conversion to on-line format. When the entire sequence of vector groups is needed for driving devices as part of inspection, a test program output should be obtained in a form compatible with test system architecture (magnetic tape format usually preferred). The preparing activity (or DESC, as its agent) may be consulted for information on obtaining such output. For referee purposes, Rome Air Development Center (RADC-RBE-2) and Defense Electronics Supply Center (DESC-ECS) each maintain a limited quantity of dated, hard copy printouts of this table.

6.3 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.4 Ordering data. The acquisition document should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity, if applicable.

e. Requirements for packaging and packing (see 5.1). Appropriate level of MIL-M-55565 must be specified.

f. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

6.5 Terms and definitions. The abbreviations, terms, symbols and definitions used herein (including terms and symbols for device terminals) are defined in MIL-STD-1313, MIL-STD-1331, and as follows.

Clock inputs (ø1, ø2). These inputs are the two-phase non-overlapping clocks.

Address bus (A0-A15). These outputs are three-state bus drivers. When the output is turned off, it is essentially an open circuit. This permits the microprocessor to be used in DMA applications.

Data bus (D0-D7). The data bus is bi-directional, transferring data to and from the memory and peripheral devices. It also has three-state output buffers.

Halt. When this input is in the low state, all activity in the machine will be halted. In the halt mode, the machine will stop at the end of an instruction, bus available will be at a one level, valid memory address will be at a zero, and all other three-state lines will be in the three-state mode.

Read/Write (R/W). This output signals the peripherals and memory devices whether the microprocessor is in a read (high) or write (low) state. The normal standby state of this signal is read (high). Three-state control going high will turn read/write to the off (high-impedance) state. Also, when the processor is halted, it will be in the off state.

Valid memory address (VMA). This output indicates to peripheral devices that there is a valid address on the address bus. In normal operation, this signal should be utilized for enabling peripheral interfaces. This signal is not three-state.

Interrupt request (IRQ). This input requests that an interrupt sequence be generated within the machine. The processor will wait until it completes the current instruction that is being executed before it recognizes the request. At that time, if the interrupt mask bit in the condition code register is not set, the machine will begin an interrupt sequence. The index register, program counter, accumulators, and condition code register are stored away on the stack. Next the microprocessor will respond to the interrupt request by setting the interrupt mask bit high so that no further interrupts may occur. Then a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFF8 and FFF9. An address loaded at these locations cause the microprocessor to branch to an interrupt routine in memory.

The halt line must be in the high state for interrupts to be serviced. Interrupts will be latched internally while halt is low.

The IRQ has a high-impedance pullup device internal to the chip; however a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Reset. The reset is used to reset and start the microprocessor from a power-down condition resulting from a power failure or initial start-up of the processor. This input can also be used to reinitialize the machine at any time after start up.

If a high level is detected in this input, this will signal the microprocessor to begin the reset sequence. During the reset sequence, the contents of the last two locations (FFFE, FFFF) in memory will be loaded into the program counter to point to the beginning of the reset routine. During the reset routine, the interrupt mask bit is set and must be cleared under program control before the microprocessor can be interrupted by IRQ. While reset is low (assuming a minimum of eight clock cycles have occurred) the microprocessor output signals will be in the following states: VMA = low, BA = low, data bus = high impedance, R/W = high (read state), and the address bus will contain the reset address FFFE. The reset control line may also be used to reinitialize the microprocessor system at any time during its operation. This is accomplished by pulsing reset low for the duration of a minimum of three complete ø2 cycles.

Three-state control (TSC). When the three-state control (TSC) line is a logic "1", the address bus and the R/W line are placed in a high-impedance state. VMA and BA are forced low whenever TSC = "1" to prevent false reads or writes on any device enabled by VMA. While TSC is held high, the ø1 and ø2 clocks must be held high and low, respectively, in order to delay program execution (this is required because of the bus lines being in an indeterminate state). Since the MPU is a dynamic device, the ø1 clock can be stopped for a maximum time PWH_1, without destroying data within the microprocessor. TSC then can be used in a short direct memory access (DMA) application.

Bus available (BA). The bus available signal will normally be in the low state; when activated, it will go to the high state indicating that the microprocessor has stopped and that the address bus is available. This will occur if the halt line is in the low state, or if the processor is in the WAIT state as a result of the execution of a WAIT instruction. At such time, all three-state output drivers will go to their off state and other outputs to their normally inactive level. The processor is removed from the WAIT state by the occurrence of a maskable (mask bit 1 = 0) or nonmaskable interrupt. Note that if TSC is in the high state, bus available will be low.

Data bus enable (DBE). DBE is the three-state control signal for the microprocessor data bus and will enable the bus drivers when in the high state. This input is TTL compatible; however, in normal operation, it would be driven by the ø2 clock. During a microprocessor read cycle, the data bus drivers will be disabled internally. When it is desired that another device control the data bus such as in DMA applications, DBE should be held low.

Nonmaskable interrupt (NMI). A low-going signal on this input requests that a non-mask-interrupt sequence be generated within the processor. As with the interrupt request signal, the processor will complete the current instruction that is being executed before it recognizes the NMI signal. The interrupt mask bit in the condition code register has no effect on NMI.

The index register, program counter, accumulators, and condition code register are stored away on the stack. Next a 16-bit address will be loaded that points to a vectoring address which is located in memory locations FFFC and FFFD. An address loaded at these locations causes the microprocessor to branch to a nonmaskable interrupt routine in memory.

NMI has a high-impedance pullup resistor internal to the chip; however, a 3 kΩ external resistor to V_{CC} should be used for wire-OR and optimum control of interrupts.

Inputs IRQ and NMI are hardware interrupt lines that are sampled during ø2 and will start the interrupt routine on the ø1 following the completion of an instruction.

The execution of a WAIT instruction speeds up the microprocessor's response to the interrupt because the stacking of the PC, IX, ACCX, and the CCR is already done. While the microprocessor is waiting for the interrupt, bus available will go high indicating the following states of the control lines: VMA is low, and the address bus R/W and data bus are all in the high-impedance state.

6.6 Logistic support. Lead materials and finishes (see 3.3), are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.7 Generic test data. Generic test data may be used to satisfy the requirements of 4.4.3. Group C generic test data shall be on date codes no more than one year old and on a die in the same microcircuit group (see appendix E of MIL-M-38510) with the same material, design and process and from the same plant as the die represented. Group D (see 4.4.3) generic data shall be on date codes no more than one year old and on the same package type (see terms, definitions, and symbols of MIL-M-38510) and from the same plant as the package represented. The vendor is required to retain the generic data for a period of not less than 36 months from the date of shipment.

6.8 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed Generic-Industry type. Generic-Industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of Generic-Industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	6800

6.9 Handling. MOS microprocessors should be handled with certain precautions to avoid damage due to the accumulation of static charge. These NMOS devices are fabricated with a silicon gate technology, including input protection, which reduces the susceptibility to damage. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or conductive carriers.

e. Avoid use of plastic, rubber, or silk in areas where NMOS devices are handled.

f. Maintain relative humidity above 50 percent.

6.10 Ordering guidance. Since the qualification and certification requirements have been removed from the specification, orders may be placed immediately.

6.11 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Air Force - 11, 19, 85, 99
Navy - OS, SH
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Agent:
DLA - ES

Preparing activity:
Air Force - 17

(Project 5962-0591-9)