MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, CMOS, 65,536-BIT STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, 65,536-bit, static random access memory microcircuits (including those with a power down data retention feature). Two product assurance classes and a choice of case outlines and lead finishes are provided and are reflected in the complete part number.

1.2 Part number. The complete part number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as follows:

Device type	Device organization	Data retention	Access/cycle time
01	65,536/1-bit RAM	No	55/55 ns
02	65,536/1-bit RAM	No	45/45 ns
03	65,536/1-bit RAM	Yes	55/55 ns
04	65,536/1-bit RAM	Yes	70/70 ns
05	8192 x 8-bit RAM (asynchronous)	Yes	150/150 ns
06	8192 x 8-bit RAM (synchronous)	Yes	150/205 ns

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Outline letter	Case outline (see MIL-M-38510, appendix C)
T	See figure 1 (22-lead, .300" x 1.26"), dual-in-line package
U	See figure 1 (22-terminal, .290" x .490"), leadless chip carrier package
X	D-10 (28-lead, 1/2" x 1 3/8"), dual-in-line cerdip package
Y	C-12 (32-terminal, .450" x .550"), leadless chip carrier package

1.3 Absolute maximum ratings.

Voltage on any pin relative to V_{SS}	-.5 V to V_{CC} +.5 V
Storage temperature range (ambient)	-65°C to +150°C
Maximum dc output current	50 mA
Power dissipation (P_D)	1.0 W
Lead temperature (soldering, 5 seconds)	+270°C
Junction temperature (T_J)	+150°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case T	30°C/W
Case U	50°C/W
Case X	15°C/W
Case Y	40°C/W

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441-5700, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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1.4 Recommended operating conditions.

Supply voltage (V_{CC}):	
Device types 01 through 06 - - - - - - - - - - - -	4.5 V dc to 5.5 V dc
Case operating temperature range (T_C)- - - - - - - -	-55°C to +125°C
Data retention supply voltage (V_{DR}):	
Device types 03, 04, 05, and 06- - - - - - - - - -	2.0 V dc to 5.5 V dc
V_{SS} power supply and signal ground - - - - - - - - -	0.0 V dc
High level input voltage, all inputs (V_{IH}):	
Device types 01 through 04 - - - - - - - - - - - - -	2.2 V dc to V_{CC}
Device types 05 and 06 - - - - - - - - - - - - - - -	2.2 V dc to V_{CC} + .3
Low level input voltage, all inputs (V_{IL}):	
Device types 01 through 04 - - - - - - - - - - - - -	-0.5 V dc to +0.8 V dc
Device types 05 and 06 - - - - - - - - - - - - - - -	-0.3 V dc to +0.8 V dc

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by contractors in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets, or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.2 Block diagrams. The block diagrams shall be as specified on figure 3.

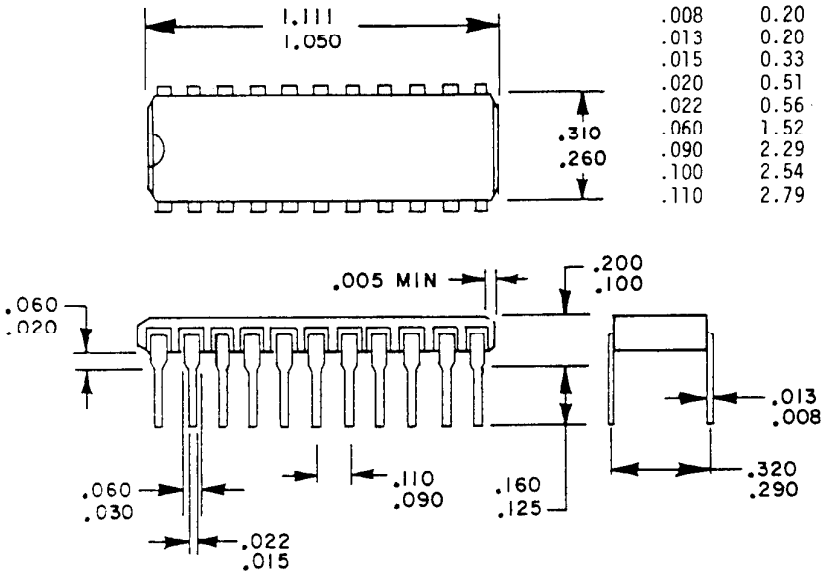
3.2.3 Truth table. The truth table shall be as specified on figure 4.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3 and on figure 1.

Continued on page 10

(22-LEAD, .300" X 1.26", DUAL-IN-LINE PACKAGE)

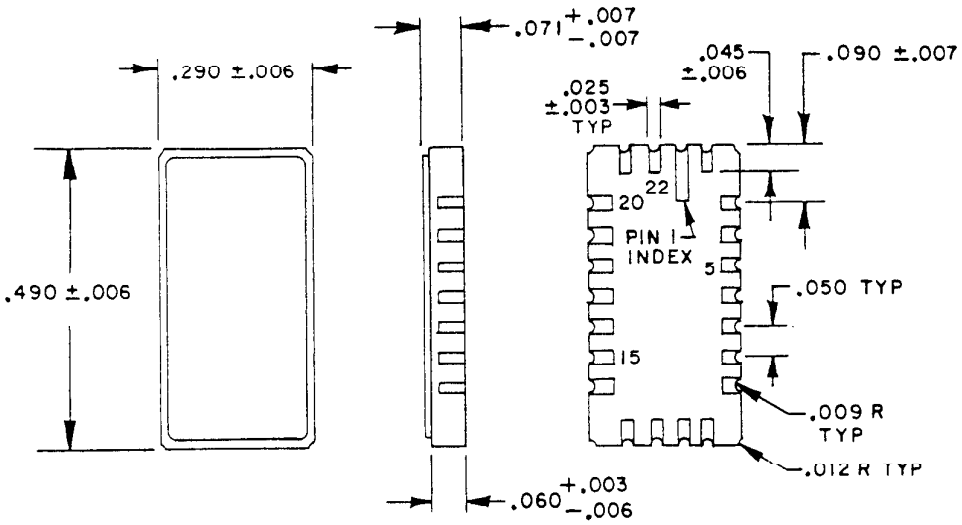
CASE T



Inches	mm	Inches	mm
.005	0.13	.125	3.18
.008	0.20	.160	4.06
.013	0.20	.200	5.08
.015	0.33	.260	6.60
.020	0.51	.290	7.37
.022	0.56	.310	7.87
.060	1.52	.320	8.13
.090	2.29	1.050	26.67
.100	2.54	1.111	28.22
.110	2.79		

(22-TERMINAL, .290" X .490", LEADLESS CHIP CARRIER PACKAGE)

CASE U



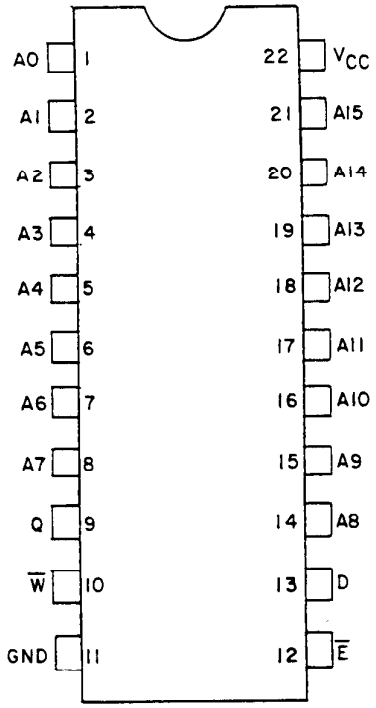
Inches	mm
.003	0.08
.006	0.15
.007	0.18
.009	0.23
.012	0.30
.025	0.64
.045	1.14
.050	1.27
.060	1.52
.071	1.80
.090	2.29
.290	7.37
.490	12.45

FIGURE 1. Case outlines.

Device types 01, 02, 03 and 04

22-PIN DIP (TOP VIEW)

CASE T



22-PIN LEADLESS CHIP CARRIER (TOP VIEW)

CASE U

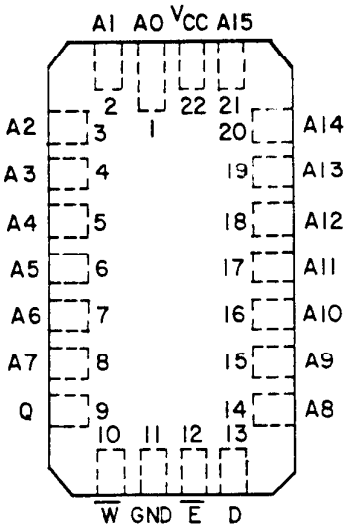
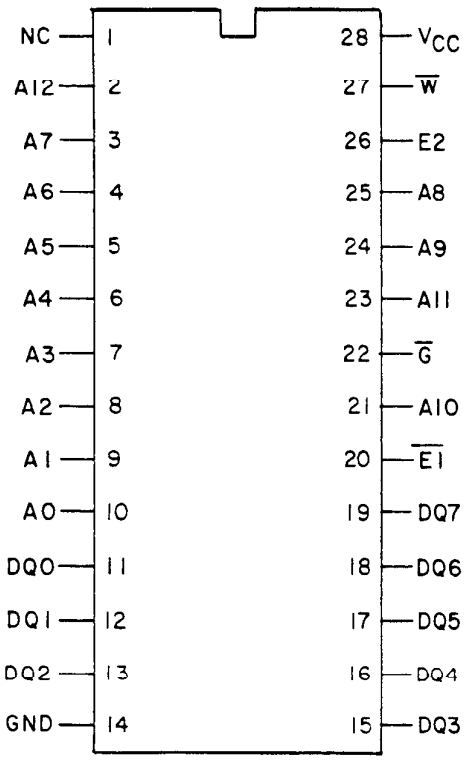


FIGURE 2. Terminal connections.

Device types 05 and 06

28-PIN DIP (TOP VIEW)

CASE X



32-PIN
LEADLESS CHIP CARRIER (TOP VIEW)

CASE Y

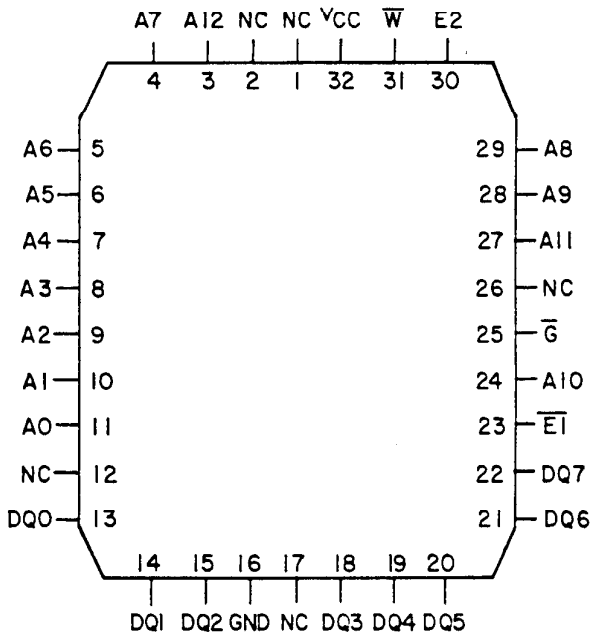


FIGURE 2. Terminal connections - Continued.

Device types 01, 02, 03, and 04

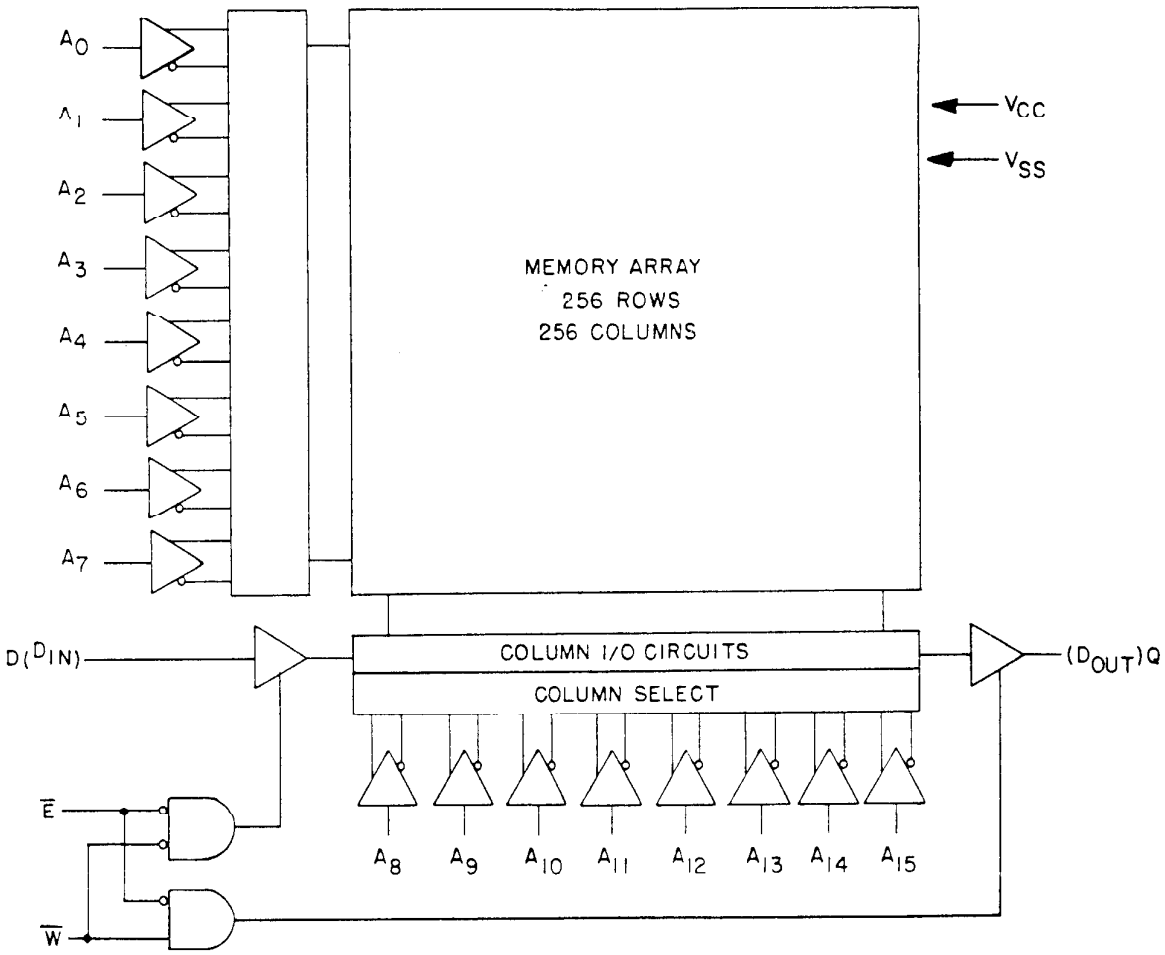


FIGURE 3. Block diagram.

Device type 05

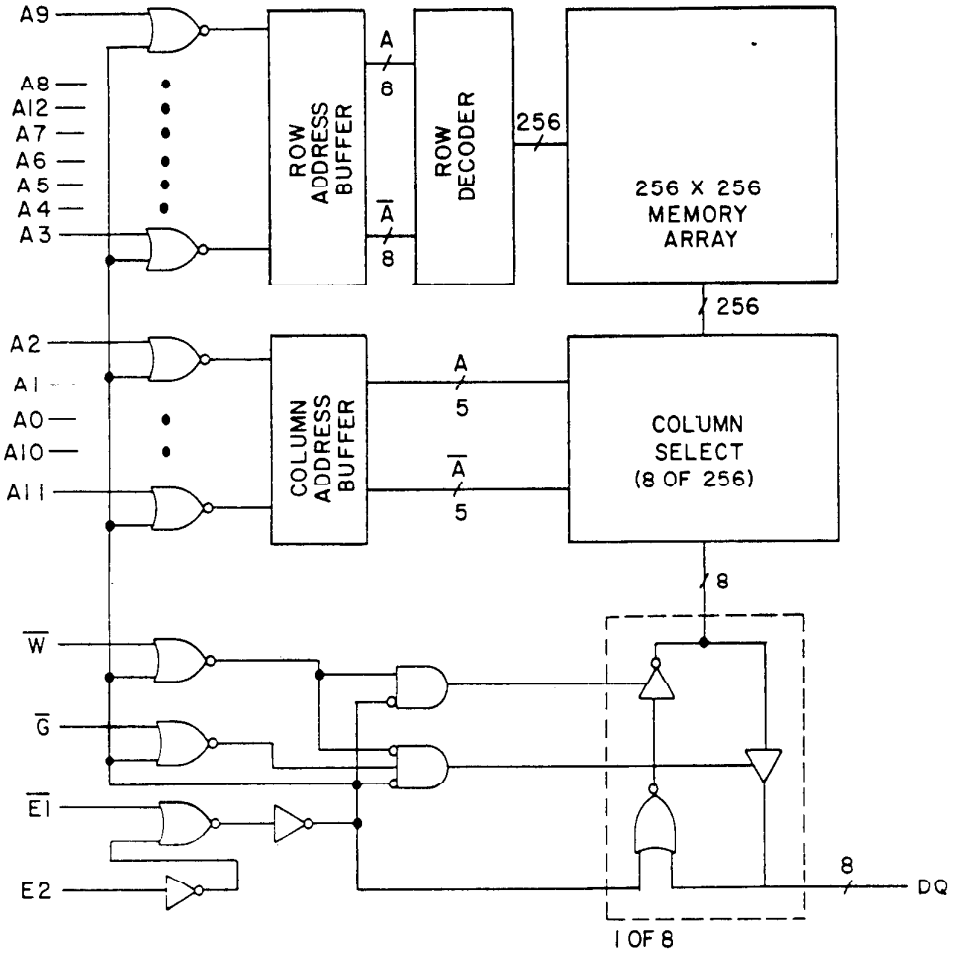


FIGURE 3. Block diagram - Continued.

Device type 06

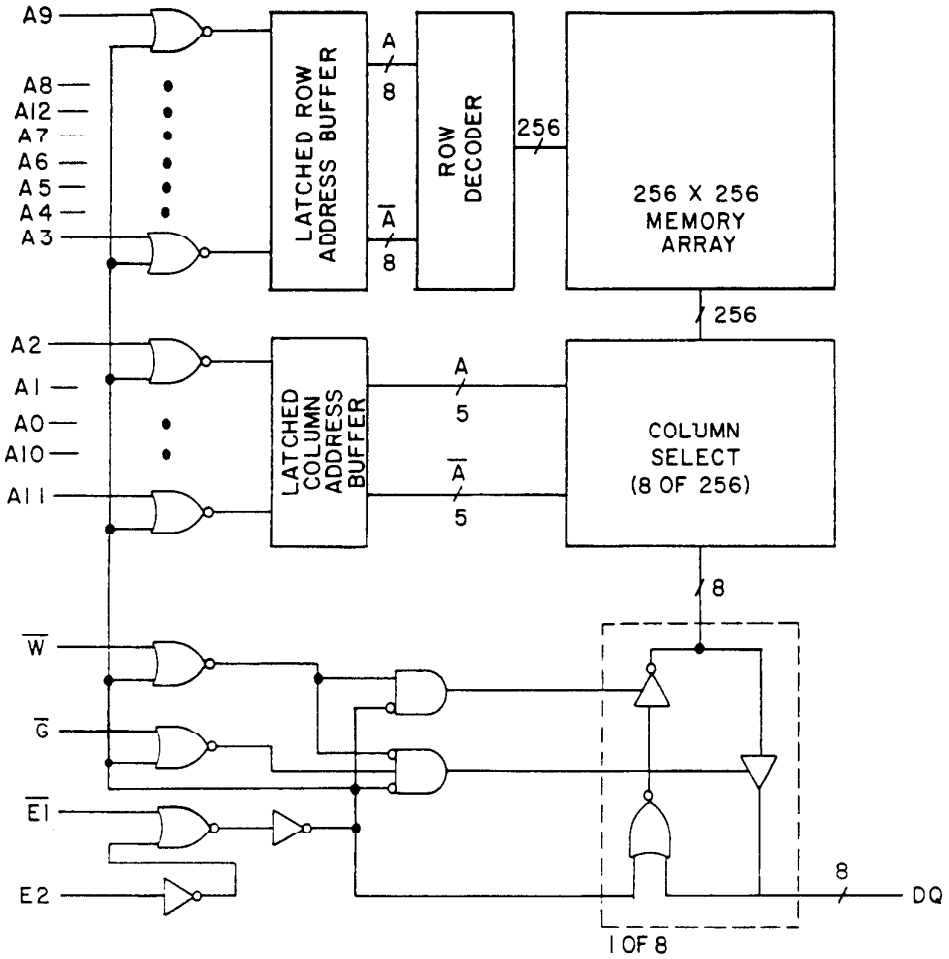


FIGURE 3. Block diagram - Continued.

Mode	$\overline{E1}$	$\overline{W}$	Output	Power	E2 (05, 06)	$\overline{G}$ (05, 06)
Not selected	High	Don't care	High Z	Standby	Low	Don't care
Write	Low	Low	High Z	Active	High	Don't care
Read	Low	High	D_{out}	Active	High	Low
Data retention (see note)	VDR	Don't care	High Z	Data retention	GND	Don't care
Enabled (High Z) 05, 06	Low	High	High Z	Active	High	High

NOTE: For device types 03, 04, 05 and 06.

FIGURE 4. Truth table.

3.2.5 Schematic circuits. The schematic circuits shall be submitted to the preparing activity prior to the inclusion of a manufacturer's device in this specification and shall be submitted to the qualifying activity as a prerequisite for qualification. All qualified manufacturers' schematics shall be maintained and available upon request.

3.2.6 Functional tests. The functional tests to be used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, then alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.2.7 Die overcoat. All devices supplied under this specification shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. Polyimide and silicone coatings are allowed as an overcoat on the die for alpha particle protection only (not as a substitute for the glassivation layer) provided each lot (i.e., polyimide and silicone coated lot) shall be subjected to and pass the group D internal moisture content test. The frequency of the internal water vapor testing may not be decreased unless otherwise approved by the preparing activity. The internal moisture content for device class S and class B after completion of all screening shall not exceed 5,000 ppm at +100°C.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.5 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit, but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 41 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

   (1) Test condition D or E, using the circuits shown on figure 5, or equivalent.

   (2) T_A = +125°C minimum.

b. Interim and final electrical test parameters shall be as specified in table II (see 3.5).

c. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

d. For classes B and S devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter measurements.

TABLE I. Electrical performance characteristics (device types 01 through 04).

Test	Symbol	Conditions $-55^{\circ}C < T_C < +125^{\circ}C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Active supply current (addresses stable)	I_{CC1}	$\overline{E} = V_{IL}$, $V_{CC} = 5.5$ V TTL I/O levels	02,03		80	mA
			01,04		60	
Active supply current (addresses cycling)	I_{CC2}	$\overline{E} = V_{IL}$, 100 percent duty cycle t_{AVAV} = minimum, $V_{CC} = 5.5$ V TTL I/O levels	02,03		80	mA
			01,04		60	
Standby supply current (addresses stable)	I_{SB1}	$\overline{E} = V_{IH}$, $V_{CC} = 5.5$ V TTL I/O levels	02,03		25	mA
			01,04		15	
Standby supply current (addresses cycling)	I_{SB2}	$\overline{E} = V_{IH}$, 100 percent duty cycle t_{AVAV} = minimum, $V_{CC} = 5.5$ V TTL I/O levels	01,03		25	mA
			02,04		15	
Data retention current	I_{CCDR}	$V_{CC} = 2.0$ V, $I_O = 0$ mA $\overline{E} = V_{CC} - 0.3$ V	03,04		600	µA
Output high voltage	V_{OH}	$I_{OH} = -4$ mA, $V_{CC} = 4.5$ V	01-04	2.4		V
Output low voltage	V_{OL}	$I_{OL} = 8$ mA, $V_{CC} = 4.5$ V	01-04		0.4	V
Input leakage (all inputs)	I_{IH} I_{IL}	$V_{IN} = 0.0$ V to 5.5 V Other pins = 0 V	01-04	-5	5	µA
Output leakage	I_{OHZ} I_{OLZ}	$V_{OUT} = 0.0$ V to 5.5 V $\overline{E} = V_{IH}$	01-04	-10	10	µA
Output short-circuit current	I_{OS}	D_{OUT} = "Logical 1" Duration $\leq$ 1 s, $V_{CC} = 5.5$ V	01-04	-50	-135	mA
Input capacitance	C_{IN}	$V_{IN} = 0$ V	01-04		5	pF
Output capacitance	C_{OUT}	$V_{OUT} = 0$ V	01-04		7	pF
Read or write cycle time	t_{AVAV}	See figures 6 and 7	02	45		ns
			01,03	55		
			04	70		
Read cycle						
Address access time	t_{AVQV}	See figure 6A	02		45	ns
			01,03		55	
			04		70	

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 01 through 04) - Continued.

Test	Symbol	Conditions $-55^{\circ}C < T_C < +125^{\circ}C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Read cycle						
Output hold from address change	t_{AXQX}	See figure 6A	01-04	5		ns
Chip enable low to chip enable high	t_{ELEH}			t_{AVAV}		ns
Chip enable access time	t_{ELQV}		02		45	ns
			01,03		55	
			04		70	
Chip enable to output active	t_{ELQX}		01,02, 03,04	5		ns
Chip disable to output disable time	t_{EHQZ}		01,02	0	35	ns
			03,04	0	40	
Chip enable to power-up time	t_{ELICCH}		01-04		0	ns
Chip disable to power-down time	t_{EHICCL}		01-04	0	45	ns
Write cycle 1						
Chip enable to end of write	t_{ELWH}	See figure 7A	02	40		ns
			01,03	50		
			04	55		
Address valid to end of write	t_{AVWH}		02	40		ns
			01,03	50		
			04	55		
Address hold time after write	t_{WHAX}		01-04	5		ns
Write pulse width	t_{WLWH}		02	30		ns
			01,03	35		
			04	40		
Address valid to start of write	t_{AVWL}		01,02	10		ns
			03,04	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 01 through 04) - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 4.5\ V$ to $5.5\ V$ unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Write cycle 1						
Data valid to end of write	t_{DVWH}	See figure 7A	02	20		ns
			01,03	25		
			04	30		
Data hold time	t_{WHDX}		01-04	5		ns
Write enable to output high-Z	t_{WLQZ}		02	0	25	ns
			01,03	0	30	
			04	0	35	
Output active from end of write	t_{WHQX}		01-04	0		ns
Write cycle 2						
Address valid to enable low	t_{AVEL}	See figure 7B	01-04	5		ns
Chip enable low to enable high	t_{ELEH}		02	40		ns
			01,03	50		
			04	60		
Address hold time after enable	t_{EHAX}		01-04	5		ns
Address valid to enable high	t_{AVEH}		02	40		ns
			01,03	50		
			04	60		
Data valid to enable high	t_{DVEH}		02	20		ns
			01,03	25		
			04	30		
Data hold time	t_{EHDX}		01-04	5		ns
Data retention						
Chip disable to data retention time	t_{CDR}	See figure 8	03,04	0		ns
Recovery time	t_R		03,04	t_{AVAV}		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 05 and 06) - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Device type	Limits Min	Limits Max	Unit
High level output voltage	V_{OH}	V_{CC} = 4.5 V, I_O = -1.0 mA	05,06	2.4		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, I_O = 4.0 mA	05,06		0.4	V
High impedance output leakage current	I_{IOZ}	V_{CC} = 5.5 V, $\overline{G}$ = 2.2 V, $V_{I/O}$ = GND and V_{CC}	05,06	-1.0	1.0	µA
Input leakge current	I_I	V_{CC} = 5.5 V, V_I = GND and V_{CC}		-1.0	1.0	µA
Standby supply current (CMOS)	I_{CCSB1}	V_{CC} = 5.5 V, I_O = 0 mA, $\overline{E1}$ = V_{CC} -0.3 V or E2 = GND +0.3 V	05,06		100	µA
Standby supply current (TTL)	I_{CCSB}	V_{CC} = 5.5 V, I_O = 0 mA, $\overline{E1}$ = 2.2 V or E2 = 0.8 V	05,06		5	mA
Enable supply current	I_{CCEN}	V_{CC} = 5.5 V, I_O = 0 mA, $\overline{E1}$ = 0.8 V, E2 = 2.2 V	05,06		5	mA
Operating supply current	I_{CCOP}	V_{CC} = 5.5 V, f = 1 MHz 1/	05,06		20	mA
Data retention supply current	I_{CCDR}	V_{CC} = 2.0 V, I_O = 0 mA, $\overline{E1}$ = V_{CC} -0.3 V or E2 = GND +0.3 V	05,06		75	µA
Input capacitance	C_{IN}	V_{CC} = 4.5 V, V_{IN} = GND T_A = +25°C, f = 1 MHz, 4/ Pins not under test = GND	05,06		12	pF
		V_{CC} = 4.5 V, V_{IN} = GND T_A = +25°C, f = 1 MHz, 5/ Pins not under test = GND			10	pF
I/O capacitance	$C_{I/O}$	V_{CC} = 4.5 V, $V_{I/O}$ = GND T_A = +25°C, f = 1 MHz, 4/ Pins not under test = GND	05,06		14	pF
		V_{CC} = 4.5 V, $V_{I/O}$ = GND T_A = +25°C, f = 1 MHz, 5/ Pins not under test = GND			12	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 05 and 06) - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Read cycle						
Read/write cycle time	t_{E1LE1L} t_{E2HE2H}	See figures 6B and 6C 2/	06	205		ns
Read/write cycle time	t_{AVAX}		05	150		ns
Address access time	t_{AVQV}		05		150	ns
Output hold after an address change	t_{AXQX}		05	10		ns
Chip enable access time	t_{E1LQV} t_{E2HQV}		05,06		150	ns
Chip enable to output disable	t_{E1HQZ}		05,06		50	ns
	t_{E2LQZ}				60	
Chip enable to output active	t_{E1LQX} t_{E2HQX}		05,06	10		ns
Output enable access time	t_{GLQV}		05		70	ns
Output high to output disable	t_{GHQZ}		05,06		50	ns
Output enable to output active	t_{GLQX}		05,06	5		ns
Address hold time	t_{E1LAX} t_{E2HAX}		06	55		ns
Write cycle						
Address setup time	t_{AVWL} t_{AVE1L} t_{AVE2H}	See figures 7C and 7D 6/	05,06	0		ns
Chip enable to end of write	t_{E1LE1H} t_{E2HE2L}		05,06	90		ns
Write enable pulse width	t_{WLWH}		05,06	90		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics (device types 05 and 06) - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified	Device type	Limits Min	Limits Max	Unit
Write cycle						
Write recovery time	t_{WHAX} t_{E1HAX} t_{E2LAX}	See figures 7C and 7D 6/	05	10		ns
Output active from end of write	t_{WHQX}		05,06	5		ns
Data valid to end of write	t_{DVWH} t_{DVE1H} t_{DVE2L}		05,06	60		ns
Data hold time	t_{WHDX}		05,06	5		ns
	t_{E1HDX}			10		
	t_{E2LDX}			10		
Write enable to output in high Z	t_{WLQZ}		05,06		50	ns
Address unlatch time	t_{E1HE1L} t_{E2LE2H}		06	55		ns
Data retention						
Chip disable to data retention time	t_{CDR}	See figure 8	05,06	0		ns
Recovery time	t_R		05,06	55		ns

1/ Typical derating = 5 mA/MHz increase in I_{CCOP}.
2/ Device type 05, see figure 6B.
Device type 06, see figure 6C.
3/ These parameters are provided for information only. Each parameter is characterized at initial design and after major process or design changes affecting the parameter.
4/ 28-pin DIP.
5/ 32-pin leadless chip carrier.
6/ Device type 05, see figure 7C.
Device type 06, see figure 7D.

Device types 01, 02, 03, and 04

Burn-in inputs

F = 100 kHz square wave(V_{IH} min = 3.0 V, V_{OL} max = 0.4)

$\overline{W}$ = F
A0 = F/2
A1 = F/4
A2 = F/8
A3 = F/16
A4 = F/32
A5 = F/64
A6 = F/128
A7 = F/256
A8 = F/512
A9 = F/1024
A10 = F/2048
A11 = F/4096
A12 = F/8192
A13 = F/16384
A14 = F/32768
A15 = F/65536

D_{IN} = F/131072

$\overline{E}$ = F/262144

C1 = 0.1 uF

R1 = 480 (±5 percent) ohm
R2 = 255 (±5 percent) ohm

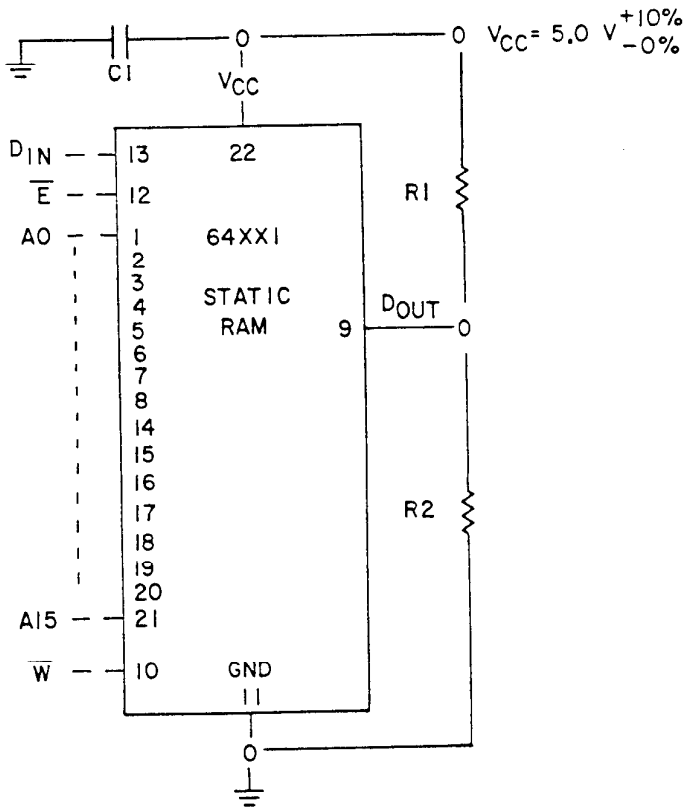
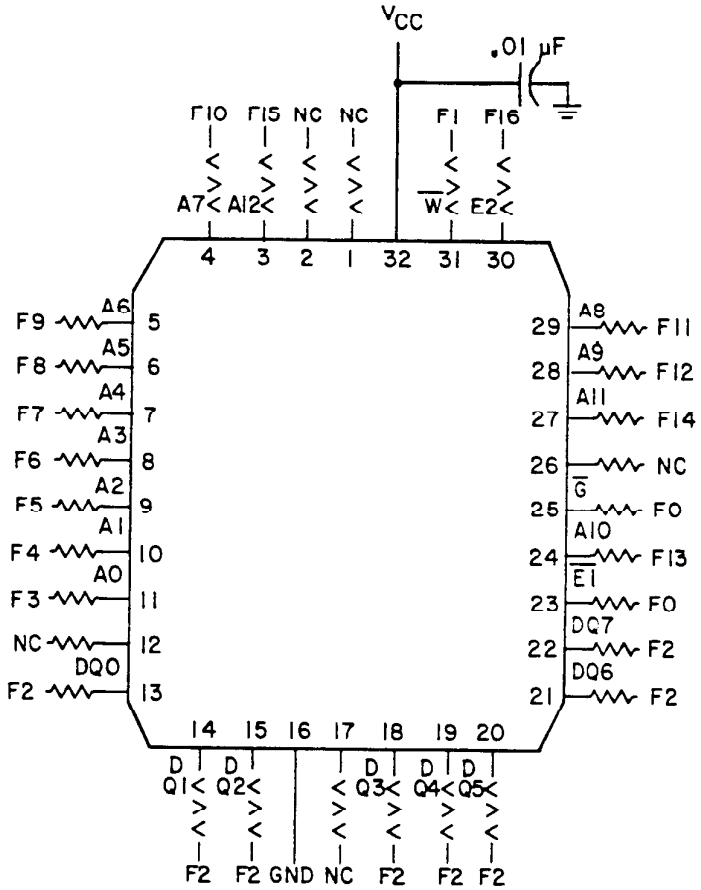


FIGURE 5. Burn-in and steady-state life test circuit.

Device types 05 and 06



F0 = 100 kHz
All Resistors 47k ohms ±10 percent
Caps = .01uF ±10 percent

Burn-in voltage
V_{CC} = 5 V min., 5.5 V max.
GND = 0 V

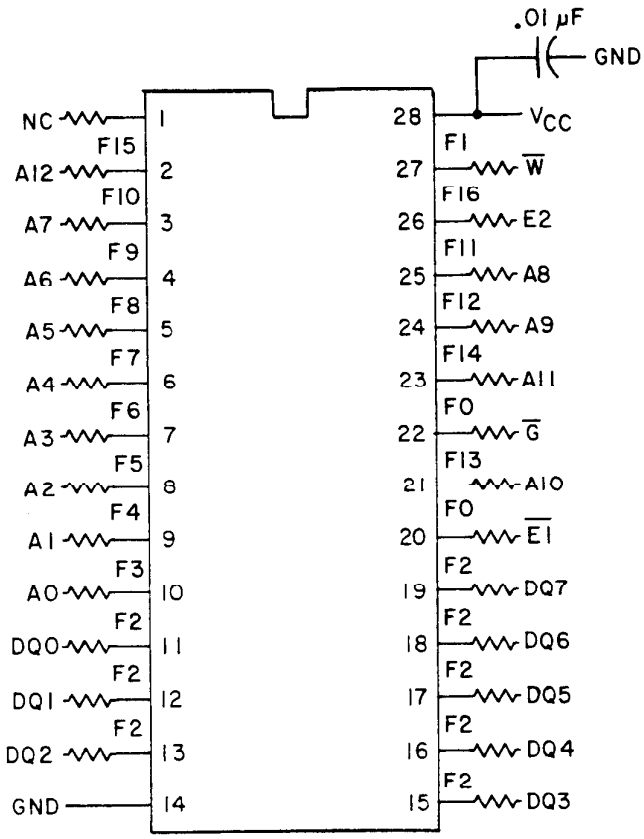
Input voltage levels
V_{IL} = 0 V
V_{IH} = 4.5 V

F1 = F0/2, F2 = F1/2, F3 = F2/2, . . . F16 = F15/2

F0 = 100 kHz	F7 = 0.78 kHz	F14 = .006 kHz
F1 = 50 kHz	F8 = 0.39 kHz	F15 = .003 kHz
F2 = 25 kHz	F9 = 0.195 kHz	F16 = .0015 kHz
F3 = 12.5 kHz	F10 = 0.0977 kHz	
F4 = 6.25 kHz	F11 = 0.048 kHz	
F5 = 3.125 kHz	F12 = 0.0244 kHz	
F6 = 1.56 kHz	F13 = 0.012 kHz	

FIGURE 5. Burn-in and steady-state life test circuit - Continued.

Device types 05 and 06



F0 = 100 kHz
All Resistors 47k ohms ±10 percent
Caps = .01uF ±10 percent

Burn-in voltage
V_{CC} = 5 V min., 5.5 V max.
GND = 0 V

Input voltage levels
V_{IL} = 0 V
V_{IH} = 4.5 V

F1 = F0/2, F2 = F1/2, F3 = F2/2, . . . F16 = F15/2

F0 = 100 kHz	F7 = 0.78 kHz	F14 = .006 kHz
F1 = 50 kHz	F8 = 0.39 kHz	F15 = .003 kHz
F2 = 25 kHz	F9 = 0.195 kHz	F16 = .0015 kHz
F3 = 12.5 kHz	F10 = 0.0977 kHz	
F4 = 6.25 kHz	F11 = 0.048 kHz	
F5 = 3.125 kHz	F12 = 0.0244 kHz	
F6 = 1.56 kHz	F13 = 0.012 kHz	

FIGURE 5. Burn-in and steady-state life test circuit - Continued.

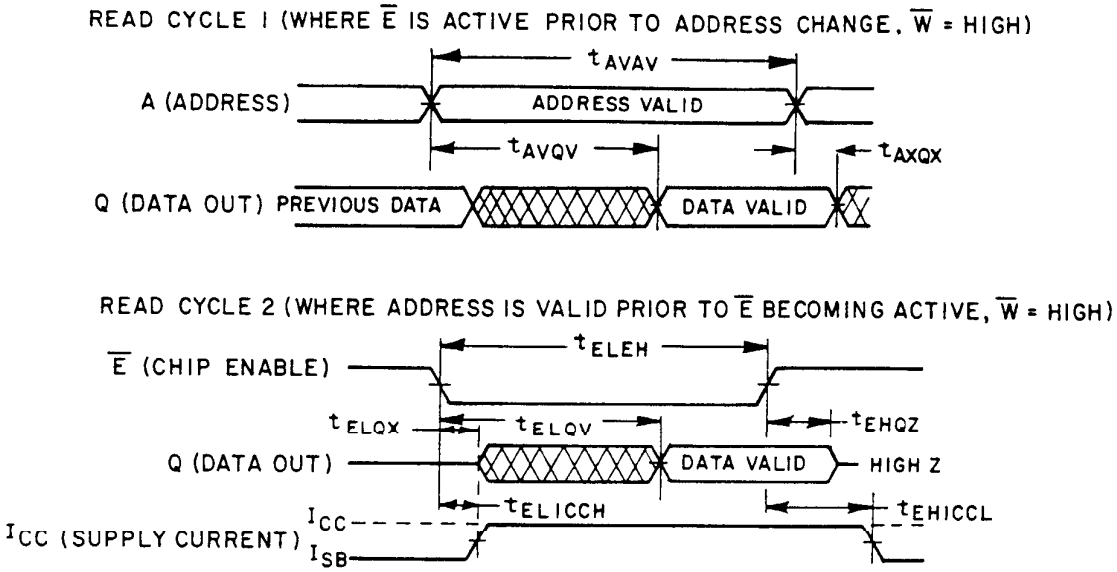


FIGURE 6A. Read cycle waveforms (device types 01-04).

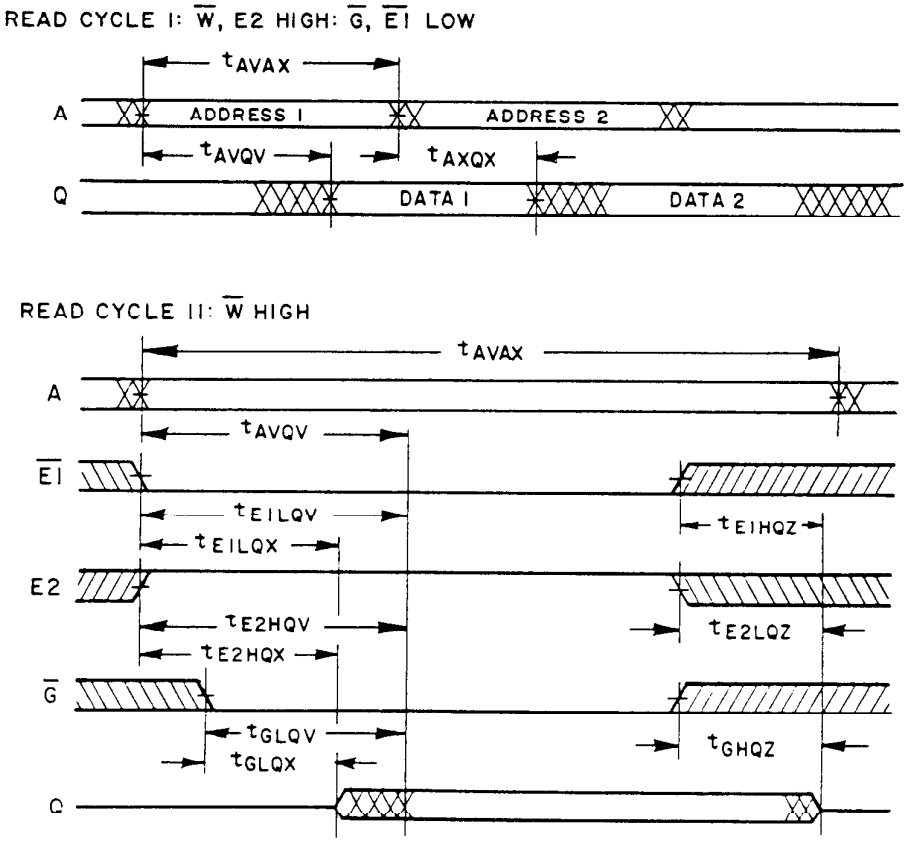


FIGURE 6B. Read cycle waveforms (device type 05).

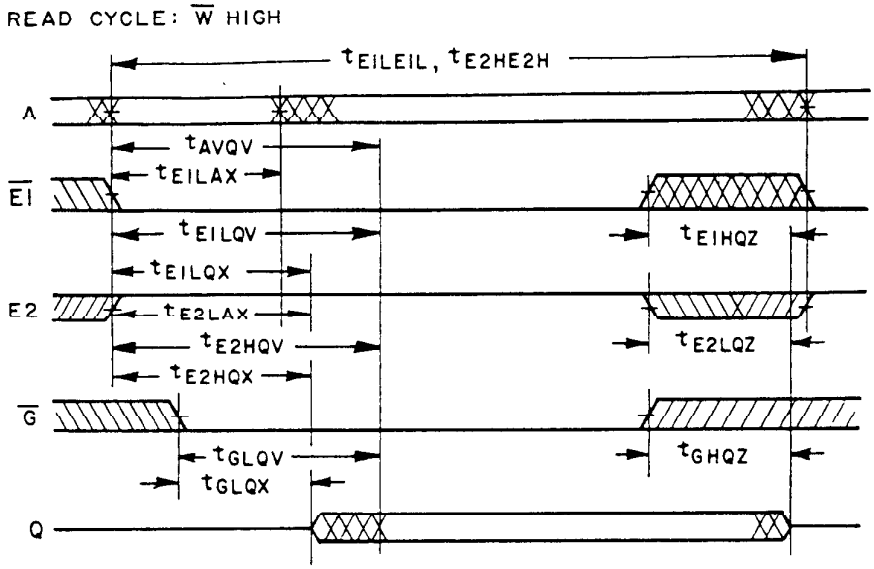


FIGURE 6C. Read cycle waveforms (device type 06).

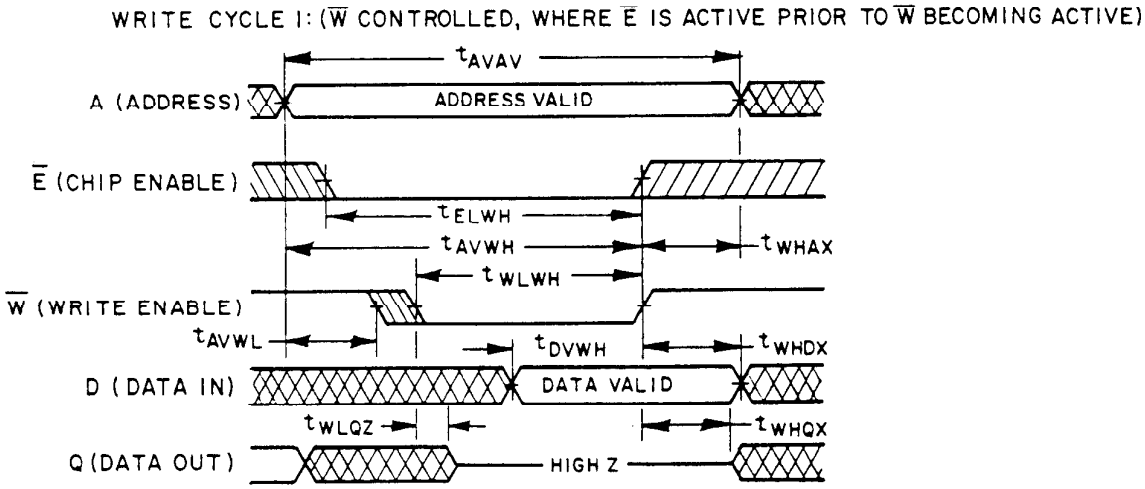


FIGURE 7A. Write cycle waveforms (device types 01-04).

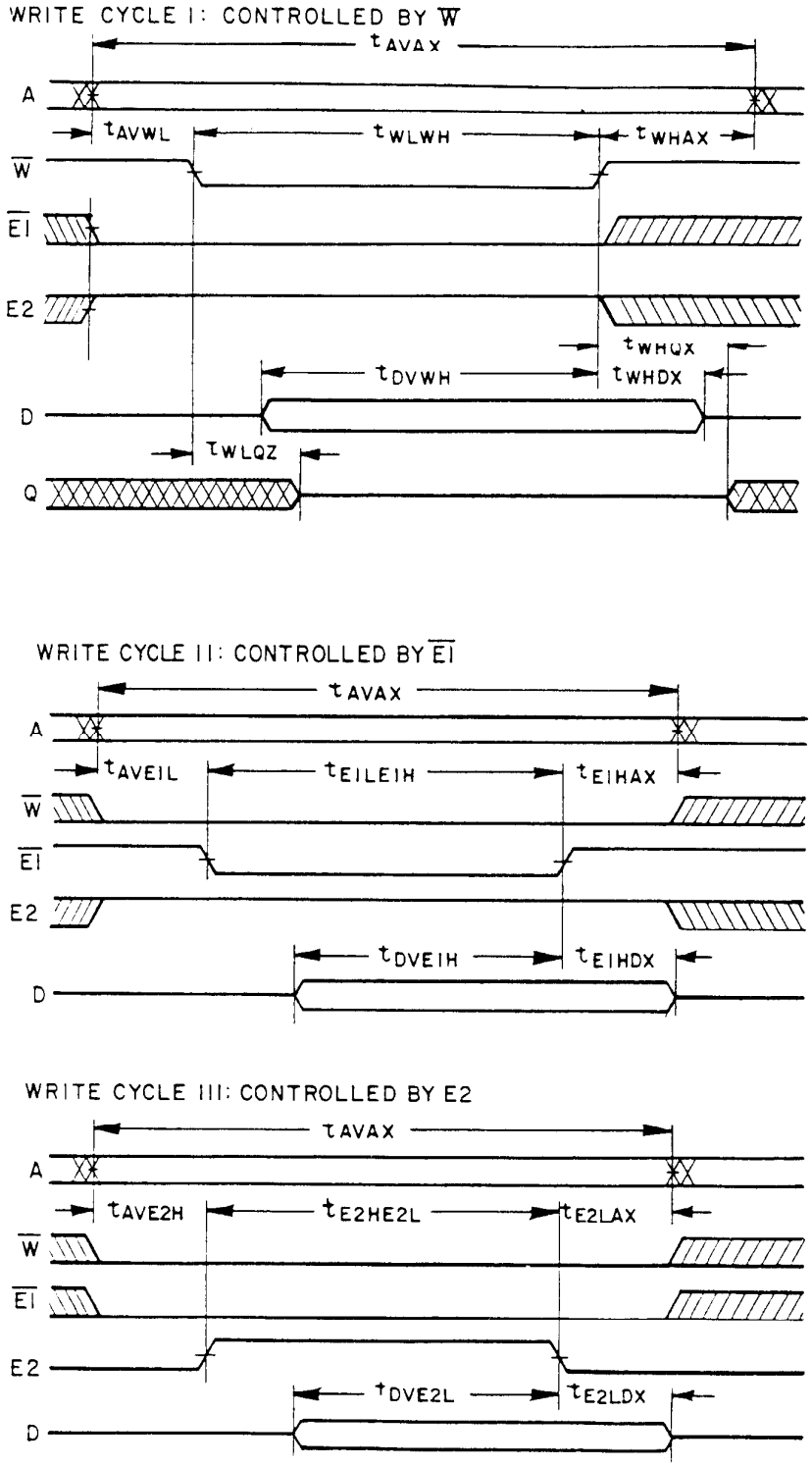
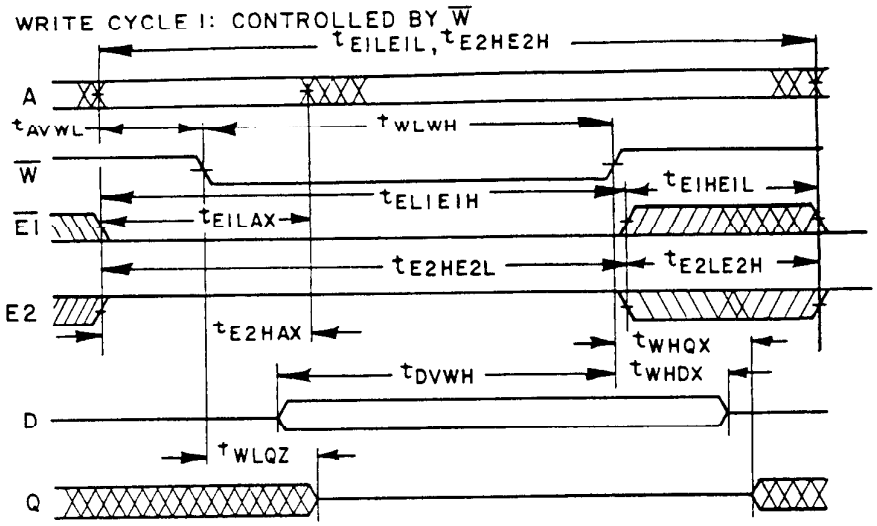
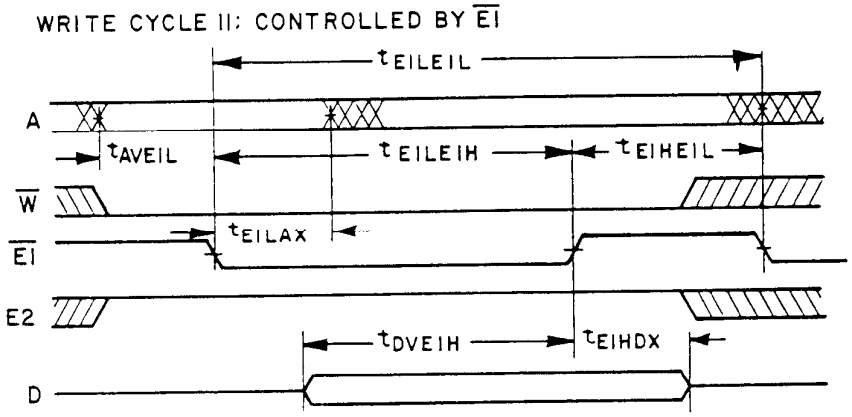


FIGURE 7C. Write cycle waveforms (device type 05).





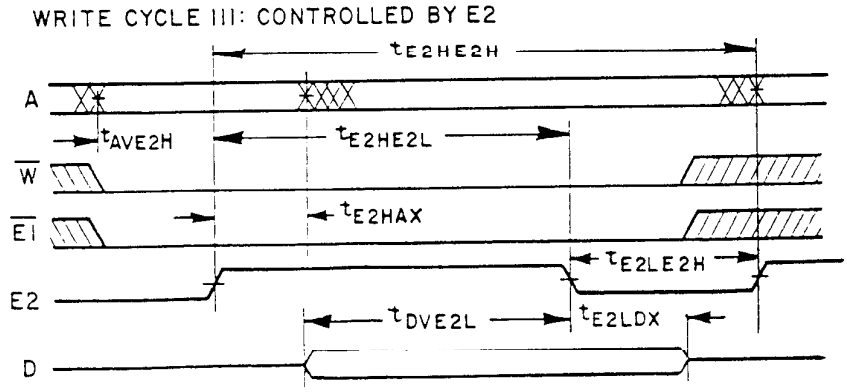


FIGURE 7D. Write cycle waveforms (device type 06).

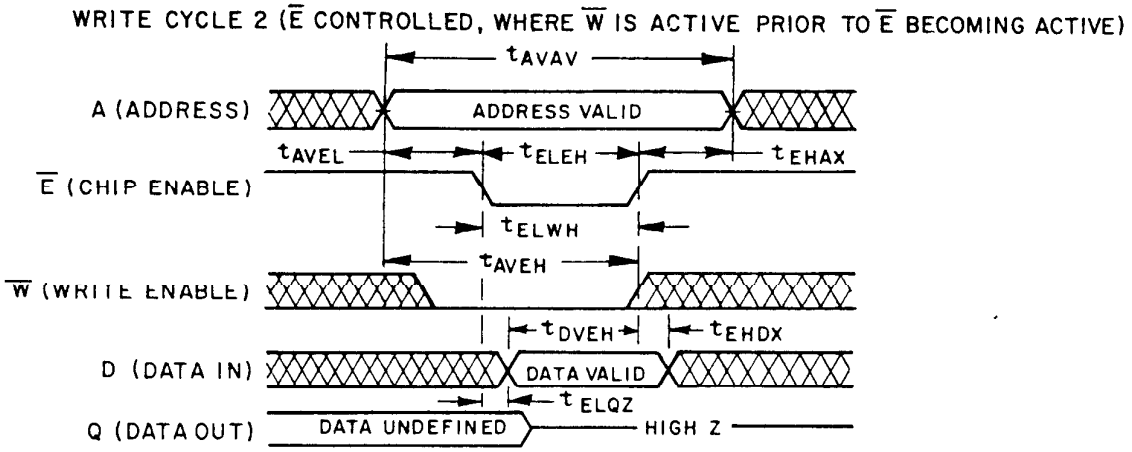


FIGURE 7B. Write cycle waveforms (device types 01-04).

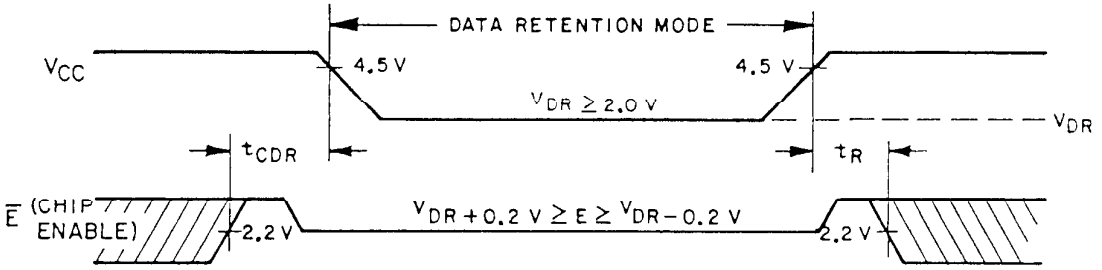


FIGURE 8. Data retention timing.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type of this specification, the slower device type may be part I qualified by conducting only group A electrical tests and submitting data in accordance with MIL-M-38510, appendix D (i.e., groups B, C, and D tests are not required).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Electrical tests shall be as specified in table II herein.

b. Subgroups 5 through 6 for class S and subgroups 5 and 6 for class B, of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 tests shall be measured only for initial qualification and after process or design changes. Capacitance shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. This test shall be performed using a fixed sample size of 25 devices and an acceptance number of zero. For device types 01, 02, 03, and 04 only: Duration of I_{OS} test shall not exceed one second. For those designs that use a die coat, a measurement of the thickness of the die coat shall be made on a sample of the qualification devices. This will then be used for the minimum limit for the measurement to be made in 4.4.4.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Electrical test requirements shall be in accordance with table II herein.

b. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015 (see 4.5.4).

c. Steady-state life test for class S devices shall be in accordance with table IIa (subgroup 5) of method 5005 of MIL-STD-883, using the circuit on figure 5 or equivalent.

d. End-point electrical test requirements shall be as specified in table II herein. Delta limits shall apply only to subgroup 5 of group B inspection and shall consist of tests specified in table IV herein.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or E, using the circuits shown on figure 5, or equivalent.

(2) T_A = +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

Continued from page 10
Continued on page 40

TABLE II. Electrical test requirements.

Line no.	MIL-STD-883 test requirements	Class S device 1/ 2/				Class B device 1/ 2/			
		Reference paragraph	Table III 3/ subgroups	Table IV 4/ delta limits	Test circuit figure	Reference paragraph	Table III 3/ subgroups	Table IV 4/ delta limits	Test circuit figure
1	Interim electrical parameters method 5004		1,2,7, 9,10				1,2,7, 9,10		
2	Static burn-in I method 1015								
3	Same as line 1								
4	Static burn-in II method 1015								
5	Same as line 1								
6	Dynamic burn-in method 1015	4.2a 4.5.2	5/		3		4.2a 4.5.2	5/	3
7	Same as line 1	4.2d	1*	Δ		4.2.d	1*	Δ	
8	Final electrical parameters method 5004		1*,2,3,4,6/ 7,8,9,10, 11				1*,2,3,7, 8,9,10,11		
9	Group A test requirements method 5005	4.4.1	1,2,3,4,6/,9, 10,11			4.4.1	1,2,3,4,6/, 7,8,9,10, 11		
10	Group B test requirements method 5005	4.4.2	1	Δ		4.4.2 4.5.3	1 7/		
11	Group C end-point electrical parameters method 5005					4.4.3	1,7,9	Δ	
12	Group D end-point electrical parameters method 5005	4.4.4	1,7,9			4.4.4	1,7,9		

1/ Blank spaces indicate tests are not applicable.
2/ For subgroups 9, 10, and 11, only the worst value measured per device need be recorded when variables data is required (e.g., during qualification).
3/ (*) indicates PDA applies to subgroup 1 (see 4.2c).
4/ (Δ) indicates delta limits shall be required, and delta values shall be computed with reference to either the initial recorded electrical parameters (see 4.5.3), or to the previous interim electrical parameters, as indicated to the qualifying activity.
5/ The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in (removal of temperature or bias) perform the final electrical parameter measurements, subgroup A1.
6/ For subgroup 4, see 4.4.1c.
7/ Indicates also applies to electrostatic discharge sensitivity tests.

TABLE III. Group A inspection for device types 01 and 02. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases I,U	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Q	W	GND	E	D	A_8
T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	2/	3/	2/	GND	0.4 V	2/	2/
	I_{CC2}		2	5/	5/	5/	5/	5/	5/	5/	5/	3/	5/	"	0.4 V	5/	5/
	I_{SB1}		3	2/	2/	2/	2/	2/	2/	2/	2/	3/	2/	"	2.2 V	2/	2/
	I_{SB2}		4	5/	5/	5/	5/	5/	5/	5/	5/	3/	5/	"	2.2 V	5/	5/
	I_{IL}	3009	5	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		5.5 V	"	5.5 V	5.5 V	5.5 V
			6	5.5 V	GND	5.5 V	"	"	"	"	"		"	"	"	"	"
			7	"	5.5 V	GND	"	"	"	"	"		"	"	"	"	"
			8	"	"	5.5 V	GND	"	"	"	"		"	"	"	"	"
			9	"	"	"	5.5 V	GND	"	"	"		"	"	"	"	"
			10	"	"	"	"	5.5 V	GND	"	"		"	"	"	"	"
			11	"	"	"	"	"	5.5 V	GND	"		"	"	"	"	"
			12	"	"	"	"	"	"	5.5 V	GND		"	"	"	"	"
			13	"	"	"	"	"	"	"	5.5 V		GND	"	"	"	"
			14	"	"	"	"	"	"	"	"		5.5 V	"	GND	"	"
			15	"	"	"	"	"	"	"	"		"	"	5.5 V	GND	"
			16	"	"	"	"	"	"	"	"		"	"	"	5.5 V	GND
			17	"	"	"	"	"	"	"	"		"	"	"	"	5.5 V
			18	"	"	"	"	"	"	"	"		"	"	"	"	"
			19	"	"	"	"	"	"	"	"		"	"	"	"	"
			20	"	"	"	"	"	"	"	"		"	"	"	"	"
			21	"	"	"	"	"	"	"	"		"	"	"	"	"
			22	"	"	"	"	"	"	"	"		"	"	"	"	"
			23	"	"	"	"	"	"	"	"		"	"	"	"	"
	I_{IH}	3010	24	5.5 V	GND	GND	GND	GND	GND	GND	GND		GND	"	GND	GND	GND
			25	GND	5.5 V	GND	"	"	"	"	"		"	"	"	"	"
			26	"	GND	5.5 V	"	"	"	"	"		"	"	"	"	"
			27	"	"	GND	5.5 V	"	"	"	"		"	"	"	"	"
			28	"	"	"	GND	5.5 V	"	"	"		"	"	"	"	"
			29	"	"	"	"	GND	5.5 V	"	"		"	"	"	"	"
			30	"	"	"	"	"	GND	5.5 V	"		"	"	"	"	"
			31	"	"	"	"	"	"	GND	5.5 V		"	"	"	"	"
			32	"	"	"	"	"	"	"	GND		"	"	"	"	"
			33	"	"	"	"	"	"	"	"		5.5 V	"	"	"	"
			34	"	"	"	"	"	"	"	"		GND	"	5.5 V	"	"
			35	"	"	"	"	"	"	"	"		"	"	GND	5.5 V	"
			36	"	"	"	"	"	"	"	"		"	"	"	GND	5.5 V
			37	"	"	"	"	"	"	"	"		"	"	"	"	GND
			38	"	"	"	"	"	"	"	"		"	"	"	"	"
			39	"	"	"	"	"	"	"	"		"	"	"	"	"
			40	"	"	"	"	"	"	"	"		"	"	"	"	"
			41	"	"	"	"	"	"	"	"		"	"	"	"	"
			42	"	"	"	"	"	"	"	"		"	"	"	"	"
	I_{OL2}	3020	43									GND		"	2.2 V		
	I_{OH2}	3021	44									5.5 V		"	2.2 V		
	V_{OL}	3007	45	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	"	6/	6/	6/
	V_{OH}	3006	46	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	"	7/	7/	7/
2	Same tests as for subgroup 1, except T_C = +125°C																
3	Same tests as for subgroup 1, except T_C = -55°C																

See footnotes at end of device types 01 and 02.

TABLE III. Group A inspection for device types 01 and 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases T,U	15	16	17	18	19	20	21	22	Algorithm (see appendix)	Measured terminal	Test limits		Unit
			Test no.	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	V_{CC}			Min	Max	
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	5.5 V		V_{WC}		4/	mA
	I_{CC2}		2	5/	5/	5/	5/	5/	5/	5/	"				"	"
	I_{SB1}		3	2/	2/	2/	2/	2/	2/	2/	"		"		"	"
	I_{SB2}		4	5/	5/	5/	5/	5/	5/	5/	"		"		"	"
	I_{IL}	3009	5	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"		A_0	-5	5	μA
			6	"	"	"	"	"	"	"	"		A_1	"	"	"
			7	"	"	"	"	"	"	"	"		A_2	"	"	"
			8	"	"	"	"	"	"	"	"		A_3	"	"	"
			9	"	"	"	"	"	"	"	"		A_4	"	"	"
			10	"	"	"	"	"	"	"	"		A_5	"	"	"
			11	"	"	"	"	"	"	"	"		A_6	"	"	"
			12	"	"	"	"	"	"	"	"		A_7	"	"	"
			13	"	"	"	"	"	"	"	"		$\overline{W}$	"	"	"
			14	"	"	"	"	"	"	"	"		$\overline{E}$	"	"	"
			15	"	"	"	"	"	"	"	"		D	"	"	"
			16	"	"	"	"	"	"	"	"		A_8	"	"	"
			17	GND	"	"	"	"	"	"	"		A_9	"	"	"
			18	5.5 V	GND	"	"	"	"	"	"		A_{10}	"	"	"
			19	"	5.5 V	GND	"	"	"	"	"		A_{11}	"	"	"
			20	"	"	5.5 V	GND	"	"	"	"		A_{12}	"	"	"
			21	"	"	"	5.5 V	GND	"	"	"		A_{13}	"	"	"
			22	"	"	"	"	5.5 V	GND	"	"		A_{14}	"	"	"
			23	"	"	"	"	"	5.5 V	GND	"		A_{15}	"	"	"
	I_{IH}	3010	24	GND	GND	GND	GND	GND	GND	"	"		A_0	"	"	"
			25	"	"	"	"	"	"	"	"		A_1	"	"	"
			26	"	"	"	"	"	"	"	"		A_2	"	"	"
			27	"	"	"	"	"	"	"	"		A_3	"	"	"
			28	"	"	"	"	"	"	"	"		A_4	"	"	"
			29	"	"	"	"	"	"	"	"		A_5	"	"	"
			30	"	"	"	"	"	"	"	"		A_6	"	"	"
			31	"	"	"	"	"	"	"	"		A_7	"	"	"
			32	"	"	"	"	"	"	"	"		$\overline{W}$	"	"	"
			33	"	"	"	"	"	"	"	"		$\overline{E}$	"	"	"
			34	"	"	"	"	"	"	"	"		D	"	"	"
			35	"	"	"	"	"	"	"	"		A_8	"	"	"
			36	5.5 V	"	"	"	"	"	"	"		A_9	"	"	"
			37	GND	5.5 V	"	"	"	"	"	"		A_{10}	"	"	"
			38	"	GND	5.5 V	"	"	"	"	"		A_{11}	"	"	"
			39	"	"	GND	5.5 V	"	"	"	"		A_{12}	"	"	"
			40	"	"	"	GND	5.5 V	"	"	"		A_{13}	"	"	"
			41	"	"	"	"	GND	5.5 V	"	"		A_{14}	"	"	"
			42	"	"	"	"	"	GND	5.5 V	"		A_{15}	"	"	"
	I_{OLZ}	3020	43								"		Q	-10	10	"
	I_{OHZ}	3021	44								"		"	-10	10	"
	V_{OL}	3007	45	6/	6/	6/	6/	6/	6/	6/	4.5 V		"		0.4	V
	V_{OH}	3006	46	7/	7/	7/	7/	7/	7/	7/	4.5 V		"	2.4		V
2																
3																

See footnotes at end of device types 01 and 02.

TABLE III. Group A inspection for device types 01 and 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases T,U	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Q	$\overline{W}$	GND	$\overline{E}$	D	A_8
4 T_C = +25°C	C_{IN}	3012	47	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	GND	8/	8/	8/
	C_{OUT}	3012	48	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	8/	8/	8/
	I_{OS}	3011	49	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	"	9/	9/	9/
7 T_C = +25°C	I/O	Functional test	50	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	"	10/	10/	10/
8 T_C = -55°C and T_C = +125°C	Same tests as for subgroup 7, except at both T_C = -55°C and +125°C.																
9 T_C = +25°C	Table I ac parameter		51	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	13/	11/ 12/	GND	11/ 12/	11/ 12/	11/ 12/
			52	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			53	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			54	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			55	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			56	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			57	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	"	12/ 14/	"	12/ 14/	12/ 14/	12/ 14/
			58	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	"	12/ 15/	"	12/ 15/	12/ 15/	12/ 15/
			59	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	"	12/ 16/	"	12/ 16/	12/ 16/	12/ 16/
			60	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	"	12/ 14/	"	12/ 14/	12/ 14/	12/ 14/
			61	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	"	12/ 15/	"	12/ 15/	12/ 15/	12/ 15/
			62	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	"	12/ 16/	"	12/ 16/	12/ 16/	12/ 16/
10	Same tests as for subgroup 9, except T_C = +125°C																
11	Same tests as for subgroup 9, except T_C = -55°C																

1/ Pins not designated may be high ≥ 2.4 V, low ≤ 0.8 V, or open.
2/ Test is done with addresses held stable and all inputs held at V_{IL} = 0.4 V and V_{IH} = 2.2 V.
3/ Outputs open.
4/ Use limits listed in table I.
5/ All input levels and timing edges are set to table I limits with read cycle timing; V_{IL} = 0.4 V and V_{IH} = 2.2 V.
6/ An input preconditioning logic sequence shall be applied that results in a logical "0" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, V_{IH} = 2.2 V, and I_{OL} = 8 mA.
7/ An input preconditioning logic sequence shall be applied that results in a logical "1" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, V_{IH} = 2.2 V, and I_{OL} = -4 mA.
8/ See 4.4.1c.
9/ Data out = "logic high"; test duration 1 second maximum.
10/ Using the specified algorithm, an ac functional test is performed using V_{IL} = 0.8 V and V_{IH} = 2.2 V.
11/ Input levels are V_{IL} = 0 V and V_{IH} = 3.0 V.
12/ Multiple timing sets shall be used so as to test all timing parameters indicated on figures 6A, 7A, and 7B to the minimum and maximum limits specified in table I.
13/ Output loaded with load specified on figure 9. Output reference level = 1.5 V for all tests except t_{EHQZ} and t_{WLQZ} where transition is measured at ±0.5 V departure from the steady-state voltage.
14/ Input levels are V_{IL} = -1.0 V and V_{IH} = 6.0 V.
15/ Input levels are V_{IL} = -1.0 V and V_{IH} = 3.0 V.
16/ Input levels are V_{IL} = 0 V and V_{IH} = 6.0 V.

TABLE III. Group A inspection for device types 01 and 02 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases T,U Test no.	15 A_9	16 A_{10}	17 A_{11}	18 A_{12}	19 A_{13}	20 A_{14}	21 A_{15}	22 V_{CC}	Algorithm (see appendix)	Measured terminal	Test limits Min	Test limits Max	Unit
4 T_C = +25°C	C_{IN}	3012	47	8/	8/	8/	8/	8/	8/	8/			Each input		5	pF
	C_{OUT}	3012	48	8/	8/	8/	8/	8/	8/	8/			Each output		7	pF
	I_{OS}	3011	49	9/	9/	9/	9/	9/	9/	9/	5.5 V		Q	-50	-135	mA
7 T_C = +25°C	I/O	Functional test	50	10/	10/	10/	10/	10/	10/	10/	4.5 V	Pattern 3	Q	4/	4/	
8 T_C = -55°C and T_C = +125°C																
9 T_C = +25°C	Table I ac parameter		51	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	11/ 12/	4.5 V	Pattern 1	Q	4/	4/	
			52	"	"	"	"	"	"	"	"	Pattern 2	"	"	"	
			53	"	"	"	"	"	"	"	"	Pattern 3	"	"	"	
			54	"	"	"	"	"	"	"	"	Pattern 1	"	"	"	
			55	"	"	"	"	"	"	"	"	Pattern 2	"	"	"	
			56	"	"	"	"	"	"	"	"	Pattern 3	"	"	"	
			57	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	"	Pattern 1	"	"	"	
			58	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	"	"	"	"	"	
			59	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	"	"	"	"	"	
			60	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	12/ 14/	"	"	"	"	"	
			61	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	12/ 15/	"	"	"	"	"	
			62	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	12/ 16/	"	"	"	"	"	
10																
11																

TABLE III. Group A inspection for device types 03 and 04. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases T,U	1	2	3	4	5	6	7	8	9	10	11	12	13	14
			Test no.	A_0	A_1	A_2	A_3	A_4	A_5	A_6	A_7	Q	$\overline{W}$	GND	$\overline{E}$	D	A_8
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	2/	3/	2/	GND	0.4 V	2/	2/
	I_{CC2}		2	5/	5/	5/	5/	5/	5/	5/	5/	3/	5/	"	0.4 V	5/	5/
	I_{SB1}		3	2/	2/	2/	2/	2/	2/	2/	2/	3/	2/	"	2.2 V	2/	2/
	I_{SB2}		4	5/	5/	5/	5/	5/	5/	5/	5/	3/	5/	"	2.2 V	5/	5/
	I_{IL}	3009	5	GND	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V		5.5 V	"	5.5 V	5.5 V	5.5 V
			6	5.5 V	GND	5.5 V	"	"	"	"	"		"	"	"	"	"
			7	"	5.5 V	GND	"	"	"	"	"		"	"	"	"	"
			8	"	"	5.5 V	GND	"	"	"	"		"	"	"	"	"
			9	"	"	"	5.5 V	GND	"	"	"		"	"	"	"	"
			10	"	"	"	"	5.5 V	GND	"	"		"	"	"	"	"
			11	"	"	"	"	"	5.5 V	GND	"		"	"	"	"	"
			12	"	"	"	"	"	"	5.5 V	GND		"	"	"	"	"
			13	"	"	"	"	"	"	"	5.5 V		GND	"	"	"	"
			14	"	"	"	"	"	"	"	"		5.5 V	"	GND	"	"
			15	"	"	"	"	"	"	"	"		"	"	5.5 V	GND	"
			16	"	"	"	"	"	"	"	"		"	"	"	5.5 V	GND
			17	"	"	"	"	"	"	"	"		"	"	"	"	5.5 V
			18	"	"	"	"	"	"	"	"		"	"	"	"	"
			19	"	"	"	"	"	"	"	"		"	"	"	"	"
			20	"	"	"	"	"	"	"	"		"	"	"	"	"
			21	"	"	"	"	"	"	"	"		"	"	"	"	"
			22	"	"	"	"	"	"	"	"		"	"	"	"	"
			23	"	"	"	"	"	"	"	"		"	"	"	"	"
	I_{IH}	3010	24	5.5 V	GND	GND	GND	GND	GND	GND	GND		GND	"	GND	GND	GND
			25	GND	5.5 V	GND	"	"	"	"	"		"	"	"	"	"
			26	"	GND	5.5 V	"	"	"	"	"		"	"	"	"	"
			27	"	"	GND	5.5 V	"	"	"	"		"	"	"	"	"
			28	"	"	"	GND	5.5 V	"	"	"		"	"	"	"	"
			29	"	"	"	"	GND	5.5 V	"	"		"	"	"	"	"
			30	"	"	"	"	"	GND	5.5 V	"		"	"	"	"	"
			31	"	"	"	"	"	"	GND	5.5 V		"	"	"	"	"
			32	"	"	"	"	"	"	"	GND		5.5 V	"	"	"	"
			33	"	"	"	"	"	"	"	"		GND	"	5.5 V	"	"
			34	"	"	"	"	"	"	"	"		"	"	GND	5.5 V	"
			35	"	"	"	"	"	"	"	"		"	"	"	GND	5.5 V
			36	"	"	"	"	"	"	"	"		"	"	"	"	GND
			37	"	"	"	"	"	"	"	"		"	"	"	"	"
			38	"	"	"	"	"	"	"	"		"	"	"	"	"
			39	"	"	"	"	"	"	"	"		"	"	"	"	"
			40	"	"	"	"	"	"	"	"		"	"	"	"	"
			41	"	"	"	"	"	"	"	"		"	"	"	"	"
			42	"	"	"	"	"	"	"	"		"	"	"	"	"
	I_{OLZ}	3020	43									GND		"	2.2 V		
	I_{OHZ}	3021	44									5.5 V		"	2.2 V		
	V_{OL}	3007	45	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	"	6/	6/	6/
	V_{OH}	3006	46	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	"	7/	7/	7/
2	Same tests as for subgroup 1, except T_C = +125°C																
3	Same tests as for subgroup 1, except T_C = -55°C																

See footnotes at end of device types 03 and 04.

TABLE III. Group A inspection for device types 03 and 04 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases T,U Test no.	15 A_9	16 A_{10}	17 A_{11}	18 A_{12}	19 A_{13}	20 A_{14}	21 A_{15}	22 V_{CC}	Algorithm (see appendix)	Measured terminal	Test limits Min	Test limits Max	Unit
1 T_C = +25°C	I_{CC1}	3005	1	2/	2/	2/	2/	2/	2/	2/	5.5 V		V_{CC}		4/	mA
	I_{CC2}		2	5/	5/	5/	5/	5/	5/	5/	"		"		"	"
	I_{SB1}		3	2/	2/	2/	2/	2/	2/	2/	"		"		"	"
	I_{SB2}		4	5/	5/	5/	5/	5/	5/	5/	"		"		"	"
	I_{IL}	3009	5	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	"		A_0	-5	5	µA
			6	"	"	"	"	"	"	"	"		A_1	"	"	"
			7	"	"	"	"	"	"	"	"		A_2	"	"	"
			8	"	"	"	"	"	"	"	"		A_3	"	"	"
			9	"	"	"	"	"	"	"	"		A_4	"	"	"
			10	"	"	"	"	"	"	"	"		A_5	"	"	"
			11	"	"	"	"	"	"	"	"		A_6	"	"	"
			12	"	"	"	"	"	"	"	"		A_7	"	"	"
			13	"	"	"	"	"	"	"	"		$\overline{W}$	"	"	"
			14	"	"	"	"	"	"	"	"		$\overline{E}$	"	"	"
			15	"	"	"	"	"	"	"	"		D	"	"	"
			16	"	"	"	"	"	"	"	"		A_8	"	"	"
			17	GND	"	"	"	"	"	"	"		A_9	"	"	"
			18	5.5 V	GND	"	"	"	"	"	"		A_{10}	"	"	"
			19	"	5.5 V	GND	"	"	"	"	"		A_{11}	"	"	"
			20	"	"	5.5 V	GND	"	"	"	"		A_{12}	"	"	"
			21	"	"	"	5.5 V	GND	"	"	"		A_{13}	"	"	"
			22	"	"	"	"	5.5 V	GND	"	"		A_{14}	"	"	"
			23	"	"	"	"	"	5.5 V	GND	"		A_{15}	"	"	"
	I_{IH}	3010	24	GND	GND	GND	GND	GND	GND	GND	"		A_0	"	"	"
			25	"	"	"	"	"	"	"	"		A_1	"	"	"
			26	"	"	"	"	"	"	"	"		A_2	"	"	"
			27	"	"	"	"	"	"	"	"		A_3	"	"	"
			28	"	"	"	"	"	"	"	"		A_4	"	"	"
			29	"	"	"	"	"	"	"	"		A_5	"	"	"
			30	"	"	"	"	"	"	"	"		A_6	"	"	"
			31	"	"	"	"	"	"	"	"		A_7	"	"	"
			32	"	"	"	"	"	"	"	"		$\overline{W}$	"	"	"
			33	"	"	"	"	"	"	"	"		$\overline{E}$	"	"	"
			34	"	"	"	"	"	"	"	"		D	"	"	"
			35	"	"	"	"	"	"	"	"		A_8	"	"	"
			36	5.5 V	"	"	"	"	"	"	"		A_9	"	"	"
			37	GND	5.5 V	"	"	"	"	"	"		A_{10}	"	"	"
			38	"	GND	5.5 V	"	"	"	"	"		A_{11}	"	"	"
			39	"	"	GND	5.5 V	"	"	"	"		A_{12}	"	"	"
			40	"	"	"	GND	5.5 V	"	"	"		A_{13}	"	"	"
			41	"	"	"	"	GND	5.5 V	"	"		A_{14}	"	"	"
			42	"	"	"	"	"	GND	5.5 V	"		A_{15}	"	"	"
	I_{OLZ}	3020	43								"		Q	-10	10	"
	I_{OHZ}	3021	44								"		"	-10	10	"
	V_{OL}	3007	45	6/	6/	6/	6/	6/	6/	6/	4.5 V		"		0.4	V
	V_{OH}	3006	46	7/	7/	7/	7/	7/	7/	7/	4.5 V		"	2.4		V
2																
3																

See footnotes at end of device types 03 and 04.

TABLE III. Group A inspection for device types 03 and 04 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Cases 1,2 Test no.	1 A_0	2 A_1	3 A_2	4 A_3	5 A_4	6 A_5	7 A_6	8 A_7	9 Q	10 W	11 GND	12 E	13 D	14 A_8
4 T_C = +25°C	C_{IN}	3012	47	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	GND	8/	8/	8/
	C_{OUT}	3012	48	8/	8/	8/	8/	8/	8/	8/	8/	8/	8/	"	8/	8/	8/
	I_{OS}	3011	49	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	"	9/	9/	9/
7 T_C = +25°C	V_{DR}	Functional test	50	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	"	10/	10/	10/
	I/O		51	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	"	11/	11/	11/
8 T_C = -55°C and T_C = +125°C	Same tests as for subgroup 7, except at both T_C = -55°C and +125°C.																
9 T_C = +25°C	Table I ac parameter		52	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	14/	12/ 13/	GND	12/ 13/	12/ 13/	12/ 13/
			53	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			54	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			55	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			56	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			57	"	"	"	"	"	"	"	"	"	"	"	"	"	"
			58	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	"	13/ 15/	"	13/ 15/	13/ 15/	13/ 15/
			59	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	"	13/ 16/	"	13/ 16/	13/ 16/	13/ 16/
			60	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	"	13/ 17/	"	13/ 17/	13/ 17/	13/ 17/
			61	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	"	13/ 15/	"	13/ 15/	13/ 15/	13/ 15/
			62	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	"	13/ 16/	"	13/ 16/	13/ 16/	13/ 16/
			63	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	"	13/ 17/	"	13/ 17/	13/ 17/	13/ 17/
10	Same tests as for subgroup 9, except T_C = +125°C																
11	Same tests as for subgroup 9, except T_C = -55°C																

1/ Pins not designated may be high > 2.4 V, low < 0.8 V, or open.
2/ Test is done with addresses held stable and all inputs held at V_{IL} = 0.4 V and V_{IH} = 2.2 V.
3/ Outputs open.
4/ Use limits listed in table I.
5/ All input levels and timing edges are set to table I limits with read cycle timing; V_{IL} = 0.4 V and V_{IH} = 2.2 V.
6/ An input preconditioning logic sequence shall be applied that results in a logical "0" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, V_{IH} = 2.2 V, and I_{OL} = 8 mA.
7/ An input preconditioning logic sequence shall be applied that results in a logical "1" at the output to be measured. Logic input levels and forcing current during measurement shall be: V_{IL} = 0.8 V, V_{IH} = 2.2 V, and I_{OL} = -4 mA.
8/ See 4.4.1c.
9/ Data out = "logic high"; test duration 1 second maximum.
10/ Data retention voltage (V_{DR}) is guaranteed by testing using a 200 ms pause at the test voltage with a data pattern and then repeating with the complemented data pattern.
11/ Using the specified algorithm, an ac functional test is performed using V_{IL} = 0.8 V and V_{IH} = 2.2 V.
12/ Input levels are V_{IL} = 0 V and V_{IH} = 3.0 V.
13/ Multiple timing sets shall be used so as to test all timing parameters indicated on figures 6A, 7A, and 7B to the minimum and maximum limits specified in table I.
14/ Output loaded with load specified on figure 9. Output reference level = 1.5 V for all tests except t_{EHQZ} and t_{WLQZ} where transition is measured at ±0.5 V departure from the steady-state voltage.
15/ Input levels are V_{IL} = -1.0 V and V_{IH} = 3.0 V.
16/ Input levels are V_{IL} = -1.0 V and V_{IH} = 3.0 V.
17/ Input levels are V_{IL} = 0 V and V_{IH} = 6.0 V.

TABLE III. Group A inspection for device types 03 and 04 - Continued. 1/

Subgroup	Symbol	Mil-STD-883 method	Cases I, J	15	16	17	18	19	20	21	22	Algorithm (see appendix)	Measured terminal	Test limits Min	Test limits Max	Unit
			Test no.	A_9	A_{10}	A_{11}	A_{12}	A_{13}	A_{14}	A_{15}	V_{CC}					
4 T_C = +25°C	C_{IN}	3012	47	8/	8/	8/	8/	8/	8/	8/			Each input		5	pF
	C_{OUT}	3012	48	8/	8/	8/	8/	8/	8/	8/			Each output		7	pF
	I_{OS}	3011	49	9/	9/	9/	9/	9/	9/	9/	5.5 V		Q	-50	-135	mA
7 T_C = +25°C	V_{DR}	Functional test	50	10/	10/	10/	10/	10/	10/	10/	2.0 V		V_{CC}			
	I/O		51	11/	11/	11/	11/	11/	11/	11/	4.5 V	Pattern 3	Q	4/	4/	
8 T_C = -55°C and T_C = +125°C																
9 T_C = +25°C	Table I ac parameter		52	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	12/ 13/	4.5 V	Pattern 1	Q	4/	4/	
			53	"	"	"	"	"	"	"	"	Pattern 2	"	"	"	
			54	"	"	"	"	"	"	"	"	Pattern 3	"	"	"	
			55	"	"	"	"	"	"	"	5.5 V	Pattern 1	"	"	"	
			56	"	"	"	"	"	"	"	"	Pattern 2	"	"	"	
			57	"	"	"	"	"	"	"	"	Pattern 3	"	"	"	
			58	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	4.5 V	Pattern 1	"	"	"	
			59	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	"	"	"	"	"	
			60	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	"	"	"	"	"	
			61	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	13/ 15/	5.5 V	"	"	"	"	
			62	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	13/ 16/	"	"	"	"	"	
			63	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	13/ 17/	"	"	"	"	"	
10																
11																

TABLE III. Group A inspection for device types 05 and 06. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
			Case Y	3	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21
			Test no.	A_{12}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	V_{SS}	Q_3	Q_4	Q_5	Q_6
1 T_C = +25°C	I_{CCSB}	3005	1	GND	GND	GND	GND	GND	GND	GND	GND	GND	3/	3/	3/	GND	3/	3/	3/	3/
	I_{CCSB}		2	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{CCEN}		3	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{CCOP}		4	2/	2/	2/	2/	2/	2/	2/	2/	2/	"	"	"	"	"	"	"	"
	I_{CCSB1}		5	GND	GND	GND	GND	GND	GND	GND	GND	GND	"	"	"	"	"	"	"	"
	I_{CCSB1}		6	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{CCDR}		7	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{CCDR}		8	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	I_{IL}	3009	9	GND	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}				"				
			10	V_{CC}	GND	V_{CC}	"	"	"	"	"	"				"				
			11		V_{CC}	GND	"	"	"	"	"	"				"				
			12	"	"	V_{CC}	GND	"	"	"	"	"				"				
			13	"	"	"	V_{CC}	GND	"	"	"	"				"				
			14	"	"	"	"	V_{CC}	GND	"	"	"				"				
			15	"	"	"	"	"	V_{CC}	GND	"	"				"				
			16	"	"	"	"	"	"	V_{CC}	GND	"				"				
			17	"	"	"	"	"	"	"	V_{CC}	GND				"				
			18	"	"	"	"	"	"	"	"	V_{CC}				"				
			19	"	"	"	"	"	"	"	"	"				"				
			20	"	"	"	"	"	"	"	"	"				"				
			21	"	"	"	"	"	"	"	"	"				"				
			22	"	"	"	"	"	"	"	"	"				"				
			23	"	"	"	"	"	"	"	"	"				"				
			24	"	"	"	"	"	"	"	"	"				"				
			25	"	"	"	"	"	"	"	"	"				"				
	I_{IH}	3010	26	"	GND	GND	GND	GND	GND	GND	GND	GND				"				
			27	GND	V_{CC}	GND	"	"	"	"	"	"				"				
			28	"	GND	V_{CC}	"	"	"	"	"	"				"				
			29	"	"	GND	V_{CC}	"	"	"	"	"				"				
			30	"	"	"	GND	V_{CC}	"	"	"	"				"				
			31	"	"	"	"	GND	V_{CC}	"	"	"				"				
			32	"	"	"	"	"	GND	V_{CC}	"	"				"				
			33	"	"	"	"	"	"	GND	V_{CC}	"				"				
			34	"	"	"	"	"	"	"	GND	V_{CC}				"				
			35	"	"	"	"	"	"	"	"	GND				"				
			36	"	"	"	"	"	"	"	"	"				"				
			37	"	"	"	"	"	"	"	"	"				"				
			38	"	"	"	"	"	"	"	"	"				"				
			39	"	"	"	"	"	"	"	"	"				"				
			40	"	"	"	"	"	"	"	"	"				"				
			41	"	"	"	"	"	"	"	"	"				"				
			42	"	"	"	"	"	"	"	"	"				"				
	I_{OLZ}	3020	43										GND	V_{CC}	V_{CC}	"	V_{CC}	V_{CC}	V_{CC}	V_{CC}
			44										V_{CC}	GND	V_{CC}	"	"	"	"	"
			45										"	V_{CC}	GND	"	"	"	"	"
			46										"	"	V_{CC}	"	GND	"	"	"
			47										"	"	"	"	V_{CC}	GND	"	"
			48										"	"	"	"	"	V_{CC}	GND	"
			49										"	"	"	"	"	"	V_{CC}	GND
			50										"	"	"	"	"	"	V_{CC}	V_{CC}

See footnotes at end of device types 05 and 06.

TABLE III. Group A inspection for device types 05 and 06 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	19	20	21	22	23	24	25	26	27	28	Algorithm (see appendix)	Measured terminal	Test limits Min	Test limits Max	Unit
			Case Y	22	23	24	25	27	28	29	30	31	32					
			Test no.	Q_7	$\overline{ET}$	A_{10}	$\overline{G}$	A_{11}	A_9	A_8	E2	$\overline{W}$	V_{CC}					
1 T_C = +25°C	I_{CCSR}	3005	1	3/	2.2 V	GND	GND	GND	GND	GND	5.5 V	GND	5.5 V		V_{CC}		5	mA
	I_{CCSB}		2	"	GND	"	"	"	"	"	0.8 V	"	"		"		"	"
	I_{CCEN}		3	"	0.8 V	"	"	"	"	"	2.2 V	"	"		"		"	"
	I_{CCOP}		4	"	4/	2/	2/	2/	2/	2/	4/	"	"	f = 1 MHz	"		20	"
	I_{CCSB1}		5	"	GND	GND	GND	GND	GND	GND	0.3 V	"	"		"		100	uA
	I_{CCSB1}		6	"	5.2 V	"	"	"	"	"	5.2 V	"	"		"		100	"
	I_{CCDR}		7	"	GND	"	"	"	"	"	0.3 V	"	2.0 V		"		75	"
	I_{CCDR}		8	"	1.7 V	"	"	"	"	"	1.7 V	"	2.0 V		"		75	"
	I_{IL}	3009	9		V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	5.5 V		A_{12}	-1	1	"
			10		"	"	"	"	"	"	"	"	"		A_7	"	"	"
			11		"	"	"	"	"	"	"	"	"		A_6	"	"	"
			12		"	"	"	"	"	"	"	"	"		A_5	"	"	"
			13		"	"	"	"	"	"	"	"	"		A_4	"	"	"
			14		"	"	"	"	"	"	"	"	"		A_3	"	"	"
			15		"	"	"	"	"	"	"	"	"		A_2	"	"	"
			16		"	"	"	"	"	"	"	"	"		A_1	"	"	"
			17		"	"	"	"	"	"	"	"	"		A_0	"	"	"
			18		GND	"	"	"	"	"	"	"	"		$\overline{E1}$	"	"	"
			19		V_{CC}	GND	"	"	"	"	"	"	"		A_{10}	"	"	"
			20		"	V_{CC}	GND	"	"	"	"	"	"		$\overline{G}$	"	"	"
			21		"	"	V_{CC}	GND	"	"	"	"	"		A_{11}	"	"	"
			22		"	"	"	V_{CC}	GND	"	"	"	"		A_9	"	"	"
			23		"	"	"	"	V_{CC}	GND	"	"	"		A_8	"	"	"
			24		"	"	"	"	"	V_{CC}	GND	"	"		E2	"	"	"
			25		"	"	"	"	"	V_{CC}	V_{CC}	GND	"		$\overline{W}$	"	"	"
	I_{IH}	3010	26		GND	GND	GND	GND	GND	GND	GND	"	"		A_{12}	"	"	"
			27		"	"	"	"	"	"	"	"	"		A_7	"	"	"
			28		"	"	"	"	"	"	"	"	"		A_6	"	"	"
			29		"	"	"	"	"	"	"	"	"		A_5	"	"	"
			30		"	"	"	"	"	"	"	"	"		A_4	"	"	"
			31		"	"	"	"	"	"	"	"	"		A_3	"	"	"
			32		"	"	"	"	"	"	"	"	"		A_2	"	"	"
			33		"	"	"	"	"	"	"	"	"		A_1	"	"	"
			34		"	"	"	"	"	"	"	"	"		A_0	"	"	"
			35		V_{CC}	"	"	"	"	"	"	"	"		$\overline{E1}$	"	"	"
			36		GND	V_{CC}	"	"	"	"	"	"	"		A_{10}	"	"	"
			37		"	GND	V_{CC}	"	"	"	"	"	"		$\overline{G}$	"	"	"
			38		"	"	GND	V_{CC}	"	"	"	"	"		A_{11}	"	"	"
			39		"	"	"	GND	V_{CC}	"	"	"	"		A_9	"	"	"
			40		"	"	"	"	GND	V_{CC}	"	"	"		A_8	"	"	"
			41		"	"	"	"	"	GND	V_{CC}	"	"		E2	"	"	"
			42		"	"	"	"	"	GND	GND	V_{CC}	"		$\overline{W}$	"	"	"
	I_{OLZ}	3020	43	V_{CC}	2.2 V		2.2 V				"	"	"		Q_0	"	"	"
			44	"	"		"				"	"	"		Q_1	"	"	"
			45	"	"		"				"	"	"		Q_2	"	"	"
			46	"	"		"				"	"	"		Q_3	"	"	"
			47	"	"		"				"	"	"		Q_4	"	"	"
			48	"	"		"				"	"	"		Q_5	"	"	"
			49	"	"		"				"	"	"		Q_6	"	"	"
			50	GND	"		"				"	"	"		Q_7	"	"	"

See footnotes at end of device types 05 and 06.

TABLE III. Group A inspection for device types 05 and 06 - Continued. 1/

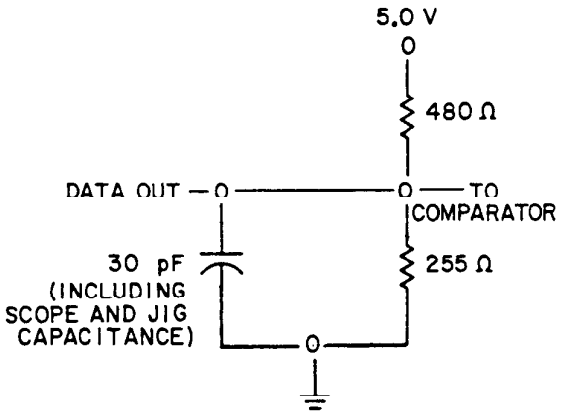
Subgroup	Symbol	MIL-STD-883 method	Case X	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
			Case Y	3	4	5	6	7	8	9	10	11	13	14	15	16	18	19	20	21
			Test no.	A_{12}	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_0	Q_1	Q_2	V_{SS}	Q_3	Q_4	Q_5	Q_6
1 T_C = +25°C	I_{OHZ}	3021	51										V_{CC}	GND	GND	GND	GND	GND	GND	GND
			52										GND	V_{CC}	GND	"	"	"	"	"
			53										"	GND	V_{CC}	"	"	"	"	"
			54										"	"	GND	"	V_{CC}	"	"	"
			55										"	"	"	"	GND	V_{CC}	"	"
			56										"	"	"	"	"	GND	V_{CC}	"
			57										"	"	"	"	"	"	GND	V_{CC}
			58										"	"	"	"	"	"	GND	GND
	V_{OL}	3007	59-66	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	5/	"	5/	5/	5/	5/
	V_{OH}	3006	67-74	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	6/	"	6/	6/	6/	6/
2	Same tests as for subgroup 1, except T_C = +125°C																			
3	Same tests as for subgroup 1, except T_C = -55°C																			
4 T_C = +25°C	C_{IN}	3012	75	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	GND	7/	7/	7/	7/
	C_{OUT}	3012	76	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	7/	"	7/	7/	7/	7/
7 T_C = +25°C	I/O	Functional test	77	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	9/	"	9/	9/	9/	9/
	V_{DR}		78	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	10/	"	10/	10/	10/	10/
8 T_C = -55°C and T_C = +125°C	Same tests as for subgroup 7, except at both T_C = -55°C and +125°C.																			
9 T_C = +25°C	Table I ac parameter	Functional test	79	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	11/	GND	11/	11/	11/	11/
			80	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	t_{ELQV}		81	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	t_{ELQV}		82	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	t_{AVQV}	13/	83	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
	t_{AVQV}	13/	84	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"
10	Same tests as for subgroup 9, except T_C = +125°C																			
11	Same tests as for subgroup 9, except T_C = -55°C																			

1/ Pins not designated may be V_{IH} or V_{IL}.
2/ Inputs = GND and V_{CC}.
3/ Outputs open.
4/ Device 05: E1 = 0.8 V, E2 = 2.2 V; Device 06: E1 and E2 toggling at V_{IH} = V_{CC} and V_{IL} = GND.
5/ Outputs preconditioned to logic "0". Output forcing current shall be 4 mA. Logic input levels during measurements shall be V_{IL} = 0.8 V, V_{IH} = 2.2 V.
6/ Outputs preconditioned to logic "1". Output forcing current shall be -1 mA. Logic input levels during measurements shall be V_{IL} = 0.8 V, V_{IH} = 2.2 V.
7/ See 4.4.1c.
8/ Use limits in table I.
9/ F = 2 MHz, V_{IH} = 2.4 V, V_{IL} = 0.4 V, I_{OH} = -4 mA, I_{OL} = 4 mA, V_{OH} > 1.5 V and V_{OL} < 1.5 V.
10/ Data retention voltage (V_{DR}) is guaranteed by testing using a 500 ms pause at the test voltage with a data pattern. Repeat with the complemented data pattern.
11/ Input pulse levels: 0 to 3 V; input rise and fall times: 5 ns maximum; input and output timing reference level: 1.5 V; output load; dynamic bridge load (TTL gate equivalent) and C_L = 50 pF. For C_L > 50 pF, access times are derated 0.15 ns per pF.
12/ Use limits in table I. A combination of test patterns is used to verify all of the ac parameters. Each pattern does not test all the ac parameters inclusively.
13/ Device type 05 only.

TABLE III. Group A inspection for device types 05 and 06 - Continued. 1/

Subgroup	Symbol	MIL-STD-883 method	Case X	19	20	21	22	23	24	25	26	27	28	Algorithm (see appendix)	Measured terminal	Test limits Min	Test limits Max	Unit
			Case Y	22	23	24	25	27	28	29	30	31	32					
			Test no.	Q_7	$\overline{ET}$	A_{10}	$\overline{G}$	A_{11}	A_9	A_8	E2	$\overline{W}$	V_{CC}					
1 T_C = +25°C	I_{OHZ}	3021	51	GND	2.2 V		2.2 V				GND	V_{CC}	5.5 V		Q_0	-1	1	μA
			52	"	"		"				"	"	"		Q_1	"	"	"
			53	"	"		"				"	"	"		Q_2	"	"	"
			54	"	"		"				"	"	"		Q_3	"	"	"
			55	"	"		"				"	"	"		Q_4	"	"	"
			56	"	"		"				"	"	"		Q_5	"	"	"
			57	"	"		"				"	"	"		Q_6	"	"	"
			58	V_{CC}	"		"				"	"	"		Q_7	"	"	"
	V_{OL}	3007	59-66	5/	5/	5/	5/	5/	5/	5/	5/	5/	4.5 V		Q_0-Q_7		0.4	V
	V_{OH}	3006	67-74	6/	6/	6/	6/	6/	6/	6/	6/	6/	4.5 V		Q_0-Q_7	2.4		V
2																		
3																		
4 T_C = +25°C	C_{IN}	3012	75	7/	7/	7/	7/	7/	7/	7/	7/	7/			Input		8/	
	C_{OUT}	3012	76	7/	7/	7/	7/	7/	7/	7/	7/	7/			Output		8/	
7 T_C = +25°C	I/O	Functional test	77	9/	9/	9/	9/	9/	9/	9/	9/	9/	4.5 V	Pattern 5				
	V_{DR}		78	10/	10/	10/	10/	10/	10/	10/	GND	10/	2.0 V	Pattern 4				
8 T_C = -55°C and T_C = +125°C																		
9 T_C = +25°C	Table I ac parameter	Functional test	79	11/	11/	11/	11/	11/	11/	11/	11/	11/	4.5 V	Patterns 1,3,5	Q		12/	
			80	"	"	"	"	"	"	"	"	"	5.5 V	Patterns 1,3,5	Q		12/	
	t_{ELQV}		81	"	"	"	"	"	"	"	"	"	4.5 V	Pattern 3	Q		150	ns
	t_{ELQV}		82	"	"	"	"	"	"	"	"	"	5.5 V	Pattern 3	"		"	"
	t_{AVQV}	13/	83	"	"	"	"	"	"	"	"	"	4.5 V	Pattern 3	"		"	"
	t_{AVQV}	13/	84	"	"	"	"	"	"	"	"	"	5.5 V	Pattern 3	"		"	"
10																		
11																		

Device types 01, 02, 03, and 04



Device types 05 and 06

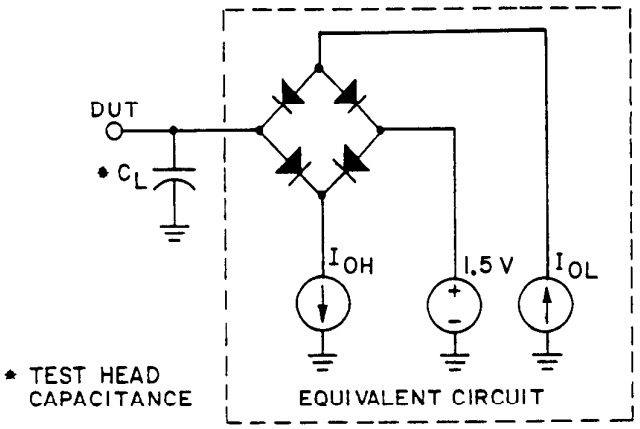


FIGURE 9. Output load circuit.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows. End-point electrical tests shall be as specified in table II herein. For those designs using a die coat, a measurement shall be made of the thickness of the die coat. The thickness shall be greater than or equal to that measured on the initial qualification devices or the devices used for requalification after a change (see 4.4.1c).

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, and voltage stress cooldown procedures. When devices are measured at +25°C following application of the operating life or burn-in test condition, they shall be cooled to within 10°C of their stable power condition at room temperature prior to removal of bias.

4.5.3 Delta measurements. Delta measurements, as specified in table II, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IV.

TABLE IV. Delta limits at +25°C.

Parameters 1/ 2/	Limits			
	01, 02	03	04	05, 06
I_{DD}	+5 μA	±15 μA	±25 μA	
V_{OL}	±60 mV	±60 mV	±60 mV	+60 mV
V_{OH}	±200 mV	±400 mV	±400 mV	-400 mV
I_{CCSB1}				+30 μA
I_{OHZ}, I_{OLZ}				±500 nA
I_{IL}, I_{IH}	+50 nA	±100 nA	±100 nA	±500 nA

1/ Conditions and mechanization of measurements shall be as specified in table III, subgroup 1.
2/ Delta limits apply to an increase from the initial value (e.g., pre-life test I_{IH} = -120 nA, post-life test I_{IH} = -170 nA).

4.5.4 Electrostatic discharge sensitivity (ESD) classification. The method and procedures shall be in accordance with method 3015 of MIL-STD-883. The test is only required to be performed on initial qualification.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design application and logistic support of existing equipment.

6.2 Application and operation guidelines.

6.2.1 Initialization. Operation to specifications guaranteed 2.0 ms after V_{CC} is initially applied. Transitioning to and from data retention voltage (V_{DR}) does not require a 2.0 ms period; t_{DRS} and t_{DRR} apply in this situation (for device types 01 through 04). Recommended transition time to and from data retention for device types 05 and 06 is minimum cycle time.

6.2.2 Read operation.

a. Since a read cycle can only occur during intervals where chip enable is low and write enable is high, these are conditions assumed for read cycle 1.

b. Read cycle 2 assumes that all address inputs are both valid and stable throughout the time chip select is low.

6.2.3 Write operation.

a. Since a write cycle can only occur during intervals where both chip enable and write enable are low, write cycle 2 assumes that write enable is the latter of the two signals to go low (active) and is also the first of the two signals to go high (inactive). Consequently, timing considerations are referenced to the edges of write enable rather than chip enable.

b Write cycle 2 assumes that, of the two control signals, chip enable is the latter of the two to go low (active) and is the first of the two signals to go high (inactive). Consequently, timing considerations are referenced to the edges of chip enable rather than write enable.

c. Since write enable is gated internally with chip enable, the value of write enable during periods where chip enable is high are irrelevant (i.e., don't care). Thus, whenever write enable transitions to the low state prior to chip enable, all timing references will be to the falling edge of chip enable rather than write enable. Similarly, whenever chip enable transitions to the high state prior to write enable, all timing references will be to the rising edge of chip enable rather than write enable.

6.3 Ordering data. The acquisition documents should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirement for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for packaging and packing.

f. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

g. Requirements for product assurance options.

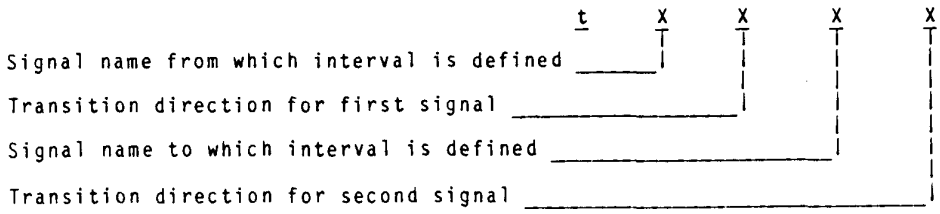
h. Requirements for special lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements shall not apply to direct purchase by or direct shipment to the Government.

i. Requirements for "JAN" marking.

6.4 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1331 and as follows:

V_{CC}	Supply voltage
V_{SS}	Common or reference voltage
Enable ($\overline{E}$)	Chip enable
Write ($\overline{W}$)	Read/write input
D_{IN} (D)	Data input
D_{OUT} (Q)	Data output
A_0-A_{15}	Address inputs
V_{IL}	Logical low input voltage
V_{IH}	Logical high input voltage
V_{OL}	Logical low output voltage
V_{OH}	Logical high output voltage
C_{IN}	Input capacitance
C_{OUT}	Output capacitance
t_{AVQV}	Address access time
t_{ELEH}	Chip enable pulse negative width
t_{ELWH}	Chip enable to end of write
t_{AVWH}	Address setup to end of write
t_{WLWH}	Write pulse width
t_{WLQZ}	Write enable to output in high-z
t_{WHQX}	Output active from end of write
t_{AVEH}	Address valid to enable high
t_{AVEL}	Address valid to enable low
t_{WLEH}	Write low to enable high
t_{EHAX}	Address hold time after enable
t_{DVEH}	Data valid to enable high
t_{EHDX}	Data hold time (enable controlled)
t_{ELICCH}	Enable low to power-up time
t_{EHICCL}	Enable high to power-down time
$\overline{OE}$ (G)	Output enable
DQ	Data input/output
I_{CC}, I_{CCOP}	Operating supply current
I_{SB}, I_{CCSB1}	Standby supply current (CMOS)
I_{CCSB}	Standby supply current (TTL)
I_{CCEN}	Enable supply current
I_{DR}, I_{CCDR}	Data retention supply current
I_{IH}, I_{IL}, I_I	Input current leakage
I_{OZH}, I_{OZL}, I_{IOZ}	High impedance output leakage current
V_{DR}, V_{CCDR}	Data retention supply voltage
$C_{I/O}$	Input/output capacitance
t_{ELQV}, t_{E1LQV}, t_{E2HQV}	Chip enable access time
t_{AVAV}, t_{E1LE1L}, t_{E2HE2H}, t_{AVAX}	Read/write cycle time
t_{OLQV}	Output enable access time
t_{EHQZ}, t_{E1HQZ}, t_{E2LQZ}	Chip disable to output disable
t_{GHQZ}	Output enable high to output disable
t_{AXQX}, t_{AVQX}	Output hold after an address change
t_{ELQX}, t_{E1LQX}, t_{E2HQX}	Chip enable to output active
t_{GLQX}	Output enable to output active
t_{ELEH}, t_{E1LE1H}, t_{E2HE2L}	Chip enable pulse negative width
t_{AVWL}, t_{AVEL}, t_{AVE1L}, t_{AVE2H}	Address setup time
t_{WHAX}, t_{EHAX}, t_{E1HAX}, t_{E2LAX}	Write recovery time
t_{DVWH}, t_{DVEH}, t_{DVE1H}, t_{DVE2L}	Data valid to end of write
t_{WHDX}, t_{EHDX}, t_{E1HDX}, t_{E2LDX}	Data hold time
t_{E1LAX}, t_{E2HAX}	Address hold time
t_{E1HE1L}, t_{E2LE2H}	Address unlatch time

6.4.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. Thus the format is:



a. Signal definitions:

A = Address
D = Data in
Q = Data out
W = Write enable
E = Chip enable

b. Transition definitions:

H = Transition to high
L = Transition to low
V = Transition to valid
X = Transition to invalid or don't care
Z = Transition to off (high impedance)

6.4.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.4.3 Waveforms.

Waveform	Input	Output
	Must be valid	Must be valid
	Change from H to L	Will change from H to L
	Change from L to H	Will change from L to H
	Don't care any change permitted	Changing state unknown
		High impedance

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 3.3). Longer leads and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military device type	Generic-industry type
01	7187S55 99C641-55
02	7187S45 99C641-45
03	7187L55 99CL641-55
04	7187L70 99CL641-70
05	65642
06	65643

6.7 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Input protection circuitry has been designed into the device to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surfaces.

b. Ground test equipment, tools, and operator.

c. Handling of devices by the leads should be avoided.

d. Devices should be stored in conductive foam or carriers.

e. The use of plastic, rubber or silk in MOS area should be avoided.

f. Relative humidity should be maintained above 50 percent, if practical.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS.

30.1 Algorithm A (pattern 1).

30.1.1 Address complement, data background = all "0".

This pattern produces maximum address line noise. It is performed in the following manner:

Step 1. Load memory with background data.
Step 2. Read minimum address location.
Step 3. Load minimum address location with "1".
Step 4. Read maximum address location.
Step 5. Load maximum address location with "1".
Step 6. Read minimum address location +1.
Step 7. Load minimum address location +1 with "1".
Step 8. Read maximum address location -1.
Step 9. Load maximum address location -1 with "1".
Step 10. Repeat steps 2 through 9 until all address locations have been read and loaded with "1".
Step 11. Repeat steps 2 though 10 reading "1" and loading "0".
Step 12. Read memory, all "0".

30.2 Algorithm B (pattern 2).

30.2.1 GALPAT (ping pong) data background = "0".

This pattern tests for performance sensitivities by testing all possible combinations of address and data out transitions. It is performed in the following manner:

Step 1. Load memory with data background.
Step 2. Write data complement in location 0 (test bit).
Step 3. Alternately read test bit and each location in the array.
Step 4. Write the test bit back to background data.
Step 5. Repeat steps 2 through 4 with each location in the array.
Step 6. Repeat steps 1 through 5 with complemented background data.

30.3 Algorithm C (pattern 3).

30.3.1 March data, data background = all "0".

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

Step 1. Load memory with background data.
Step 2. Read location 0.
Step 3. Write data complement in location 0.
Step 4. Read data complement in location 0.
Step 5. Repeat steps 2 through 4 for all other locations in memory (sequentially).
Step 6. Read data complement at location 0.
Step 7. Write data at location 0.
Step 8. Read data at location 0.
Step 9. Repeat steps 6 through 8 for all other locations in the memory (sequentially).
Step 10. Repeat steps 1 through 9 with data background of all "1".

30.4 Algorithm D (pattern 4).

30.4.1 Data retention, data background = checkerboard.

This algorithm tests for data retention mode functionality. It is performed in the following manner:

Step 1. Load memory with background data.
Step 2. Set chip enable = V_{CC}.
Step 3. Reduce V_{CC} and chip enable to minimum V_{DR}.
Step 4. Pause for 200 ms.
Step 5. Bring V_{CC} and chip enable back up and test for background data.
Step 6. Repeat steps 1 through 5 with complemented background data.

30.5 Algorithm E (pattern 5).

30.5.1 Checkerboard, $\overline{\text{checkerboard}}$.

Step 1. Load memory with a checkerboard pattern.
Step 2. Read the memory, verifying the checkerboard pattern.
Step 3. Load the memory with a $\overline{\text{checkerboard}}$ pattern.
Step 4. Read the memory, verifying the $\overline{\text{checkerboard}}$ pattern.

Custodians:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1041)