

MILITARY SPECIFICATION

MICROCIRCUITS, DIGITAL, NMOS, 65,536 BIT, RANDOM ACCESS MEMORY (RAM),
 MONOLITHIC SILICON

This specification is approved for use by the Department of the Air Force, and is available for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, N-channel, dynamic, NMOS, 65,536/1-bit, random access memory microcircuits utilizing a 128 cycle refresh architecture and having pin number 1 as a no-connect. Two product assurance classes are provided and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510, and as specified herein.

1.2.1 Device type. The device type shall be as follows:

<u>Device type</u>	<u>Circuit organization</u>	<u>Access time</u>	<u>Refresh</u>
01 ($T_{case} = -55^{\circ}C$ instant-on to $+110^{\circ}C$ operating) <u>1/</u>	65,536/1-bit RAM	150 ns	128 Cycles (1 ms)
02 ($T_{case} = -55^{\circ}C$ instant-on to $+110^{\circ}C$ operating) <u>1/</u>	65,536/1-bit RAM	150 ns	128 Cycles (2 ms)
03 ($T_{case} = -55^{\circ}C$ instant-on to $+110^{\circ}C$ operating) <u>1/</u>	65,536/1-bit RAM	200 ns	128 Cycles (2 ms)

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

<u>Letter</u>	<u>Case outline (see MIL-M-38510, appendix C)</u>
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
Z	C-10 (18 terminal, .285" x .425"), chip carrier package

1.3 Absolute maximum ratings.

Voltage on any pin relative to V_{SS}	- - - - -	-1.5 V to +7 V
Storage temperature range (ambient)	- - - - -	$-65^{\circ}C$ to $+150^{\circ}C$
Power dissipation (minimum cycle time)	- - - - -	1.0 W maximum
Thermal resistance (minimum cycle time)	- - - - -	$\theta_{JC} = 15^{\circ}C/W$ maximum
Lead temperature (soldering, 5 seconds)	- - - - -	$270^{\circ}C$ maximum
Maximum junction temperature (T_J)	- - - - -	$+150^{\circ}C$
Short circuit output current	- - - - -	150 mA

1/ See initialization 6.4.1.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss ABF, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

1.3.1 Alpha particle induced error rate. The error rate shall not exceed 1 error in 1×10^6 device operating hours, under the following test conditions:

- a. $V_{CC} = 4.5 \text{ V}$
- b. $T_C = 25^\circ\text{C}$.
- c. Device in a checkerboard pattern.
- d. Cycle time equal to 250 ns.

1.4 Recommended operating conditions:

	Min	Max	Unit
Supply voltages:			
V_{CC} - - - - -	4.5	5.5	V dc
V_{SS} - - - - -	0 <u>2/</u>	0 <u>2/</u>	V dc
High-level input voltage:			
All inputs (V_{IH}) - - - - -	2.4	6.5	V dc
Low-level input voltage:			
All inputs (V_{IL}) - - - - -	-1.5	0.8	V dc
Refresh cycle time (t_{REF})			
Device type 01 - - - - -	---	1.0	ms
Device types 02 and 03 - - - - -	---	2.0	ms
Case operating temperature range (T_C) - - -	-55	+110	$^\circ\text{C}$

2. APPLICABLE DOCUMENTS

2.1 Government specifications and standards. Unless otherwise specified, the following specifications and standards, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this specification to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification For.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of specifications, standards, handbooks, drawings, and publications required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting officer.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein, the text of this specification shall take precedence.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Case outlines. The case outlines shall be as specified in 1.2.3.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

2/ V_{SS} is common for all supply voltages.

TABLE I. Electrical performance characteristics.

Characteristic	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Output high voltage	V_{OH}	$I_{OH} = -5.0 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	A11	2.4	V_{CC}	V
Output low voltage	V_{OL}	$I_{OL} = 4.0 \text{ mA}$ $V_{CC} = 4.5 \text{ V}$	A11		0.4	V
Input leakage, all inputs	$I_{I(L)(H)}$	$V_{IN} = 0 \text{ to } 6.5 \text{ V}$	A11	-10	+10	μA
Output leakage	$I_{O(L)(H)}$	$\overline{\text{RAS}} \text{ \& } \overline{\text{CAS}} = V_{IH}$ $V_{OUT} = 0.0 \text{ to } 5.5 \text{ V}$	A11	-10	+10	μA
Supply current from V_{CC}	$I_{CC1} \underline{1/}$	$\overline{\text{RAS}}$ & $\overline{\text{CAS}}$ cycling $t_{RC} = 250 \text{ ns}$, See figure 10	A11		60	mA
	I_{CC2}	$\overline{\text{RAS}}$ & $\overline{\text{CAS}} = V_{IH}$ $D_{OUT} = \text{High Z}$	A11		10	mA
	I_{CC3}	$\overline{\text{RAS}}$ cycling, $t_{RC} = 250 \text{ ns}$ $\overline{\text{CAS}} = V_{IH}$, See figure 11	A11		50	mA
Input capacitance (A_0 - A_7)	$C_{IN1} \underline{2/}$		A11		5	pF
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, D_{IN} , $\overline{\text{WE}}$ input capacitance	$C_{IN2} \underline{2/}$		A11		10	pF
Output capacitance	$C_{OUT} \underline{2/}$		A11		8	pF
Random read or write cycle time	t_{RC}	See figures 5, 6, 7, 9	01,02 03	250 345	10100 10145	ns
Read-write cycle time	$t_{R/W}$	See figures 5, 8	01,02 03	270 370	10100 10145	ns
Access time from $\overline{\text{RAS}}$	$t_{RAC} \underline{3/}$	See figures 5, 6, 8 $t_{RCD} = \text{Min}$	01,02 03		150 200	ns
Access time from $\overline{\text{CAS}}$	$t_{CAC} \underline{3/}$	See figures 5, 6, 8 $t_{RCD} \geq \text{Max}$	01,02 03		85 115	ns
Output buffer turn off delay	t_{OFF}	See figures 5, 6, 8	A11	0	40	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}	See figures 5 through 9	01,02 03	90 135		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristic	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	See figures 5 through 9	01,02 03	150 200	10000 10000	ns
$\overline{\text{RAS}}$ hold time	t_{RSH}	See figures 5, 6, 7, 8	01,02 03	90 115		ns
$\overline{\text{CAS}}$ hold time	t_{CSH}	See figures 5, 6, 7, 8	01,02 03	150 200		ns
$\overline{\text{CAS}}$ pulse width	t_{CAS}	See figures 5, 6, 7, 8	01,02 03	90 115		ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	See figures 5, 6, 7, 8	01,02 03	25 35	60 80	ns
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	See figures 5, 6, 7, 8	A11	0		ns
Row address setup time	t_{ASR}	See figures 5 through 9	A11	0		ns
Row address hold time	t_{RAH}	See figures 5 through 9	01,02 03	20 25		ns
Column address setup time	t_{ASC}	See figures 5, 6, 7, 8	A11	0		ns
Column address hold time	t_{CAH}	See figures 5, 6, 7, 8	01,02 03	30 40		ns
Column address hold time referenced to $\overline{\text{RAS}}$	t_{AR}	See figures 5, 6, 7, 8	01,02 03	80 110		ns
Read command setup time	t_{RCS}	See figures 5, 6, 8	A11	0		ns
Read command hold time	t_{RCH}	See figures 5, 6, 8	A11	0		ns
Write command hold time	t_{WCH}	See figures 5, 7	01,02 03	45 55		ns
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	See figures 5, 7	01,02 03	120 150		ns
Write command pulse width	t_{WP}	See figures 5, 7, 8	01,02 03	45 55		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Characteristic	Symbol	Conditions	Device type	Limits		Unit
				Min	Max	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	See figures 5, 7, 8	01,02 03	45 55		ns
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	See figures 5, 7, 8	01,02 03	45 55		ns
Data in setup time	t_{DS}	See figures 5, 7, 8	A11	0		ns
Data in hold time	t_{DH}	See figures 5, 7, 8	01,02 03	45 55		ns
Data in hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	See figures 5, 7, 8	01,02 03	120 150		ns
Refresh period	t_{REF}		01 02,03		1.0 2.0	ms
Write command setup time	t_{WCS}	See figures 5, 7	A11	0		ns
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay	t_{CWD}	See figures 5, 8	01,02 03	50 90		ns
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay	t_{RWD}	See figures 5, 8	01,02 03	110 160		ns
Read command hold time referenced to $\overline{\text{RAS}}$	t_{RRH}	See figures 5, 6	01,02 03	25 30		ns

1/ Depends on cycle rate and output load. Limits are for cycle rates listed in conditions column. Limits are for one Schottky TTL and 100 pF. Worse case data pattern (alternate "1"s & "0"s) at a repetition frequency of 4.0 MHz for normal cycle.

2/ Capacitance measured with Boonton Meter or effective capacitance calculated from the equation:

$$C = \frac{I_{\Delta t}}{\Delta V}$$
 with ΔV equal to 3 volts and $V_{\text{CC}} = 5.0$ V.

3/ Load = One Schottky TTL +100 pF or equivalent.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Truth table. The truth table shall be as specified on figure 3.

3.2.1 Functional tests. The functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, then alternate test patterns to accomplish the same results shall be submitted to the qualifying activity for approval.

3.2.5 Die overcoat. All devices supplied under this specification shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. Polyimide and silicone coatings are allowed as an overcoat on the die for alpha particle protection provided each lot (i.e. polyimide and silicon coating lot) shall be subjected to and pass the internal moisture content test. The internal moisture content for device class S and class B after completion of all screening shall not exceed 5,000 ppm at 100°C.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 and 6.5 herein.

3.4 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I, and apply over the full recommended case operating temperature range.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (pre burn-in) (method 5004)	2, 10	2, 10
Final electrical test parameters (method 5004)	1,2*,3,9,10*,11	1,2*,3,10*,11
Group A test requirements (method 5005)	1,2,3,4,9,10,11	1,2,3,4,10,11
Group B test requirements (method 5005) subgroup 5	1,2,3,9,10,11	N/A
Group C end-point electrical parameters (method 5005)	NA	1,2,3,10,11
Additional electrical subgroups for group C periodic inspections	None	None
Group D end-point electrical parameters (method 5005)	1,2,3,10,11	1,2,3,10,11

*The PDA applies to subgroups 2 and 10 (see 4.2d.), only functional attributes of subgroup 10 shall apply to PDA.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 46 (see MIL-M-38510, appendix E).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

- a. When the alternate screening option of the alternate screening procedures for class B microcircuits of method 5004 of MIL-STD-883 is applied, the following additional items are applicable:
 - (1) Internal visual, method 2010 of MIL-STD-883, condition B. In addition to the changes indicated by the alternate screens of method 5004, the following additional clarifications and deletions are applicable:
 - (a) Metallization inspection shall be applicable to the top layer metal conductor (i.e., A1) and need not include "underlying conductors" such as polysilicon.
 - (b) Omit 3.2.1.1(b) through 3.2.1.1(e), 3.2.1.2(b) through 3.2.1.2(e) and 3.2.3(e) (items 3.2.1.1(f) and 3.2.3(g) do not apply).
 - (2) Burn-in duration for class B shall be 160 hours minimum.
 - (3) The following voltage stress test may be used to satisfy 3.3.1c of method 5004 of MIL-STD-883. The voltage stress test shall be added to screening procedure (method 5004 of MIL-STD-883) after constant acceleration and before the pre-burn-in electricals. Voltage stress test condition is shown on figure 4, (same as burn-in) or equivalent, with the following voltage modifications:
 - (a) $V_{CC} = +7.0$ volts
 - (b) $T_A = 125^{\circ}\text{C}$ minimum for 12 hours minimum.
- b. Burn-in (method 1015 of MIL-STD-883):
 - (1) Test condition D, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = 125^{\circ}\text{C}$ minimum.
- c. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.
- d. The percent defective allowable (PDA) shall be as specified in MIL-M-38510.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

- a. Electrical test requirements shall be as specified in table II herein.
- b. Subgroups 5, 6, 7, and 8 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. Subgroup 4 shall be measured only for initial qualification and after process or design changes which may affect capacitance. Perform C_{IN1} , C_{IN2} , and C_{OJT} parameter measurements to table I limits. Measurements are made with a Boonton meter or effective capacitance is calculated from the equation $C = \frac{I \Delta t}{\Delta V}$ with ΔV equal to 3 volts and $V_{CC} = 5.0$ V.
- d. LTPD's for subgroups may be combined as follows:

<u>Subgroups</u>	<u>Combined LTPD</u>
1,9	5
2,10	7
3,11	7

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. A special subgroup shall be added using an LTPD of 15 for class S and B devices. This subgroup shall consist of a high voltage test of the input protection circuits, VZAP (see 4.5.3).

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. Soft error rate - System testing to be performed using conditions stated in 1.3.1. Accumulate 10^5 device hours minimum for the specified generic device type.
- c. Steady-state life test (method 1005 of MIL-STD-883) conditions:
 - (1) Test condition D, using the circuit shown on figure 4, or equivalent.
 - (2) $T_A = 125^\circ\text{C}$ minimum.
 - (3) Test duration - 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

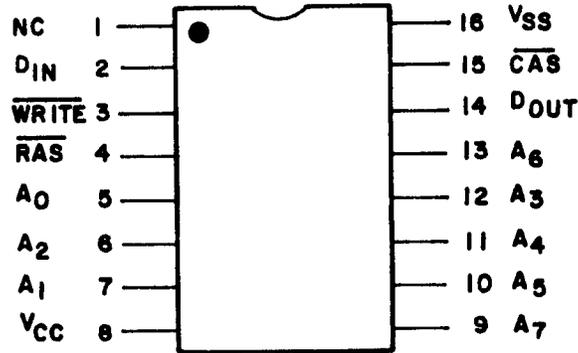
4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883. End-point electrical parameters shall be as specified in table II herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

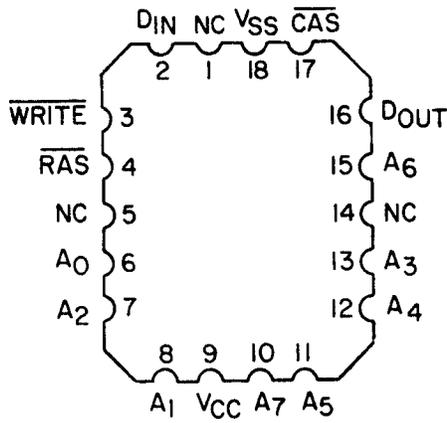
4.5.1 Voltage and current. All voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, and voltage stress cooldown procedures. When devices are measured at 25°C following application of the operating life or burn-in test condition, they shall be cooled to 35°C prior to removal of the bias.

Device types 01, 02, and 03
Case E



Case Z



Option A with active terminals on plane 1.

A ₀ -A ₇	Address Inputs
CAS	Column Address Strobe
D _{IN}	Data In
D _{OUT}	Data Out
WE	Write Input
RAS	Row Address Strobe

FIGURE 1. Terminal connections.

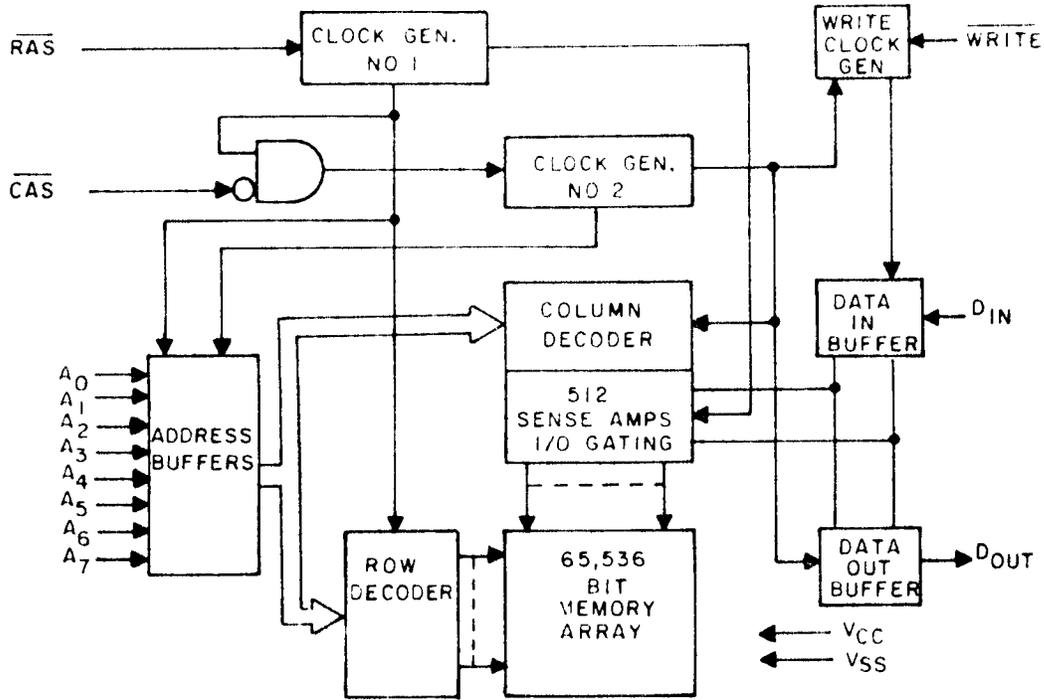


FIGURE 2. Block diagram.

Truth table						
Inputs						Output
Operation <u>7/</u>	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	D_{IN}	ADDR.	$\overline{\text{Write}}$	D_{OUT} <u>1/</u>
Chip not selected	H	H	X <u>2/</u>	X	X	High Z
Write "L" in cell A_{xy} <u>3/</u>	L	L	L	A_{xy}	L	High Z <u>4/</u>
Write "H" in cell A_{xy}	L	L	H	A_{xy}	L	High Z <u>4/</u>
Read data in cell A_{xy}	L	L	X	A_{xy}	H	High Z (A_{xy})
RAS only refresh	L	H	X	$\text{A}_{x5/}$	X	High Z
Hidden $\overline{\text{RAS}}$ only refresh	L	L	H	A_x	H	Data ($\text{A}_{x-N,y-N}$) <u>6/</u>

1/ D_{OUT} is not inverted from D_{IN} .

2/ "X" = Don't care.

3/ A_{xy} denotes proper address logic to address cell A_{xy} .

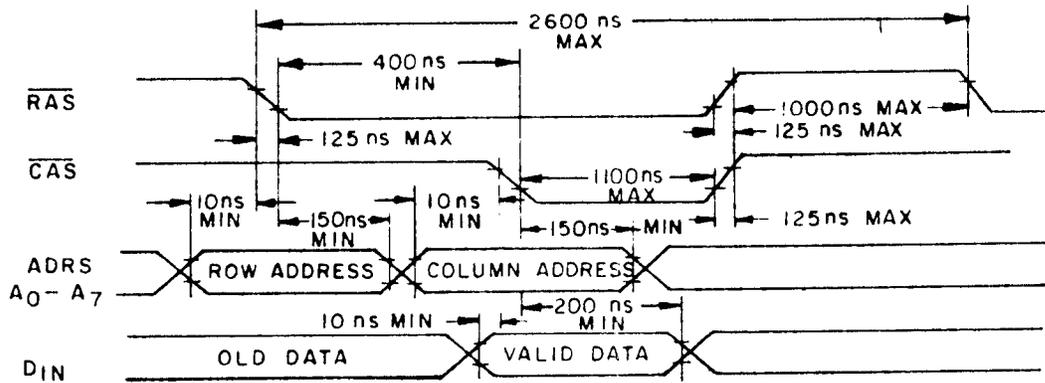
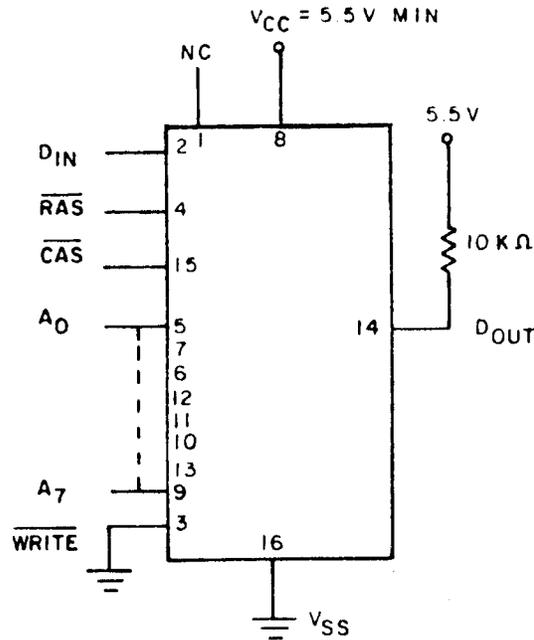
4/ For "EARLY WRITE" timing, data out remains at high impedance. For "LATE WRITE" timing, data out is valid from access time to the beginning of a subsequent cycle, or until $\overline{\text{CAS}}$ goes to a high level.

5/ A_x depends only on $\text{A}_0\text{-A}_6$; A_7 is a don't care.

6/ When $\overline{\text{CAS}} = \text{V}_{\text{IL}}$, the data output will contain data from the last valid read cycle (i.e., N cycles before).

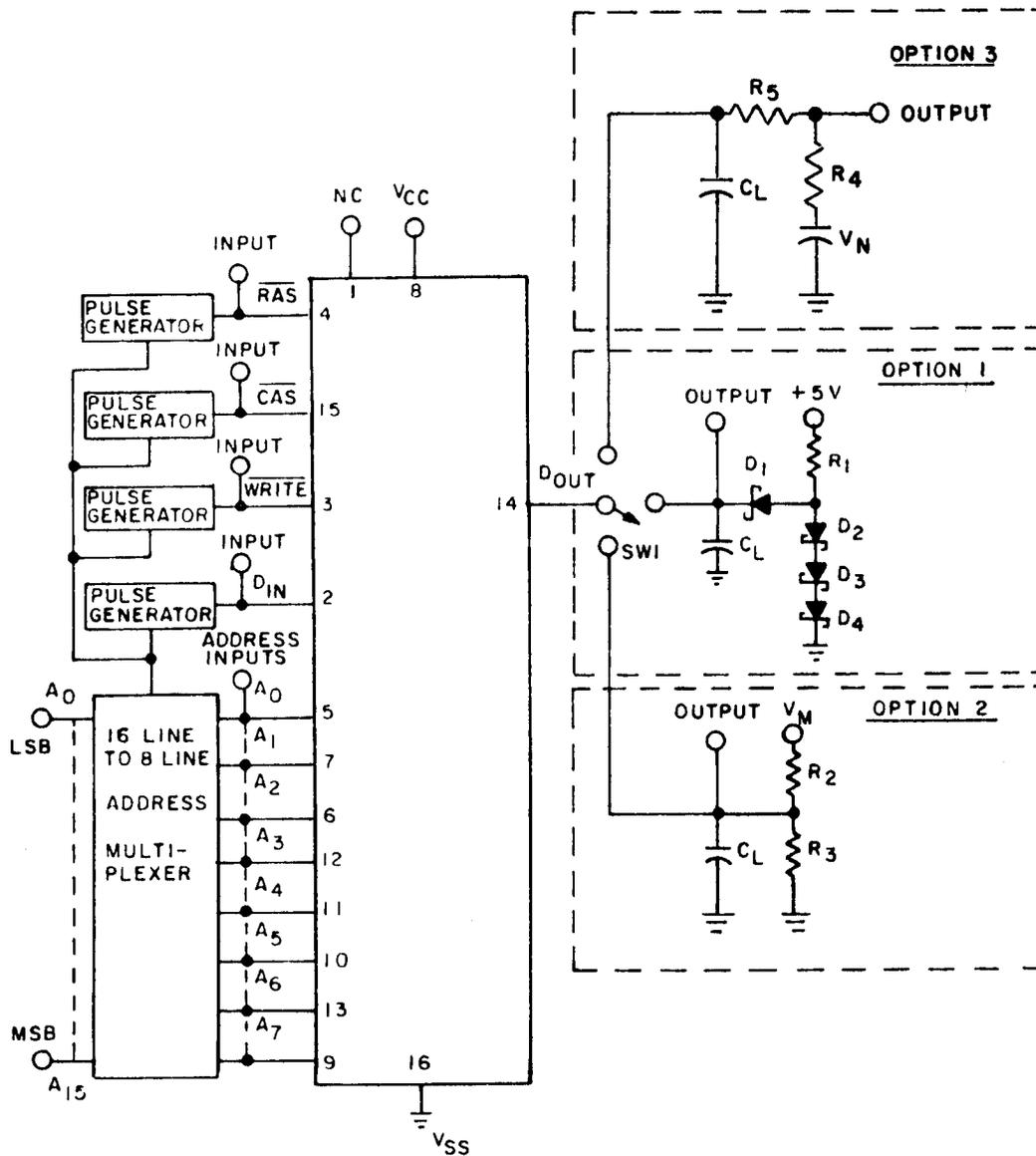
7/ A 100 μs pause plus eight initialization cycles required before truth table applies, total time 500 μs . All timing requirements must be applied.

FIGURE 3. Truth table.



NOTES: Measurement points are V_{IL} and V_{IH}
 A_0-A_7 = Binary count LSB-MSB
 t_{RISE} = 125 ns max.
 t_{FALL} = 125 ns max.

FIGURE 4. Burn-in and steady state life test circuit.



NOTES:

1. $C_L = 100 \text{ pF min-}$ (includes scope probe, wiring, and stray wiring without package in test fixture).
2. D1-D4 are 1N3064 or equivalent.
3. All generators t_{TLH} and $t_{THL} \leq 10 \text{ ns}$.
4. All resistors are 1/2 watt.
5. Option 1 or option 2 load circuit may be used for all A.C. tests except the high impedance test, where option 2 shall be used.
6. SW1 is a software switch.
7. Option 2 conditions are: $V_M = 5.0 \text{ V}$, $R_2 = 910\Omega \pm 5\%$, $R_3 = 320\Omega \pm 5\%$.
8. Option 1 conditions are: $R_1 = 2.8 \text{ k}\Omega \pm 1\%$.
9. Option 3 conditions are: $X_N = 1.311 \text{ V}$, $R_4 = 100\Omega \pm 5\%$, $R_5 = 117\Omega \pm 5\%$.

FIGURE 5. Switching time test circuit.

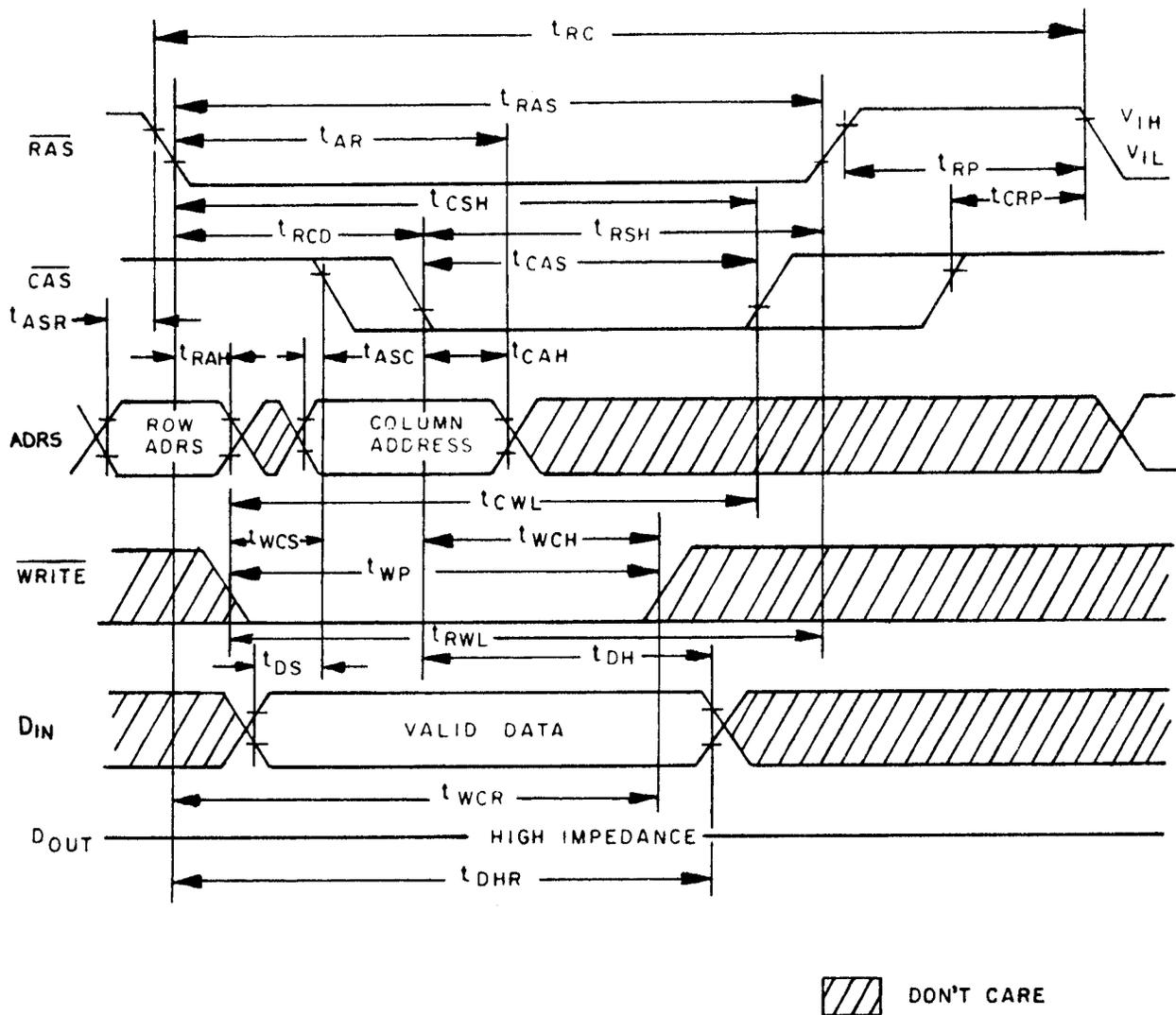


FIGURE 7. Write cycle waveforms.

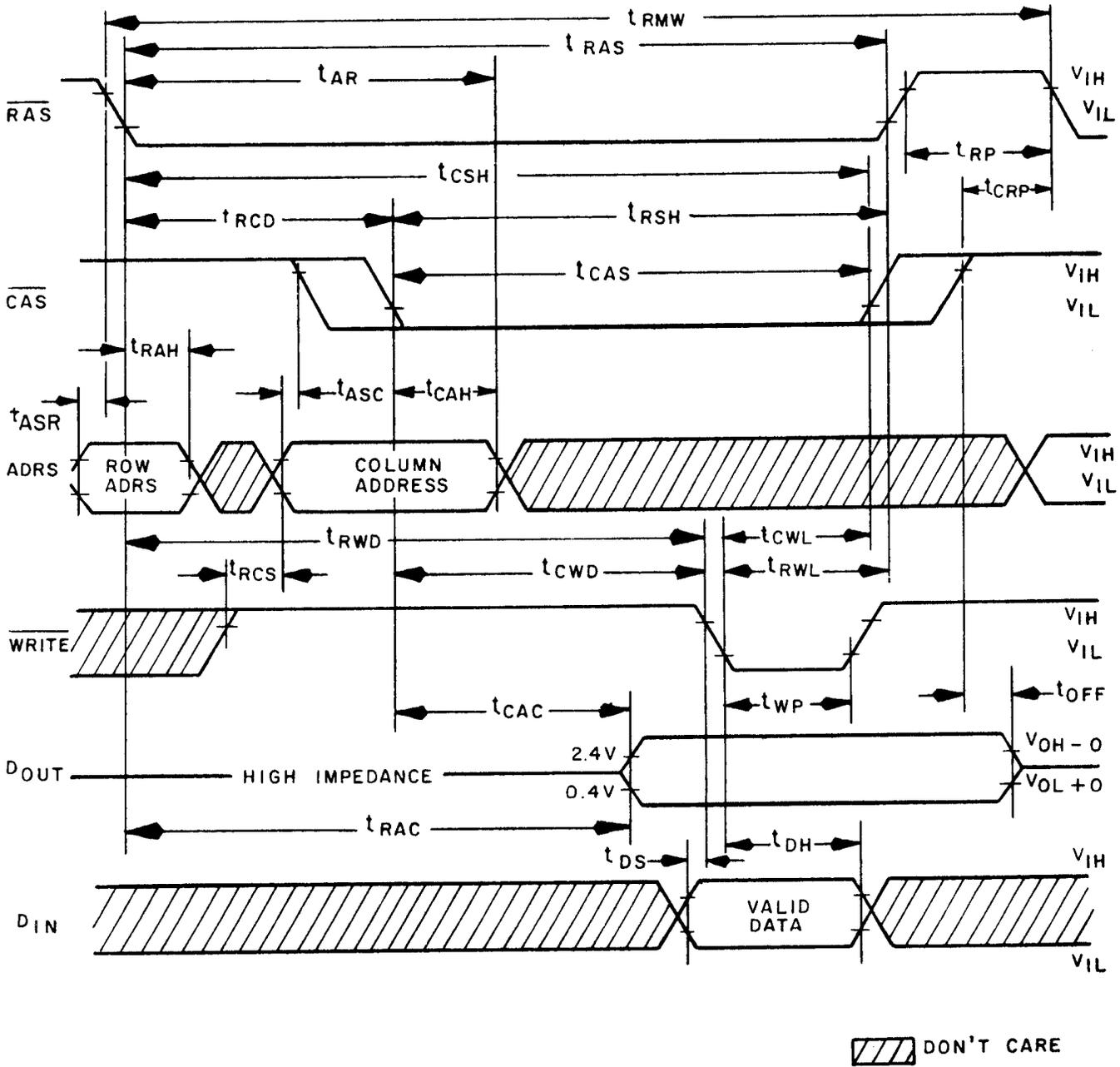


FIGURE 8. Read/write, read/modify/write cycle waveforms.

$\overline{\text{RAS}}$ ONLY REFRESH CYCLE

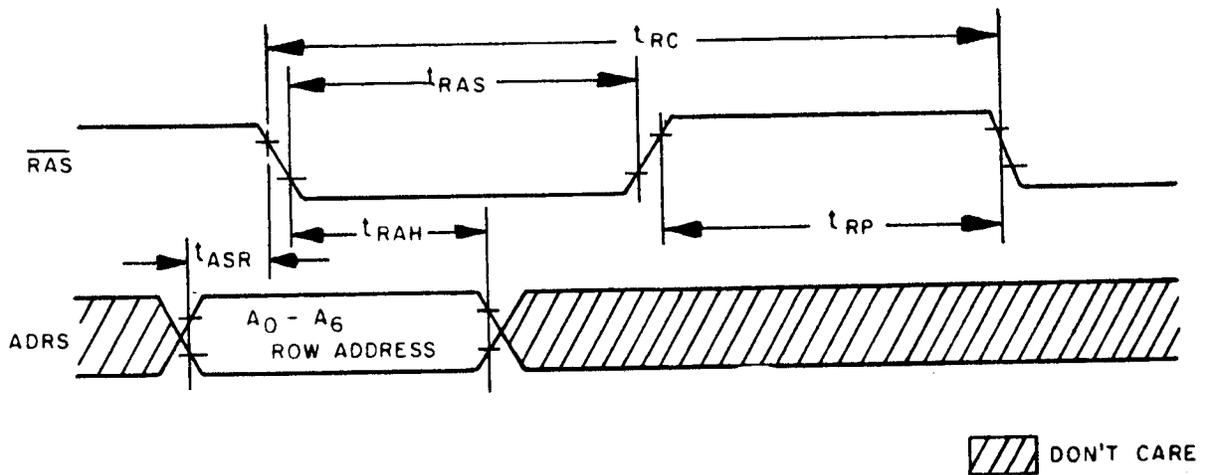
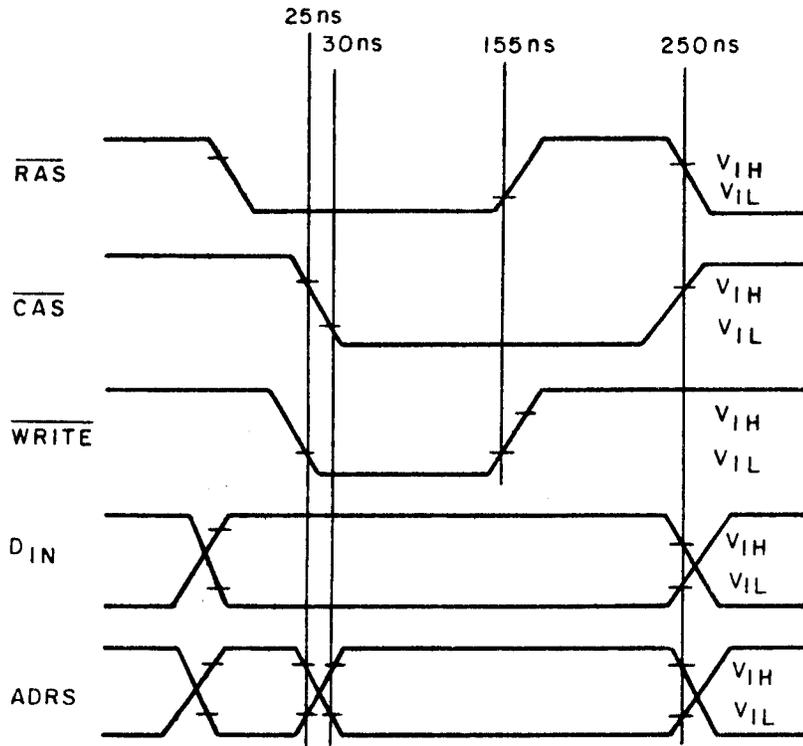
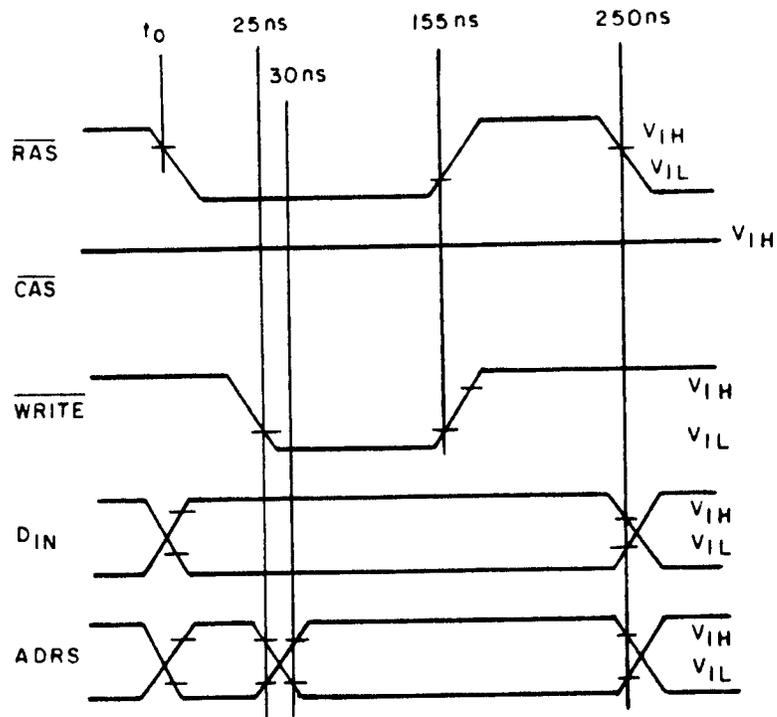


FIGURE 9. "RAS-ONLY" refresh cycle waveforms.



NOTE:
 $t_{\text{RISE}} = t_{\text{FALL}} = 5 \text{ ns max.}$
 $V_{\text{IL}} = 0.8 \text{ V.}$
 $V_{\text{IH}} = 2.4 \text{ V.}$

FIGURE 10. Timing waveforms for active current (I_{CCI}) measurements.



NOTE: $\overline{\text{CAS}} = V_{\text{IH}}$
 $t_{\text{RISE}} = t_{\text{FALL}} = 5 \text{ ns max.}$
 $V_{\text{IL}} = 0.8\text{V}$
 $V_{\text{IH}} = 2.4\text{V}$

FIGURE 11. Timing waveforms for refresh current (I_{CC3}) measurements.

TABLE III. Group A inspection for device types 01 and 02 - Continued.
Terminal conditions (pins not designated may be high >2.4 V, or low <0.45 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E																Measured terminal	Test limits			
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		17	18	Min	Max
			NC	D _{IN}	WRITE	RAS	A0	A2	A1	V _{CC}	A7	A5	A4	A3	A6	DOUT	CAS	V _{SS}					
4 T _C = 25°C	t _{CIN1}			9/	9/	9/	9/	9/	9/	5.0 V	9/	9/	9/	9/	9/	9/	9/	9/					5 pF
	t _{CIN2}			9/	9/	9/	9/	9/	9/	"	9/	9/	9/	9/	9/	9/	9/	9/					10 "
	t _{QOUT}			9/	9/	9/	9/	9/	9/	"	9/	9/	9/	9/	9/	9/	9/	9/					8 "
9 T _C = 25°C	t _{RAC}			10/	10/	10/	10/	10/	10/	5.0 V	10/	10/	10/	10/	10/	10/	10/	10/	10.0 V	Pat. 3	DOUT		150 ns
				11/	11/	11/	11/	11/	11/	4.5 V	11/	11/	11/	11/	11/	11/	11/	11/	"	Pat. 4	"		"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 5	"		"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 6	"		"
	t _{CAC}			12/	12/	12/	12/	12/	12/	"	12/	12/	12/	12/	12/	12/	12/	12/	Pat. 11	"		90 "	
	t _{RAC}			11/	11/	11/	11/	11/	11/	5.5 V	11/	11/	11/	11/	11/	11/	11/	11/	"	Pat. 4	"		150 "
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 5	"		"
				"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 6	"		"
	t _{CAC}			12/	12/	12/	12/	12/	12/	"	12/	12/	12/	12/	12/	12/	12/	12/	Pat. 11	"		90 "	
	t _{RAC}			13/	13/	13/	13/	13/	13/	4.5 V	13/	13/	13/	13/	13/	13/	13/	13/	"	Pat. 4	"		150 "
				14/	14/	14/	14/	14/	14/	5.5 V	14/	14/	14/	14/	14/	14/	14/	14/	"	Pat. 4	"		"
				14/	14/	14/	14/	14/	14/	4.5 V	14/	14/	14/	14/	14/	14/	14/	14/	"	Pat. 7	"		"
				15/	15/	15/	15/	15/	15/	"	15/	15/	15/	15/	15/	15/	15/	15/	"	Pat. 8	"		"
				15/	15/	15/	15/	15/	15/	"	15/	15/	15/	15/	15/	15/	15/	15/	"	Pat. 9	"		"
				14/	14/	14/	14/	14/	14/	"	14/	14/	14/	14/	14/	14/	14/	14/	"	Pat. 10	"		"
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = 110°C																						
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C, omit tests 49, 50, 51, 52																						

See footnotes at end of table.

TABLE III. Group A inspection for device type 03.
Terminal conditions (pins not designated may be high 2.4 V, or low 0.45 V, or open)

Subgroup	MIL-STD-883 method	Symbol	Case #																Measured terminal	Test limits		Unit
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		17	18	
	Test no.	NC	DIN	WRITE	RAS	A0	A2	A1	VCC	A7	A5	A4	A3	A6	DOUT	CAS	VSS		Min	Max		
1 Tc = 25°C	3009	I _{IL} (ad)	0.0 V	5.5 V	10.0 V	0.0 V	10.0 V	0.0 V	0.0 V	0.0 V	0.0 V	0.0 V	A0	-10	+10	μA						
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A2	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A7	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A5	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A4	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A3	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6	"	"	"	
2	3010	I _{IH} (ad)	6.5 V	"	16.5 V	0.0 V	10.0 V	6.5 V	6.5 V	"	6.5 V	"	A0	"	"	"						
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A2	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A1	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A7	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A5	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A4	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A3	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	A6	"	"	"	
3	3009	I _{IL} (DIN)	0.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	"	10.0 V	0.0 V	10.0 V	10.0 V	0.0 V	"	10.0 V	"	DIN	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	WRITE	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	RAS	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CAS	"	"	"	
	3010	I _{IH} (DIN)	6.5 V	16.5 V	16.5 V	16.5 V	16.5 V	16.5 V	"	16.5 V	6.5 V	16.5 V	16.5 V	6.5 V	"	16.5 V	"	DIN	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	WRITE	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	RAS	"	"	"	
	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	CAS	"	"	"	
4	3009	I _{IL} (PIN 1)	0.0 V	"	10.0 V	0.0 V	10.0 V	0.0 V	0.0 V	"	10.0 V	"	PIN 1	"	"	"						
	3010	I _{IH} (PIN 1)	6.5 V	"	16.5 V	6.5 V	16.5 V	6.5 V	6.5 V	"	16.5 V	"	PIN 1	"	"	"						
	3009	I _{OLZ} Z/	0.0 V	0.0 V	0.0 V	5.0 V	0.0 V	0.0 V	"	10.0 V	0.0 V	10.0 V	10.0 V	0.0 V	10.0 V	5.0 V	"	DOUT	"	"	"	
	3010	I _{OHZ} Z/	0.0 V	0.0 V	0.0 V	15.0 V	10.0 V	10.0 V	"	10.0 V	0.0 V	10.0 V	10.0 V	10.0 V	15.0 V	5.0 V	"	DOUT	"	"	"	
	3007	V _{OL}	3/	3/	3/	3/	3/	3/	4.5 V	3/	3/	3/	3/	3/	14.0 mA	3/	"	DOUT	---	0.4	V	
	3005	V _{OH}	3/	3/	3/	3/	3/	3/	4.5 V	3/	3/	3/	3/	3/	-5.0 mA	3/	"	DOUT	2.4	---	V	
	3005	I _{CC2}	0.0 V	2.4 V	2.4 V	10.0 V	10.0 V	10.0 V	5.5 V	10.0 V	0.0 V	10.0 V	10.0 V	10.0 V	10.0 V	10.0 V	2.4 V	"	VCC	---	10	mA
	3005	I _{CC1}	4/	4/	4/	4/	4/	4/	5.5 V	4/	4/	4/	4/	4/	4/	5/	"	VCC	---	60	mA	
5	3005	I _{CC3}	5/	6/	6/	6/	6/	5.5 V	6/	6/	6/	6/	6/	6/	5/	2.4 V	"	VCC	---	50	mA	
	3005	V _{0Z}	7/	7/	7/	7/	7/	4.5 V	7/	7/	7/	7/	7/	7/	7/	7/	"	DOUT	8/	8/	V	

Same tests, terminal conditions, and limits as for subgroup 1, except Tc = 110°C.

Same tests, terminal conditions, and limits as for subgroup 1, except Tc = -55°C.

See footnotes at end of table.

TABLE III. Group A inspection for device type 03 - Continued.
Terminal conditions (pins not designated may be high ≥ 2.4 V, or low < 0.45 V, or open)

Subgroup	Symbol	MIL-STD-883 method	Case E																Measured terminal	Test limits		Unit	
			1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16		Min	Max		
			Case 1	Case 2	Case 3	Case 4	Case 5	Case 6	Case 7	Case 8	Case 9	Case 10	Case 11	Case 12	Case 13	Case 14	Case 15	Case 16					
			NC	D _{IN}	WRITE	RAS	A ₀	A ₂	A ₁	V _{CC}	A ₇	A ₅	A ₄	A ₃	A ₆	D _{OUT}	CAS	V _{SS}					
4 T _C = 25°C	ICIN1	35	9/	9/	9/	9/	9/	9/	9/	5.0 V	9/	9/	9/	9/	9/	9/	9/	9/					
	ICIN2	36	9/	9/	9/	9/	9/	9/	9/	5.0 V	9/	9/	9/	9/	9/	9/	9/	9/					
	ICOUT	37	9/	9/	9/	9/	9/	9/	9/	5.0 V	9/	9/	9/	9/	9/	9/	9/	9/					
9 T _C = 25°C	t _{TRAC}	38	10/	10/	10/	10/	10/	10/	10/	5.0 V	10/	10/	10/	10/	10/	10/	10/	10/	Pat. 3	D _{OUT}	200	ns	
		39	11/	11/	11/	11/	11/	11/	11/	4.5 V	11/	11/	11/	11/	11/	11/	11/	11/	Pat. 4	"	"	"	
		40	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 5	"	"	"	
		41	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 6	"	"	"	
t _{CAC}		42	12/	12/	12/	12/	12/	12/	12/	"	12/	12/	12/	12/	12/	12/	12/	12/	Pat. 11	"	115	"	
		43	11/	11/	11/	11/	11/	11/	11/	5.5 V	11/	11/	11/	11/	11/	11/	11/	11/	Pat. 4	"	200	"	
t _{CAC}		44	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 5	"	"	"	
		45	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	"	Pat. 6	"	"	"	
t _{TRAC}		46	12/	12/	12/	12/	12/	12/	12/	"	12/	12/	12/	12/	12/	12/	12/	12/	Pat. 11	"	115	"	
		47	13/	13/	13/	13/	13/	13/	13/	4.5 V	13/	13/	13/	13/	13/	13/	13/	13/	Pat. 4	"	200	"	
		48	13/	13/	13/	13/	13/	13/	13/	5.5 V	13/	13/	13/	13/	13/	13/	13/	13/	Pat. 4	"	"	"	
		49	14/	14/	14/	14/	14/	14/	14/	4.5 V	14/	14/	14/	14/	14/	14/	14/	14/	Pat. 7	"	"	"	
		50	14/	14/	14/	14/	14/	14/	14/	"	14/	14/	14/	14/	14/	14/	14/	14/	Pat. 8	"	"	"	
		51	15/	15/	15/	15/	15/	15/	15/	"	15/	15/	15/	15/	15/	15/	15/	15/	Pat. 9	"	"	"	
		52	14/	14/	14/	14/	14/	14/	14/	"	14/	14/	14/	14/	14/	14/	14/	14/	Pat. 10	"	"	"	
10	Same tests, terminal conditions, and limits as for subgroup 9, except T _C = 110°C																						
11	Same tests, terminal conditions, and limits as for subgroup 10, except T _C = -55°C, omit tests 49, 50, 51, 52																						

1/ See the appendix for description of algorithms.

2/ Multiple toggles between 5.0 V and 0.0 V are applied to RAS and CAS; after toggling, RAS and CAS are at 5.0 V.

3/ These tests are listed but not tested. The output limits shall be set and used as conditions for dynamic go/no-go testing.

4/ All input levels and timing edges are set as shown on figure 10 or equivalent.

5/ Output loaded with one Standard Schottky TTL and 100 pF.

6/ All input levels and timing edges are set as shown on figure 11 or equivalent.

7/ All input levels and timing edges are set as shown in table IV - Timing Set no. 3 or equivalent.

8/ Using pattern no. 2, measure output voltage (tri-state voltage) to be greater than or equal to V_{OL} - 0.5 V after 40 ns (t_{OFF}) delay for a zero access; measure output voltage (tri-state voltage) to be less than or equal to V_{OH} - 0.5 V after 40 ns (t_{OFF}) delay for a one access.

9/ Capacitance measured with Boonton meter or effective capacitance calculated from the equation C = IΔE / ΔV with IΔE equal to 3 volts and V_{CC} = 5.0 V.

10/ All input levels and timing edges are set as shown in table IV - Timing Set no. 1 or equivalent.

11/ All input levels and timing edges are set as shown in table IV - Timing Sets no. 1, no. 2, no. 3, or equivalent.

12/ All input levels and timing edges are set as shown in table IV - timing Set no. 5 or equivalent.

13/ All timing edges are set as shown in table IV - Timing Set no. 4 or equivalent. Input levels are V_{IL} = -1.5 V, V_{IH} = 6.5 V.

14/ All timing edges are set as shown in table IV - Timing Set no. 4 or equivalent. Input levels are V_{IL} = 0.8 V, V_{IH} = 2.4 V.

15/ All input levels and timing edges are set as shown in table IV - Timing Set no. 6 or equivalent.

TABLE IVa. Recommended timing set designation for screening table I limits (device type 01 and 02).

Parameter		Spec limit (ns)	Timing set no. 1	Timing set no. 2	Timing set no. 3	Timing set no. 4 (nominal)	Timing set no. 5 (RMW)	Timing set no. 6 (extended)
Number	Symbol							
1a b	t _{RC} Min Max	250 10100	250* ---	250* ---	310 ---	320 ---	--- ---	--- 10100*
2a b	t _{R/W} Min Max	270 10100	--- ---	--- ---	--- ---	--- ---	270* ---	--- ---
3	t _{RAC} Max	150	150*	150*	210	150*	---	150*
4	t _{CAC} Max	85	---	85*	85*	90	85*	---
5	t _{RP} Min	90	90*	90*	90*	120	100	90*
6a b	t _{RAS} Min Max	150 10000	150* ---	150* ---	210 ---	180 ---	160 ---	--- 10000*
7	t _{RSH} Min	90	125	90*	90*	125	100	9975
8	t _{CSH} Min	150	240	150*	210*	280	160	10025
9a b	t _{CAS} Min Max	90 10000	220 ---	90* ---	125 ---	225 ---	100 ---	--- 10000*
10a b	t _{RCD} Min Max	25 60	25* ---	--- 60*	--- 120	--- 55	--- 60*	25* ---
11	t _{ASR} Min	0	0*	0*	0*	10	0*	0*
12	t _{RAH} Min	20	20*	55	120	30	55	20*
13	t _{ASC} Min	0	0*	0*	0*	5	0*	0*
14	t _{CAH} Min	30	55	30*	30*	75	30*	55
15	t _{AR} Min	80	80*	90	150	130	90	80*
16	t _{RCS} Min	0	0*	0*	0*	---	---	0*
17	t _{RCH} Min	0	0*	25	0*	---	---	0*
18	t _{WCH} Min	45	95	90	45*	85	NA	95

See footnotes at end of table.

TABLE IVa. Recommended timing set designation for screening table I limits
(device type 01 and 02) - Continued.

Parameter		Spec limit (ns)	Timing set no. 1	Timing set no. 2	Timing set no. 3	Timing set no. 4 (nominal)	Timing set no. 5 (RMW)	Timing set no. 6 (extended)
Number	Symbol							
19	t_{WCR} Min	120	120*	150	165	140	160	120*
20	t_{WP} Min	45	100	45*	50	100	45*	100
21	t_{RWL} Min	45	130	45*	95	125	45*	9980
22	t_{CWL} Min	45	220	45*	125	240	45*	10005
23a	$t_{DS(CAS)}$ Min	0	0*	---	0*	10	---	0*
b	$t_{DS(WE)}$ Min	0	---	0*	---	---	0*	---
24a	$t_{DH(CAS)}$ Min	45	95	---	45*	85	---	95
b	$t_{DH(WE)}$ Min	45	---	45*	---	---	45*	---
25	t_{DHR} Min	120	120*	140	165	140	160	120*
26	t_{WCS} Min	0	0*	0*	0*	10	NA	0*
27	t_{CRP} Min	0	0*	90	60	20	100	65
28	t_{RRH} Min	25	90	25*	30	---	---	25*
29	t_{CWD} Min	50	NA	NA	NA	NA	50*	NA
30	t_{RWD} Min	110	NA	NA	NA	NA	110*	NA

NOTES: * Indicates parameter being tested at specification limit
NA - Not applicable

Timing set no. 1, no. 2, no. 3, no. 5, no. 6 - Use V_{IH} min (2.4 V) and V_{IL} max (0.8 V) and $t_{TRANSITION} = 5$ ns

Timing set no. 4 - Nominal timing; will not violate limits if V_{IH} max (6.5 V) and V_{IL} min (-1.5 V) and $t_{TRANSITION} = 10$ ns are used.

TABLE IVb. Recommended timing set designation for screening table I limits (device type 03).

Parameter		Spec limit (ns)	Timing set no. 1	Timing set no. 2	Timing set no. 3	Timing set no. 4 (nominal)	Timing set no. 5 (RMW)	Timing set no. 6 (extended)
Number	Symbol							
1a b	t _{RC} Min Max	345 10,145	345* ---	345* ---	405 ---	405 ---	--- ---	--- 10,145
2a b	t _{R/W} Min Max	370 10,145	--- ---	--- ---	--- ---	--- ---	370* ---	--- ---
3	t _{RAC} Max	200	200*	200*	270	200*	---	200*
4	t _{CAC} Max	115	---	115*	115*	120	115*	---
5	t _{RP} Min	135	135*	140	135*	200	155	135*
6a b	t _{RAS} Min Max	200 10,000	200* ---	200* ---	270 ---	240 ---	210 ---	--- 10,000
7	t _{RS} Min	115	165	115*	115*	165	125	10,035
8	t _{CS} Min	200	335	200	320	370	210	10,035
9a b	t _{CAS} Min Max	115 10,000	305 ---	115* ---	150 ---	295 ---	130 ---	--- 10,000*
10a b	t _{RCD} Min Max	35 80	35* ---	--- 80*	--- 150	--- 75	--- 80*	35* ---
11	t _{ASR} Min	0	0*	0*	0*	10	0*	0*
12	t _{RAH} Min	25	25*	65	150	40	60	25*
13	t _{ASC} Min	0	0*	0*	0*	5	0*	0*
14	t _{CAH} Min	40	75	40*	40*	85	40*	75
15	t _{AR} Min	110	110*	120	190	170	120	110*
16	t _{RCS} Min	0	0*	0*	0*	---	---	0*
17	t _{RCH} Min	0	0*	25	0*	---	---	0*
18	t _{WCH} Min	55	115	55*	55*	105	NA	115

See footnotes at end of table.

TABLE IVb. Recommended timing set designation for screening table I limits
(device type 03) - Continued.

Parameter		Spec limit (ns)	Timing set no. 1	Timing set no. 2	Timing set no. 3	Timing set no. 4 (nominal)	Timing set no. 5 (RMW)	Timing set no. 6 (extended)
Number	Symbol							
19	t_{WCR} Min	150	150*	150*	200	180	210	150*
20	t_{WP} Min	55	120	55*	55*	115	55*	120
21	t_{RWL} Min	55	170	120	115	175	55*	9970
22	t_{CWL} Min	55	300	120	155	300	55*	10,005
23a	$t_{DS}(\overline{CAS})$ Min	0	0*	---	0*	10	---	0*
b	$t_{DS}(\overline{WE})$ Min	0	---	0*	---	---	0*	---
24a	$t_{DH}(\overline{CAS})$ Min	55	120	---	55*	105	---	115
b	$t_{DH}(\overline{WE})$ Min	55	---	55*	---	---	55*	---
25	t_{DHR} Min	150	150*	140	200	180	215	150*
26	t_{WCS} Min	0	0*	0*	0*	10	NA	0*
27	t_{CRP} Min	0	0*	140	95	75	160	100
28	t_{RRH} Min	30	NA	30*	NA	---	---	NA
29	t_{CWD} Min	80	NA	NA	NA	NA	80*	NA
30	t_{RWD} Min	160	NA	NA	NA	NA	160*	NA

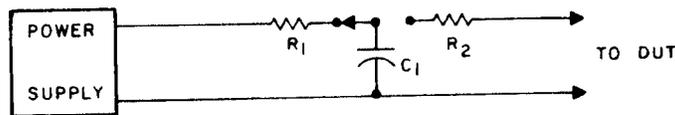
NOTES: * Indicates parameter being tested at specification limit
NA - Not applicable

Timing set no. 1, no. 2, no. 3, no. 5, no. 6 - Use V_{IH} min (2.4 V) and
 V_{IL} max (0.8 V) and $t_{TRANSITION} = 5$ ns

Timing set no. 4 - Nominal timing; will not violate limits if V_{IH} max (6.5 V)
and V_{IL} min (-1.5 V) and $t_{TRANSITION} = 10$ ns are used.

4.5.3 High voltage (V_{zap}) test of input protection circuits. One input terminal of the device under test (DUT) shall be subjected to a voltage pulse of 150 volts from a 100 picofarad source in the following test sequence:

- a. Measure I_{IH} and I_{IL} at one input terminal of the DUT at 25°C. Also measure I_{CC} at 25°C. These measurements shall be made in accordance with table III herein. The test limits for a single terminal measurement of I_{IH} and I_{IL} shall be ± 10 microamperes, maximum.
- b. In the circuit below, charge the capacitor to -150 volts. Then, using the same terminal of the device as selected above for leakage measurements, switch the capacitor to discharge into the device terminal. Then repeat the procedure with +150 volts.
- c. Within 24 hours, repeat the I_{CC} , I_{IH} , and I_{IL} measurements on the same terminal as performed above. At this time a DUT exhibiting leakage currents in excess of the specified limits is defective.



R_1 = Appropriate current limiting resistance

R_2 = 1.5 k Ω $\pm 5\%$.

C_1 = 100 pF $\pm 20\%$

Power supply voltage = V_{zap} = +150 Vdc and -150 Vdc

DUT pin 16 (V_{SS}) shall be ground potential during stress.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The acquisition document should specify the following:

- a. Complete part number (see 1.2).
- b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.
- c. Requirement for certificate of compliance, if applicable.
- d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action and reporting of results, if applicable.

- f. Requirements for product assurance options.
- g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.
- h. Requirement for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-STD-1331, and as follows:

VCC	- - - - -	Supply voltage
VSS	- - - - -	Common or reference voltage mode
RAS	- - - - -	Row address strobe, input
CAS	- - - - -	Column address strobe, input
WRITE or WR	- - - - -	Read or write input
DIN	- - - - -	Data-input
DOUT	- - - - -	Data-output
A ₀ through A ₇ , ADDR, or ADRS	- - - - -	Address input
LSB	- - - - -	Least significant address bit
MSB	- - - - -	Most significant address bit
Pattern 1 through 10	- - - - -	Test pattern algorithms
NC	- - - - -	No connect
TS no.	- - - - -	Timing set number

6.4 Application and operation guidelines.

6.4.1 Initialization. The device requires a 100 μ s pause and eight pump cycles after power up before it will operate properly. Any cycle that performs refresh may be used for a pump cycle.

6.4.2 Addressing. Addressing 1 of 65,536 (2^{16}) cells requires handling a 16-bit address word. This is accomplished with minimum pin count by multiplexing two 8-bit address fields onto the eight address inputs (A₀-A₇). The two fields are brought on chip in succession by the high to low transition of the row address and column (RAS, CAS) strobes which activate internal timing generators and latch the address information on chip for decoding.

6.4.3 Read operation. When a valid row address is presented to the address inputs, the row address strobe (RAS) can fall and thereby clock the row address into the address latches. After a row address hold time (t_{RAH}), the column address can be presented to the device and the column address strobe (CAS) can fall to latch the column address onto the chip. The WRITE input is held at a logic "1" (high) level. The output is in the high impedance state and will remain in that state until access time. At access time it will turn on and assume the appropriate level ("1" to "0"). A feature referred to as "Gated CAS" is simply a delayed internal signal that is gated with the external CAS signal which causes the on chip CAS clock to occur at a fixed interval after RAS. This allows CAS to become active (low) any time after row address hold time (t_{RAH}) has been satisfied but before the maximum RAS to CAS delay time (t_{RCD}) without affecting access time referenced to RAS (t_{RAC}). CAS can occur later than t_{RCD} maximum without affecting device operation but access time will be controlled exclusively by CAS which is access time referenced to CAS (t_{CAC}).

6.4.4 Write operation. The same procedure applies for latching the address information on chip that was explained for the read operation. Data can be written into the device in several ways. In all cases, however, writing is accomplished by the falling edge of CAS or WRITE (while RAS is low) whichever occurs latest. Data is latched onto the chip.

- a. Early write - Data in and WRITE precede the fall of CAS by a set-up time (t_{DS} and t_{WCS} , respectively) and remain valid for a hold time (t_{DH} and t_{WCH}). The setup and hold times are with respect to the falling edge of CAS. Data out remains in the high impedance state for the entire cycle.

- b. Late write - The fall of WRITE occurs after data in and CAS by a specified time (CAS to WRITE delay t_{cwp}). Data in set-up and hold times are referenced to the fall of WRITE. Data out will contain data from the selected cell at access time. If the fall of WRITE occurs prior to the CAS to WRITE delay limit, the state of the data out pin is indeterminate.

6.4.5 Refresh operations. The basic device constraint is that no cell shall be refreshed at intervals exceeding 1.0 milliseconds. There are 256 cells along each row in the storage matrix and there are 256 such rows. A normal read or refresh cycle refreshes 256 cells in two rows simultaneously. A row address 128 cycle "burst" every millisecond or a single distributed cycle every 7.812 microseconds at each of the first 128 row addresses (i.e., A_0 - A_6 ; A_7 is a don't care) will accomplish complete memory refreshing. A refresh cycle can be accomplished in two ways. Either a normal read cycle or a "RAS only" cycle will accomplish refresh. The RAS only refresh requires less power than a standard RAS/CAS cycle.

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer lead lengths and lead forming shall not affect the part number.

6.6 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

<u>Military device type</u>	<u>Generic industry type</u>	<u>Access time</u>	<u>Refresh</u>
01	6665, 4564, 2164, 8264	150 ns	1 ms
02	6665, 4564, 2164, 8264	150 ns	2 ms
03	6665, 4564, 2164, 8264	200 ns	2 ms

6.7 Handling. MOS devices must be handled with certain precautions to avoid damage due to the accumulation of static charge. Input protection circuitry has been designed into the device to minimize the effect of this static buildup. However, the following handling practices are recommended.

- Devices should be handled on benches with conductive and grounded surfaces.
- Ground test equipment and tools.
- Do not handle devices by the leads.
- Store devices in conductive foam or carriers.
- Avoid the use of plastic, rubber, or silk in MOS areas.
- Maintain relative humidity above 50 percent, if practical.

6.8 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue, due to the extensiveness of the changes.

Custodian:

Air Force - 17

Review activities:

Air Force - 11, 19, 85, 99
DLA - ES

Agent:

DLA - ES

Preparing activity:

Air Force - 17

(Project 5962-F665)

APPENDIX

FUNCTIONAL ALGORITHMS AND TIMING SETS

Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion.

Timing sets are displayed in table IV. Note that multiple passes through the memory are required to screen table I limits. The timing conditions and input levels shown in table IV are recommended and will properly screen table I limits. Equivalent timing sets may be used that serve the same purpose; however, each manufacturer must demonstrate that this condition will be met.

NOTE: Step 1 of all algorithms may be performed initially and if testing is continuous (no dead time exceeding 5 ms between tests), step 1 does not have to be repeated for each algorithm.

PATTERN 1CONTINUOUS READ, DATA BACKGROUND = X-BAR

This pattern is used to allow the maximum amount of current I_{CC} to be drawn from the V_{CC} power supply. It is performed in the following manner with normal cycle timing:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with background data
- Step 3 - Sequentially read entire memory
- Step 4 - Repeat step 3 as many times as necessary to achieve a reading

Test time - Undefined

PATTERN 2OUTPUT HIGH IMPEDANCE (t_{off})

This pattern verifies the output buffer switches to high impedance (tri-state) within the specified 30 ns after the rise of \overline{CAS} . It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load minimum address location with "0"
- Step 3 - Read minimum address location and measure V_{OL}
- Step 4 - Raise \overline{CAS} and measure $V_{OUT} \geq V_{OL} + 0.5$ V after 30 ns delay
- Step 5 - Load minimum address location with "1"
- Step 6 - Read minimum address location and measure V_{OH}
- Step 7 - Raise \overline{CAS} and measure $V_{OUT} \leq V_{OH} - 0.5$ V after 30 ns delay

Test time = 12 x cycle time

PATTERN 3 V_{BUMP}/V_{BOGGLE} DATA BACKGROUND = ALL "0" (discharged state)

This pattern indicates sense amplifier margin by slewing the supply voltage between memory writing and reading. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Pause 600 μ s ramping V_{CC} to 4.5 V inhibiting all clocks
- Step 3 - Load memory with background data
- Step 4 - Pause 600 μ s ramping V_{CC} to 5.5 V inhibiting all clocks
- Step 5 - Read memory with background data
- Step 6 - Repeat steps 2 through 5 for background data complement

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- Step 7 - Load memory with background data
- Step 8 - Pause 600 μ s ramping V_{CC} to 4.5 V inhibiting all clocks
- Step 9 - Read memory with background data
- Step 10 - Pause 600 μ s ramping V_{CC} to 5.5 V inhibiting all clocks
- Step 11 - Repeat steps 7 through 9 for background data complement

Test time = $(8N + 8) \times \text{cycle time} + 280 \mu\text{s}$

PATTERN 4

ADDRESS COMPLEMENT, DATA BACKGROUND = ALL "0"

This pattern produces maximum address line noise and checks the decoder dynamic response times. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with background data
- Step 3 - Read minimum address location
- Step 4 - Load minimum address location with "1"
- Step 5 - Read maximum address location
- Step 6 - Load maximum address location with "1"
- Step 7 - Read minimum address location + 1
- Step 8 - Load minimum address location +1 with "1"
- Step 9 - Read maximum address location -1
- Step 10 - Load maximum address location -1 with "1"
- Step 11 - Repeat steps 3 through 10 until all address locations have been read and loaded with "1"s.
- Step 12 - Repeat steps 3 through 11 reading "1"s and loading "0"s.
- Step 13 - Read memory, all "0"s

Test time = $(6N + 8) \times \text{cycle time}$

PATTERN 5

MARCHING COLUMNS, INITIAL DATA BACKGROUND = ALL "0"

This pattern is a good test for sense line imbalance and response plus restore noise in addition to multiple selection. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with data background
- Step 3 - Write test column complement
- Step 4 - Read test column complement
- Step 5 - Write test columns true
- Step 6 - Repeat 3 through 6 for all columns sequentially
- Step 7 - Write background data to "1"
- Step 8 - Write test column complement
- Step 9 - Read test column complement
- Step 10 - Write test columns true
- Step 11 - Repeat 8 through 10 for all columns sequentially

Test time = $(512N + 8) \times \text{cycle time}$

PATTERN 6

MARCH DATA, DATA BACKGROUND = ALL "0"

This pattern tests for address uniqueness and multiple selection. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with background data
- Step 3 - Read location 0
- Step 4 - Write data complement in location 0
- Step 5 - Read data complement in location 0

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- Step 6 - Repeat steps 3 through 5 for all other locations in memory (sequentially)
- Step 7 - Read data complement at maximum location
- Step 8 - Write data at maximum location
- Step 9 - Read data at maximum location
- Step 10 - Repeat steps 7 through 9 for all other locations in the memory (sequentially)
- Step 11 - Repeat steps 2 through 10 with data background of all "1"

Test time = $(14N + 8) \times \text{cycle time}$

PATTERN 7STATIC REFRESH (PERIPHERY RETENTION)

This pattern tests for periphery retention time by attempting to write after a lengthy pause. This test is performed at 110°C (case) only, and is not used to measure the retention time of the periphery circuits, but to insure that they will hold for at least 5 ms. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with all "0"s
- Step 3 - Read memory, all "0"s
- Step 4 - Pause (stop all clocks) 2 ms
- Step 5 - Load memory with all "1"s
- Step 6 - Read memory, all "1"s
- Step 7 - Pause (stop all clocks) 2 ms
- Step 8 - Load memory with all "0"s
- Step 9 - Read memory, all "0"s

Test time = $(6N + 8) \times \text{cycle time} + 10 \text{ ms}$

PATTERN 8REFRESH TEST (CELL RETENTION)

This test is used to check the retention time of memory cells under static and dynamic conditions. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with all "0"s
- Step 3 - Pause 1 ms (stop all clocks)
- Step 4 - Read memory, all "0"s
- Step 5 - Repeat steps 2 through 4 with all "1"s
- Step 6 - Read minimum address location
- Step 7 - Read maximum address location
- Step 8 - Repeat steps 6 and 7 for 1 ms
- Step 9 - Read memory, all "1"s
- Step 10 - Load memory, all "0"s
- Step 11 - Repeat steps 6 through 9 with all "0"s
- Step 12 - Read address location 32767
- Step 13 - Read address location 32768
- Step 14 - Repeat steps 12 and 13 for 1 ms
- Step 15 - Read memory, all "0"s
- Step 16 - Load memory, all "1"s
- Step 17 - Repeat steps 12 through 15 with all "1"s

Test time = $(10N + 8) \times \text{cycle time} + 6 \text{ ms}$

PATTERN 9EXTENDED CYCLE TEST (10 μs), DATA BACKGROUND = X-BAR

This test is used to verify the 10 μs maximum limit on $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ pulse widths. Front and back edge timing is held to normal cycle timing while the cycle is increased to allow 10 μs of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ active time (low level). It is performed in the following manner:

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- Step 1 - Perform 8 pump cycles
- Step 2 - Write data in location 0
- Step 3 - Read data in location 0
- Step 4 - Repeat steps 2 and 3 for all other locations in the memory (sequentially)
- Step 5 - Repeat steps 2 through 4 with complement data

Test time = $(4N + 8) \times \text{cycle time}$

PATTERN 10RAS-ONLY/REFRESH TEST

This test is used to verify the functionality of the $\overline{\text{RAS}}$ -only mode of cell refreshing. It is done at high temperature only and is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with all "0"s
- Step 3 - Perform 128 $\overline{\text{RAS}}$ -only cycles ($\overline{\text{CAS}} = \overline{\text{WE}} = "1"$)
- Step 4 - Repeat step 3 for 0.5 second
- Step 5 - Read memory, all "0"s
- Step 6 - Repeat step 2 through 5 with all "1"s

Test time = $(4N + 8) \times \text{cycle time} + 1 \text{ second}$

PATTERN 11READ-MODIFY-WRITE (RMW), DATA BACKGROUND = ALL "0"

This pattern verifies the Read-Modify-Write mode for the memory. It is performed in the following manner:

- Step 1 - Perform 8 pump cycles
- Step 2 - Load memory with background data
- Step 3 - Read minimum address location and load with "1" using RMW cycle
- Step 4 - Read maximum address location and load with "1" using RMW cycle
- Step 5 - Read minimum address location + 1 and load with "1" using RMW cycle
- Step 6 - Read maximum address location - 1 and load with "1" using RMW cycle
- Step 7 - Repeat steps 3 through 6 until all address locations have been read and loaded with "1"
- Step 8 - Repeat steps 3 through 7 reading "1"s and loading "0"s
- step 9 - Read memory, all "0"s

Test time = $(2N + 8) \times \text{read or write cycle time} + (2N) \times \text{read-modify-write cycle time}$