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28 February 1986
SUPERSEDING
MIL-M-38510/127
8 February 1982

MILITARY SPECIFICATION

MICROCIRCUITS, LINEAR, CMOS MULTIPLYING D/A CONVERTERS, MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS multiplying D/A converters. Two product assurance classes and a choice of case outlines and lead finishes are provided for each type and are reflected in the complete part number.

1.2 Part number. The part number shall be in accordance with MIL-M-38510.

1.2.1 Device type. The device type shall be as follows:

Device type	Multiplying D/A converter circuit with:
01	8-bit resolution, 8-bit end-point linearity
02, 05	10-bit resolution, 10-bit end-point linearity
03, 06	12-bit resolution, 10-bit end-point linearity
04, 07	12-bit resolution, 12-bit end-point linearity

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outline. The case outline shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
E	D-2 (16-lead, 1/4" x 7/8") dual-in-line package
V	D-6 (18-lead, 1/4" x 15/16") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage (V_{DD})	+17 V
Reference input voltage (V_{REF})	±25 V
Digital input voltage (V_{IN})	V_{DD} to ground
Output voltage (V_{OUT})	-100 mV to V_{DD}
Lead temperature (soldering, 60 seconds)	300°C
Storage temperature	-65° to +150°C
Junction temperature (T_J)	175°C
Maximum power dissipation	450 mW up to 75°C
Derating factor above 75°C	6 mW/°C

1.4 Recommended operating conditions.

Supply voltage	+15 V 1/
Reference voltage range	-10 V to +10 V 2/
Output compliance voltage	0 V 3/
Ambient operating temperature range	-55° to +125°C

1/ Linearity is guaranteed only at V_{DD} = +15 V. Linearity will degrade at lower supply voltages.
2/ Linearity is guaranteed only at V_{REF} = ±10 V. Linearity errors become more apparent as the magnitude of V_{REF} is decreased toward 0 V.
3/ All linearity testing is done at I_{OUT1} using the internal feedback resistor with I_{OUT2} grounded.

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center (RBE-2), Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

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1.5 Power and thermal characteristics.

Package	Case outline	Maximum allowable power dissipation	Maximum θ_{J-C}	Maximum θ_{J-A}
16-lead dual-in-line	E	400 mW at T_A = 125°C	35°C/W	120°C/W
18-lead dual-in-line	V	400 mW at T_A = 125°C	35°C/W	120°C/W

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specification and standard. The following specification and standard, form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents shall be those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this specification and the references cited herein (except for associated detail specifications, specification sheets or MS standards), the text of this specification shall take precedence. Nothing in this specification, however, shall supersede applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specification. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510, and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Schematic circuit. The schematic circuit shall be submitted to the preparing activity prior to inclusion of manufacturer's device in this specification and shall be submitted to the qualifying activity and agent activity (DESC-ECS) as a prerequisite for qualification. All qualified manufacturer's schematics shall be maintained by the agent activity and will be available upon request. The schematic circuit shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be as specified in 1.2.3 herein.

3.2.4 Functional diagram and CMOS switch schematic. The functional diagram and CMOS switch schematic shall be as specified on figure 3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. *The electrical performance characteristics of table I* apply over the full recommended ambient operating temperature range, unless otherwise specified. *Also, IOUT1 and IOUT2 are at actual ground or virtual ground.* (See figure 3.) The R-2R resistor network has Johnson or thermal noise. Noise at the device under test (DUT) outut is related to the noise resistance value according to $en = \sqrt{(4KTRn(BW))}$.

Where:

K = Boltzmann's constant (1.38×10^{-23} joules per kelvin).
T = Absolute temperature (in kelvin).
Rn = RoRf/(Ro+Rf) changes with Ro and the digital code word.
BW = Bandwidth (in hertz).

TABLE I. Electrical performance characteristics.

Characteristic	Symbol	Conditions (See 3.4 and figure 6; all digital inputs at V_{DD} = +15 V; V_{REF} = +10 V, unless otherwise specified)		Device type	Limits Min	Limits Max	Unit
Supply current from V_{DD}	I_{DD}	V_{IL} = 0 V, and V_{IH} = V_{DD}	25°C < T_A < 125°C	01-04	---	100	µA
				05-07	---	2.0	mA
			T_A = -55°C	All	---	2.5	mA
		V_{IL} = 0.8 V, and V_{IH} = 2.4 V	25°C < T_A < 125°C	All	---	2.0	mA
			T_A = -55°C	All	---	2.5	mA
Reference input current	I_{REF}	V_{IH} = V_{DD}	V_{REF} = +10 V	All	0.5	2.0	mA
			V_{REF} = -10 V	All	-2.0	-0.5	mA
Digital input leakage current	I_{IL}	V_{IL} = 0 V		01-04	-1.0	1.0	µA
		V_{IL} = 0.8 V and V_{IL} = 0 V		05-07	-200	1.0	µA
	I_{IH}	V_{IH} = V_{DD}		01-04	-1.0	1.0	µA
		V_{IH} = 2.4 V and V_{IH} = V_{DD}		05-07	-1.0	100	µA
Zero-scale current	I_{ZS}	V_{IL} = 0.8 V	Measured at I_{OUT1}	01-03	-100	100	nA
				04,07	-50	50	nA
				05,06	-100	100	nA
	$I_{ZS'}$	V_{IH} = 2.4 V	Measured at I_{OUT2}	01-03	-100	100	nA
				04,07	-50	50	nA
				05,06	-100	100	nA
Full-scale error	$+d_{VFS}$	V_{IH} = V_{DD}	V_{REF} = +10 V	01	-1.5	1.5	%VFS
				02,05	-1.0	1.0	%VFS
				03,04	-0.4	0.4	%VFS
				06,07	-0.4	0.4	%VFS
	$-d_{VFS}$	V_{IH} = V_{DD}	V_{REF} = -10 V	01	-1.5	1.5	%VFS
				02,05	-1.0	1.0	%VFS
				03,04	-0.4	0.4	%VFS
				06,07	-0.4	0.4	%VFS

TABLE I. Electrical performance characteristics - Continued.

Characteristic	Symbol	Conditions (See 3.4 and figure 6; all digital inputs at V_{DD} = +15 V; V_{REF} = +10 V, unless otherwise specified)	Device type	Limits Min	Limits Max	Unit
Full-scale error drift	d_{VFS}/dt	Change in $+d_{VFS}$ from 25°C to 125°C and from 25°C to -55°C.	All	-10	10	ppm VFS/°C
Power supply sensitivity at full scale from V_{DD}	+PSS, -PSS	Change in $+d_{VFS}$ from V_{DD} at 15 V to V_{DD} at 16 V and 14 V, respectively.	01-04	-130	130	ppm VFS/V
			05-07	-20	20	ppm VFS/V
Linearity error (end-point)	LE	$V_{IH} = V_{DD}$, V_{IL} = 0 V 1/	01	-0.2	0.2	%VFS
			02,03, 05,06	-.05	.05	%VFS
			04,07	-.012	.012	%VFS
Major carry errors (differential linearity)	MCE	$V_{IH} = V_{DD}$, V_{IL} = 0 V The difference between adjacent codes at all major transitions (i.e., 01111111 to 10000000)	01	-0.4	0.4	%VFS
			02,03, 05,06	-0.1	0.1	%VFS
			04,07	-.025	.025	%VFS
Feedthrough error	FTE	V_{IL} = 0 V; V_{REF} = 20 Vpp at 100 kHz; group D only. T_A = 25°C. See figure 7.	01-04	---	10	mVpp
			05-07	---	25	mVpp
Output current settling time (to 1/2 LSB)	t_{SLH}	All inputs switched simultaneously, low to high and high to low. T_A = 25°C. See figure 8. 2/	All	---	1	µs
	t_{SHL}		All	---	1	µs
Output capacitance	C_o	All digital inputs at V_{DD}. T_A = 25°C. See figure 9. — C_o at I_{OUT1}	01-04	---	200	pF
			05-07	---	300	pF
		C_o at I_{OUT2}	01-04	---	75	pF
			05-07	---	100	pF
		All digital inputs at 0 V. T_A = 25°C. See figure 9. — C_o at I_{OUT1}	01-04	---	75	pF
			05-07	---	100	pF
		C_o at I_{OUT2}	01-04	---	200	pF
			05-07	---	300	pF

1/ Linearity is specified to be within ±1/2 LSB. Thus an 8-bit device with a 10 V reference must have end-point linearity to within 1/2 of $(100\%VFS/2^8)$ = 0.195 %VFS or 0.2 %VFS.

2/ For each device type, output current settling time is the duration from the digital input transition until the output for a 10 V analog input transition is within 1/2 LSB of final value.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table III.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein.

3.6.1 Serialization. All class S devices shall be serialized in accordance with MIL-M-38510.

3.6.2 Correctness of indexing and markings. All devices shall be subjected to the final electrical tests specified in table II after part marking to verify that they are correctly indexed and identified by part number. Optionally, an approved electrical test may be devised especially for this requirement.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 80 (see MIL-M-38510, appendix E).

TABLE II. Electrical test requirements.

MIL-STD-883 test requirement	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1	1
Final electrical test parameters (method 5004)	1*,2,3	1*,2,3
Group A test requirements (method 5005)	1,2,3,7,8,12	1,2,3,7,8,12
Group C end-point and group B, class S, electrical parameters (method 5005)	1,2,3, and table IV delta limits	1 and table IV delta limits
Additional electrical subgroup for group C periodic inspection	N/A	---
Group D end-point electrical parameters (method 5005)	1,2,3	1
Additional electrical subgroup for group D periodic inspection	N/A	---

*PDA applies to subgroup 1 (see 4.2c).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-M-38510 and methods 5005 and 5007, as applicable, of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply:

a. Burn-in tests (method 1015 of MIL-STD-883).

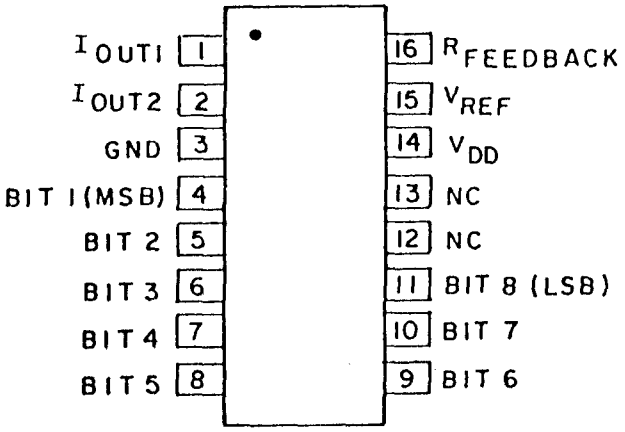
(1) Class S devices - Dynamic tests (test condition D or E) using the circuit shown on figure 4; test duration shall be 240 hours minimum. Static tests (test condition A) using the circuit shown on figure 5; test duration shall be 48 hours minimum.

(2) Class B devices - Test condition A using the circuit shown on figure 5; or test condition D using the circuit shown on figure 4.

b. Interim and final electrical test parameters shall be as specified in table II, except interim electrical parameters test prior to burn-in is optional at the discretion of the manufacturer.

Device type 01

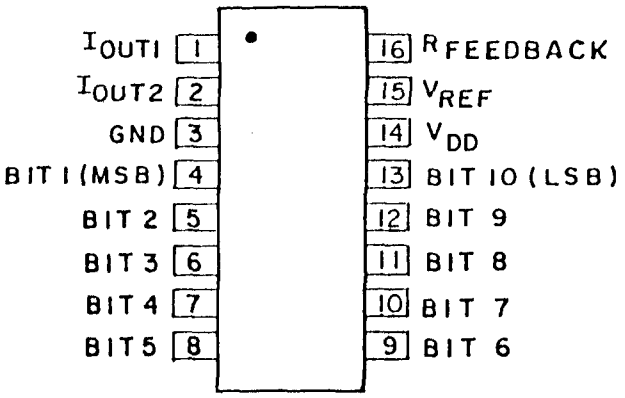
Case E



16 lead
dual-in-line
(top view)

Device types 02 and 05

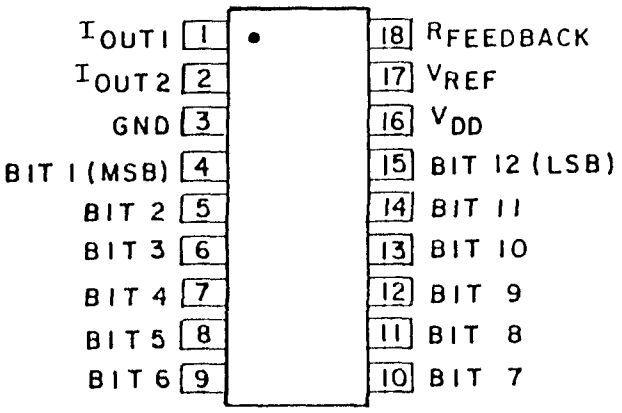
Case E



16 lead
dual-in-line
(top view)

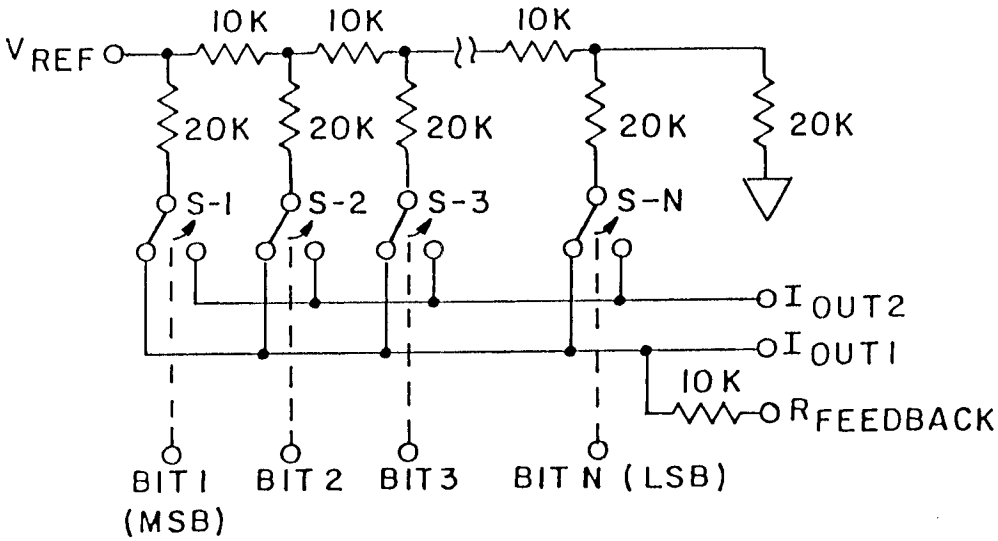
Device types 03, 04, 06, and 07

Case V



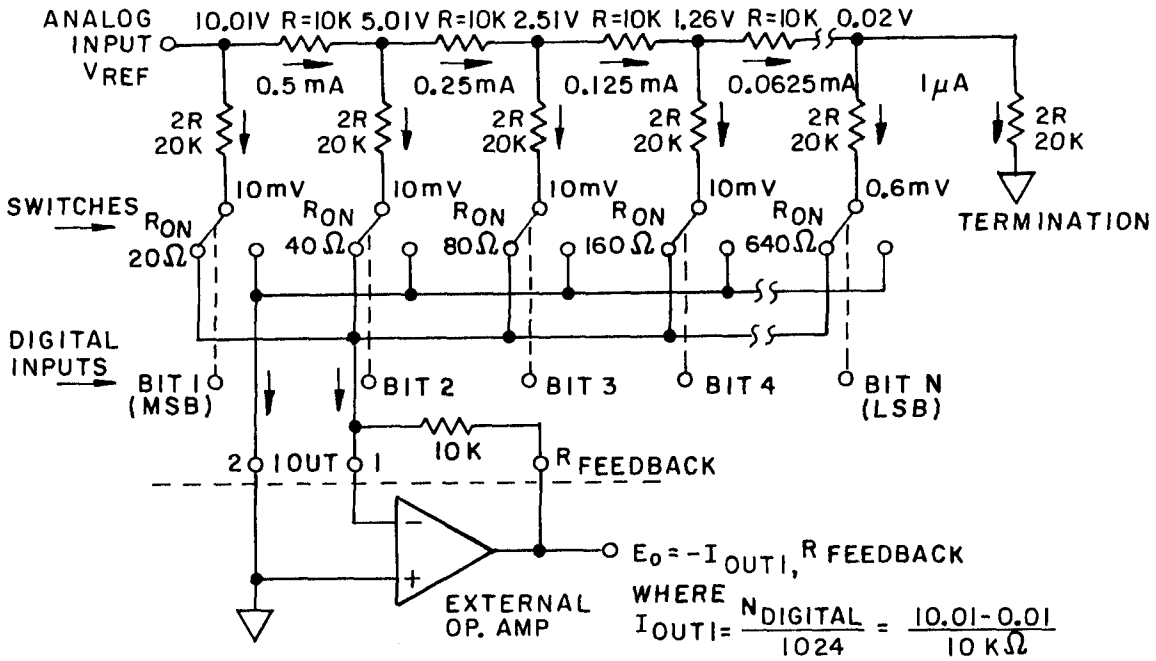
18 lead
dual-in-line
(top view)

FIGURE 1. Terminal connections.



Digital Inputs
(DTL/TTL/CMOS COMPATIBLE)

FIGURE 2. Schematic circuit.



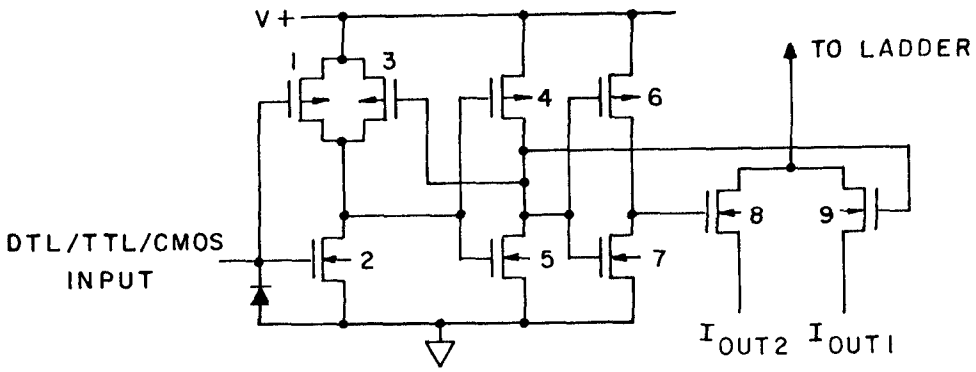
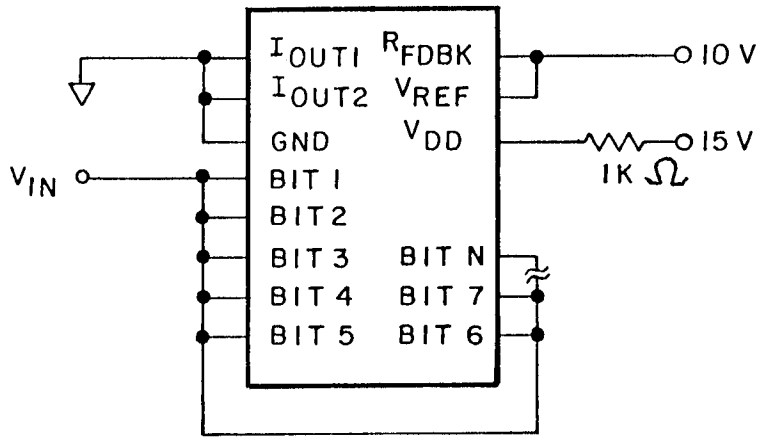


FIGURE 3. Functional diagram and CMOS switch schematic.

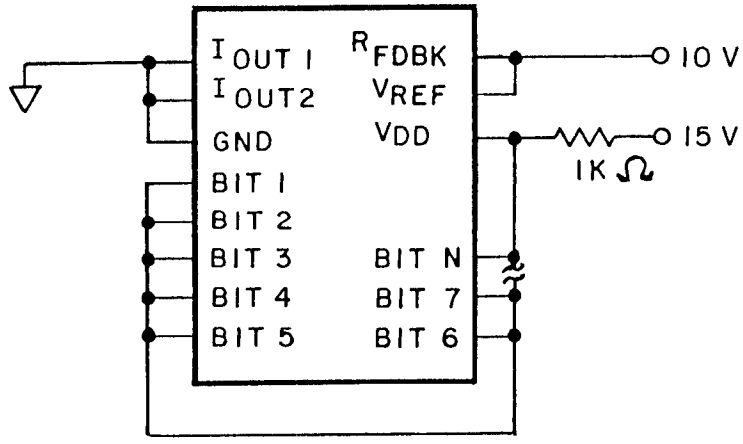


NOTES:

1. The measured value of the resistor shall not exceed ± 5% of its branded value due to use, heat or age.

2. V_{IN} = 0 to 3 V square wave, @ $5 \leq f \leq 10$ Hz

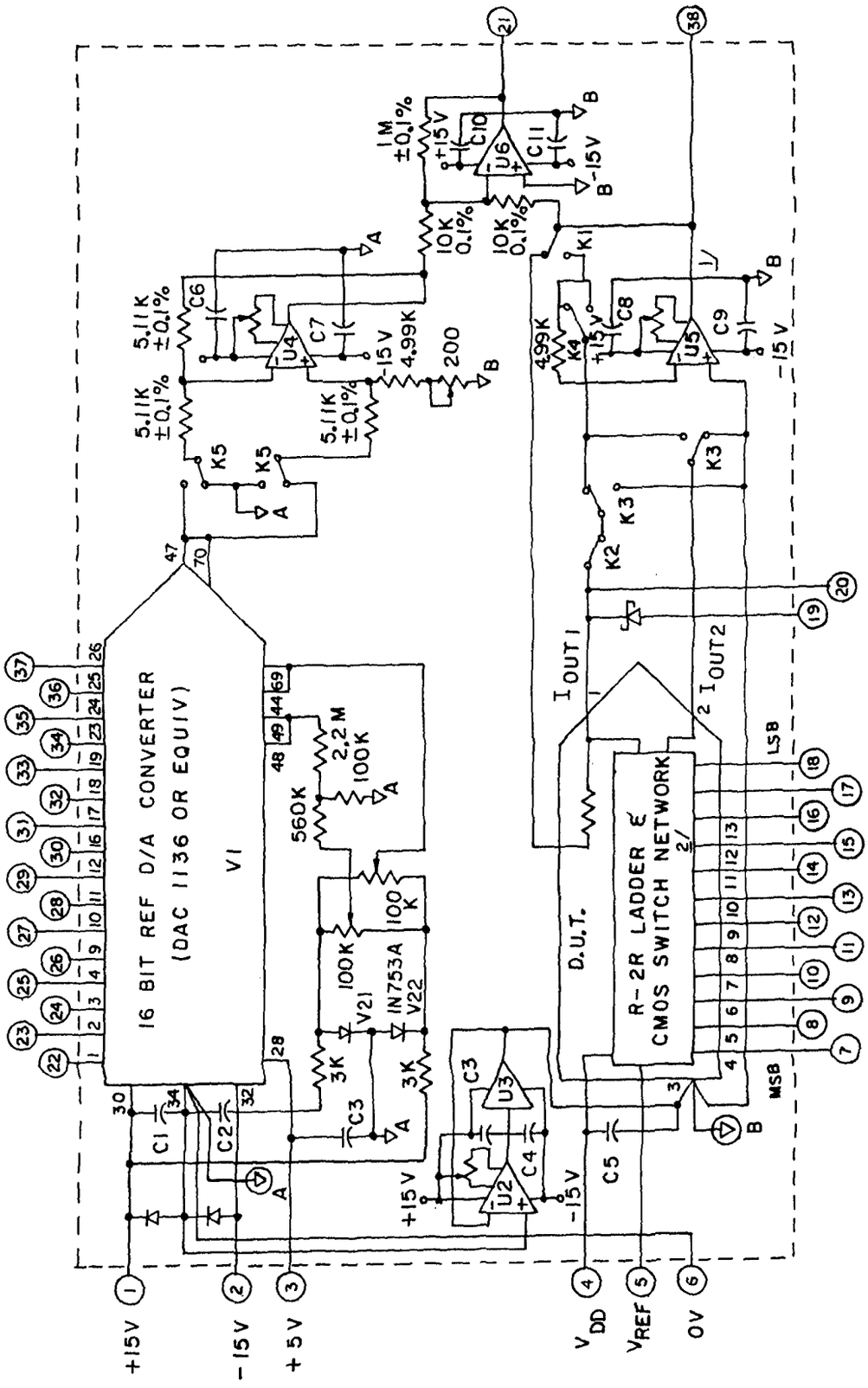
FIGURE 4. Test circuit for the dynamic burn-in and operating life tests.



NOTE:

1. The measured value of the resistor shall not exceed ± 5% of its branded value due to use, heat or age.

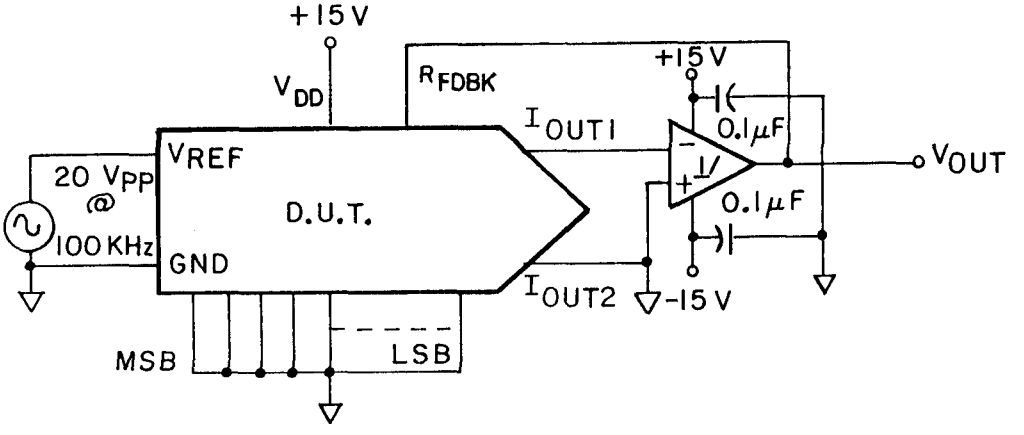
FIGURE 5. Test circuit for the burn-in (steady state power) and life tests.



NOTES: 1/ Op amp offset error (V_{IO} + I_{IB} RF) adds to linearity error since $I_{OUT\ 1}$ and $I_{OUT\ 2}$ must go to 0 V. For 10:1 measurement accuracy with a 12 bit DAC, acceptable op amps include the LF155, LF156 and OP-05 with V_{IO} (adj.) and the OP-07 without V_{IO} (adj.).

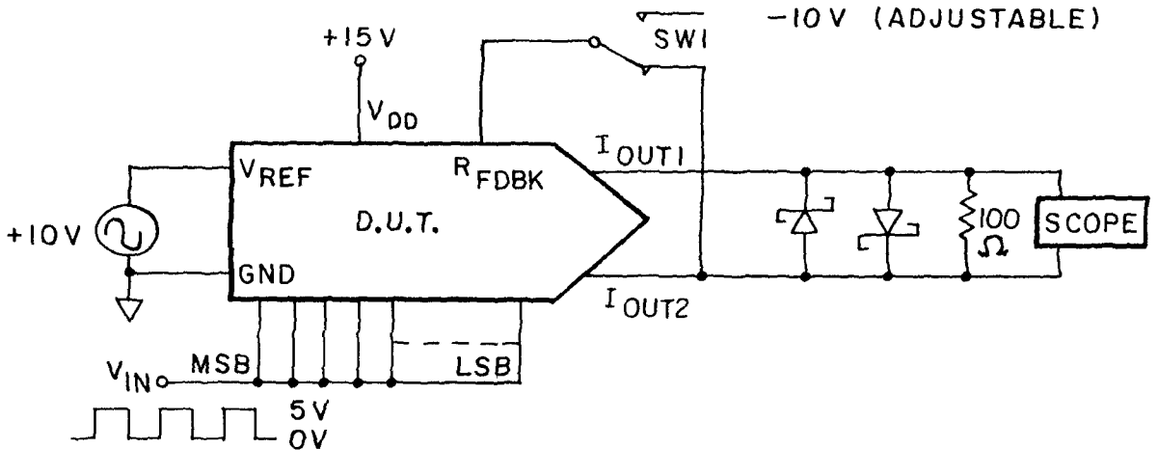
2/ One millivolt of offset error on 10 VFS causes 0.01% linearity error.

FIGURE 6. Test circuit for static tests.



1/ Op amp bandwidth shall be 10 MHz min.

FIGURE 7. Test circuit for feedthru error.



Measure the propagation delay from the 50% point of the digital input transition until the output settles to within 1/2 LSB of final value.

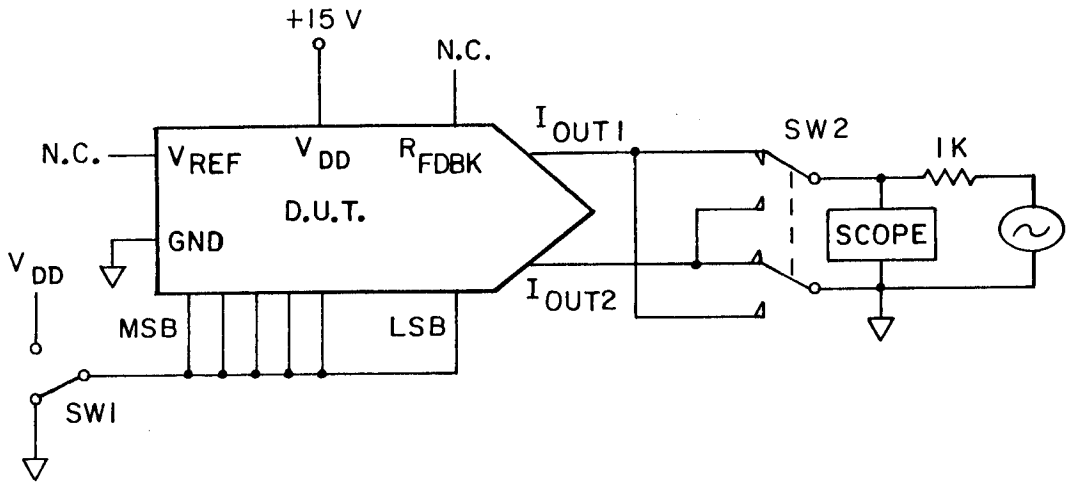
t_{SLH}

1. With $V_{IN} = V_{IH}$, and SW1 at -10 V, adjust -10 V supply for 0V at IOUT1.
2. Switch V_{IN} with pulse train. Measure t_{SLH} from rise of V_{IN} to output settling to within 1/2 LSB.

t_{SHL}

1. Set SW1 to ground.
2. Switch V_{IN} with pulse train. Measure t_{SHL} from fall of V_{IN} to output settling to within 1/2 LSB.

FIGURE 8. Test circuit for settling time.



Calculate Co from Co = 159 $(VA/VO)^2-1)$ - Co'
where Co' is the fixture capacitance without the DUT.

FIGURE 9. Test circuit for output capacitance.

TABLE III. Group A inspection for device type 01.

Subgroup	Symbol	Test no.	Adapter pin numbers 4	5	7 thru 14	22 thru 37	Energized relays	Measured pin No.	Value	Unit	Equation	Limits Min	Max	Unit
Calibration		1	Adjust P6 with all bits at 0 V				K1, K4	38	E1	µV	E_{cal} = E1	---	100	µV
1 T_A = 25°C	I_{DD}	2	+15 V	+10 V	0000 0000	1111 1111 1111 1111	None	4	I1	µA	I_{DD} = I1 (Digital 0 = 0 V)	---	100	µA
		3	"	"	1111 1111	"	"	"	I2	µA	I_{DD} = I2 (Digital 1 = 15 V)	---	100	µA
		4	"	"	0000 0000	"	"	"	I3	mA	I_{DD} = I3 (Digital 0 = 0.8 V)	---	2	mA
		5	"	"	1111 1111	"	"	"	I4	mA	I_{DD} = I4 (Digital 1 = 2.4 V)	---	2	mA
	I_{REF}	6	+15 V	+10 V	1111 1111	1111 1111 1111 1111	K2	20	I5	mA	I_{REF} = I5 (Digital 1 = 15 V)	0.5	2	mA
	I_{REF}	7	+15 V	-10 V	1111 1111	1111 1111 1111 1111	K2	20	I6	mA	I_{REF} = I6 (Digital 1 = 15 V)	-2	-0.5	mA
	I_{IL}	8	+15 V	+10 V	0000 0000	1111 1111 1111 1111	None	7	I7	µA	I_{IL} = I7 (Digital 0 = 0 V)	-1	1	µA
		9	"	"	"	"	"	8	I8	"	I_{IL} = I8 "	"	"	"
		10	"	"	"	"	"	9	I9	"	I_{IL} = I9 "	"	"	"
		11	"	"	"	"	"	10	I10	"	I_{IL} = I10 "	"	"	"
		12	"	"	"	"	"	11	I11	"	I_{IL} = I11 "	"	"	"
		13	"	"	"	"	"	12	I12	"	I_{IL} = I12 "	"	"	"
		14	"	"	"	"	"	13	I13	"	I_{IL} = I13 "	"	"	"
		15	"	"	"	"	"	14	I14	"	I_{IL} = I14 "	"	"	"
	I_{IH}	16	+15 V	+10 V	1111 1111	1111 1111 1111 1111	None	7	I15	µA	I_{IH} = I15 (Digital 1 = 15 V)	-1	1	µA
		17	"	"	"	"	"	8	I16	"	I_{IH} = I16 "	"	"	"
		18	"	"	"	"	"	9	I17	"	I_{IH} = I17 "	"	"	"
		19	"	"	"	"	"	10	I18	"	I_{IH} = I18 "	"	"	"
		20	"	"	"	"	"	11	I19	"	I_{IH} = I19 "	"	"	"
		21	"	"	"	"	"	12	I20	"	I_{IH} = I20 "	"	"	"
		22	"	"	"	"	"	13	I21	"	I_{IH} = I21 "	"	"	"
		23	"	"	"	"	"	14	I22	"	I_{IH} = I22 "	"	"	"
	I_{ZS}	24	+15 V	+10 V	0000 0000	1111 1111 1111 1111	K1	38	E2	mV	I_{ZS} = 2 (E2 - E1)	-100	100	nA
	$I_{ZS'}$	25	+15 V	+10 V	1111 1111	1111 1111 1111 1111	K1, K3	38	E3	mV	$I_{ZS'}$ = 2 (E3 - E1)	-100	100	nA
	$^{+}d_{VFS}$	26	+15 V	+10 V	1111 1111	0000 0000 1111 1111	None	21	E4	V	$^{+}d_{VFS}$ = 0.01 (E4)	-1.5	1.5	%VFS
	$^{-}d_{VFS}$	27	+15 V	-10 V	1111 1111	0000 0000 1111 1111	K5	21	E5	V	$^{-}d_{VFS}$ = 0.01 (E5)	-1.5	1.5	%VFS
	+PSS	28	+15 V	+10 V	1111 1111	0000 0000 1111 1111	None	21	E6	V	+PSS = 1000 (E7 - E6)	-130	130	ppm
			+16 V	+10 V	"	"	"	"	E7	V		"	"	VFS/V
	-PSS	29	+14 V	+10 V	"	"	"	"	E8	V	-PSS = 1000 (E8 - E6)	"	"	"
	VOS	30	+15 V	+10 V	0000 0000	1111 1111 1111 1111	None	21	E9	V	VOS = E9/100 VOS is the DUT zero scale gain error	---	---	V
	LE	31	+15 V	+10 V	0001 0000	1110 1111 1111 1111	None	21	E10	V	For each input code N, calculate the corresponding linearity error in % VFS.	-0.2	0.2	%VFS
		32	"	"	0010 "	1101 "	"	"	E11	"		"	"	"
		33	"	"	0011 "	1100 "	"	"	E12	"		"	"	"
		34	"	"	0100 "	1011 "	"	"	E13	"		"	"	"
		35	"	"	0101 "	1010 "	"	"	E14	"	$LE = 10\left[(EA/100) - (NK + VOS)\right]$	"	"	"
		36	"	"	0110 "	1001 "	"	"	E15	"	Where:	"	"	"
		37	"	"	0111 "	1000 "	"	"	E16	"	EA = Measured value E10 thru E29.	"	"	"
		38	"	"	1000 "	0111 "	"	"	E17	"		"	"	"
		39	"	"	1001 "	0110 "	"	"	E18	"	N = DUT input digital code word in	"	"	"
		40	"	"	1010 "	0101 "	"	"	E19	"	decimal form. Thus for 8 bits	"	"	"
		41	"	"	1011 "	0100 "	"	"	E20	"	$N = (A1)2^7 + (A2)2^6 + \ldots$	"	"	"
		42	"	"	1100 "	0011 "	"	"	E21	"	$+ (A8)2^0$	"	"	"
		43	"	"	1101 "	0010 "	"	"	E22	"	A1,A2, ... A8 are 0 or 1.	"	"	"
		44	"	"	1110 "	0001 "	"	"	E23	"		"	"	"
		45	"	"	1111 "	0000 "	"	"	E24	"	K = Actual volts/count scale factor.	"	"	"
		46	+15 V	+10 V	0000 0001	1111 1110 1111 1111	None	21	E25	V	$K = (^{+}d_{VFS} - VOS)/255$ $^{+}d_{VFS}$ = E4/100	"	"	"
		47	"	"	" 0010	" 1101 "	"	"	E26	"	VOS = E9/100	"	"	"
		48	"	"	" 0100	" 1011 "	"	"	E27	"		"	"	"
		49	"	"	" 1000	" 0111 "	"	"	E28	"		"	"	"

TABLE III. Group A inspection for device type 01 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 4	5	7 thru 14	22 thru 37	Energized relays	Measured pin No.	Value	Unit	Equation	Limits Min	Max	Unit
1 T_A = 25°C	LE	50	+15 V	+10 V	The DUT code word and Ref. D/A complement shall correspond to the most positive error combination of the most significant upper four bits and all of the lower order bits with positive errors.		None	21	E29	V		-0.2	0.2	%VFS
		51 52 53 54	+15 V " " "	+10 V " " "	Starting with the code word for test 50, complement each of the lower order bits one at a time and measure the corresponding errors.		None " " "	21 " " "	E30 E31 E32 E33	V " " "	For each input code N, calculate the corresponding linearity error in % VFS. LE = [10 (EA/100) - (NK + VOS)] Where: EA = Measured value E30 thru E48			
		55	+15 V	+10 V	The DUT code word and Ref. D/A complement shall correspond to the most negative error combination of the most significant upper four bits and all of the lower order bits with negative errors.		None	21	E34	V	N = DUT input digital code word in decimal form. Thus for 8 bits $N = (A1)2^7 + (A2)2^6 + \ldots + (A8)2^0$ A1, A2, ... A8 are 0 or 1.			
		56 57 58 59	+15 V " " "	+10 V " " "	Starting with the code word for test 55, complement each of the lower order bits one at a time and measure the corresponding errors.		None " " "	21 " " "	E35 E36 E37 E38	V " " "	K = Actual volts/count scale factor. $K = (+d_{VFS} - VOS)/255$ $+d_{VFS}$ = E4/100 VOS = E9/100			
		60 thru 69	+15 V	-10 V	Apply the same code combinations to the DUT and Ref. D/A as described for tests 50 thru 59.		K5	21	E39 thru E48	V	The above equations apply except K is computed from the negative full scale error ($-d_{VFS}$) = E5/100			
	MCE	70	+15 V	+10 V	0111 1111 1000 0000	1000 0000 1111 1111 0111 1111 "	None "	21 "	E49 E50	V "	For each set of major carry codes N and N+1, calculate the associated error in %VFS as follows: MCE = [10 (EB - EA)/100 - 0.03906] Where: EB = Measured value E50, E52, E54, etc. EA = Measured value E49, E51, E53, etc.	-0.4	0.4	%VFS
		71	"	"	0011 1111 0100 0000	1100 0000 " 1011 1111 "	" "	" "	E51 E52	" "				
		72	"	"	0001 1111 0010 0000	1110 0000 " 1101 1111 "	" "	" "	E53 E54	" "				
		73	"	"	0000 1111 0001 0000	1111 0000 " 1110 1111 "	" "	" "	E55 E56	" "				
		74	"	"	0000 0111 " 1000	1111 1000 " " 0111 "	" "	" "	E57 E58	" "				
		75	"	"	" 0011 " 0100	" 1100 " " 1011 "	" "	" "	E59 E60	" "				
		76	"	"	" 0001 " 0010	" 1110 " " 1101 "	" "	" "	E61 E62	" "				
		77	"	"	" 0000 " 0001	" 1111 " " 1110 "	" "	" "	E63 E64	" "				
2 T_A = 125°C		78 thru 154	Same tests, terminal conditions, and limits as for subgroup 1, tests 1 thru 77, except T_A = 125°C. Measured values are E65 to E128 and I23 to I44.											
3 T_A = -55°C		155 thru 231	Same tests, terminal conditions, and limits as for subgroup 1, tests 1 thru 77, except T_A = -55°C and I_{DD} = 2.5 mA for all conditions of V_{IL} and V_{IH}. Measured values are E129 to E192 and I45 to I66.											
7 T_A = 25°C	LE	232 233	+15 V "	+10 V "	0000 0000 0000 0001	1111 1111 1111 1111 1111 1110 "	None "	21 "	E193 E194	V "	For each input code N, calculate the corresponding linearity error in %VFS. LE = 10([(EA/100) - (NK + VOS)]) Where: EA = Measured value E193 thru E448 N = DUT input digital code word in decimal form. Thus for 8 bits $N = (A1)2^7 + (A2)2^6 + \ldots + (A8)2^0$ A1, A2, ... A8 are 0 or 1. K = Actual volts/count scale factor. $K = (+d_{VFS} - VOS)/255$ $+d_{VFS}$ = E448/100 VOS = E193/100 Worst positive error Worst positive code Worst negative error Worst negative code			
			"	"	0000 0010	1111 1101 "	"	"		"				
			"	"	...	... "	"	"		"				
			"	"	1111 1101	0000 0010 "	"	"		"				
			"	"	1111 1110	0000 0001 "	"	"		"				
			"	"	1111 1111	0000 0000 "	"	"		"				
			This subgroup checks all digital input codes.									-	.2	%VFS
												-	-	OCT
												.2	-	%VFS
												-	-	OCT

TABLE III. Group A inspection for device type 01 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers: 4	5	7 thru 14	22 thru 37	Energized relays	Measured pin: No.	Value	Unit	Equation	Limits: Min	Max	Unit
8 T_A = 125°C	LE	234 235	Same tests, terminal conditions, and limits as for subgroup 7, tests 232 and 233, except T_A = 125°C.									--- --- -0.2 ---	0.2 --- --- ---	%VFS OCT %VFS OCT
	dV_{FS}/dt	236	Calculate dV_{FS}/dt = (+dV_{FS} at 125°C - +dV_{FS} at 25°C)/100°C from tests 103 and 26, respectively.									-10	10	ppm VFS/°C
8 T_A = -55°C	LE	237 238	Same tests, terminal conditions, and limits as for subgroup 7, tests 232 and 233, except T_A = -55°C.									--- --- -0.2 ---	0.2 --- --- ---	%VFS OCT %VFS OCT
	dV_{FS}/dt	239	Calculate dV_{FS}/dt = (+dV_{FS} at -55°C - +dV_{FS} at 25°C)/80°C from tests 180 and 26, respectively.									-10	10	ppm VFS/°C
12 T_A = 25°C	FTE	240	V_{REF} = 20 Vpp at 100 kHz. All digital inputs = 0 V. See figure 7.					6	V1	mVpp	FTE = V1	---	10	mVpp
	t_{SLH}	241	All digital inputs switched simultaneously from logic low to logic high. Output settling is to within 1/2 LSB of the rated accuracy. See figure 8.					6	t1	µs	t_{SLH} = t1	---	1	µs
	t_{SHL}	242	All digital inputs switched simultaneously from logic high to logic low. Output settling is to within 1/2 LSB of the rated accuracy. See figure 8.					6	t2	µs	t_{SHL} = t2	---	1	µs
	C_o	243	All digital inputs set at V_{DD}. V_a = 100 mVpp at 1 MHz is applied thru a 1 kΩ resistor to the output under test. See figure 9.					6	V2	mVpp	$C_o = 159\sqrt{((V_a/V_o)^2 - 1)} - C_o'$ Where: V_o = The measured output. C_o' = The fixture capacitance.	---	200	pF
		244						7	V3	mVpp		---	75	pF
	C_o	245	All digital inputs set at 0 V. V_a = 100 mVpp at 1 MHz is applied thru a 1 kΩ resistor to the output under test. See figure 9.					6	V4	mVpp	$C_o = 159\sqrt{((V_a/V_o)^2 - 1)} - C_o'$ Where: V_o = The measured output. C_o' = The fixture capacitance.	---	75	pF
		246						7	V5	mVpp		---	200	pF

TABLE III. Group A inspection for device types 02 and 05.

Subgroup	Symbol	Test no.	Adapter pin numbers: 4	5	7 thru 16	22 thru 37	Energized relays	Measured pin: No.	Value	Unit	Equation		Device type	Limits: Min	Max	Unit
Calibration		1	Adjust P6 with all bits at 0 V				K1, K4	38	E1	μV	E_{cal} = E1		02,05	---	100	μV
1 T_A = 25°C	I_{DD}	2	+15 V	+10 V	0000 0000 00	1111 1111 1111 1111	None	4	I1	μA	I_{DD} = I1	(Digital 0 = 0 V)	02	---	100	μA
										mA			05	---	2	mA
		3	"	"	1111 1111 11	"	"	"	I2	μA	I_{DD} = I2	(Digital 1 = 15 V)	02	---	100	μA
										mA			05	---	2	mA
		4	"	"	0000 0000 00	"	"	"	I3	mA	I_{DD} = I3	(Digital 0 = 0.8 V)	02,05	---	2	mA
		5	"	"	1111 1111 11	"	"	"	I4	mA	I_{DD} = I4	(Digital 1 = 2.4 V)	02,05	---	2	mA
	I_{REF}	6	+15 V	+10 V	1111 1111 11	1111 1111 1111 1111	K2	20	I5	mA	I_{REF} = I5	(Digital 1 = 15 V)	02,05	0.5	2	mA
	I_{REF}	7	+15 V	-10 V	1111 1111 11	1111 1111 1111 1111	K2	20	I6	mA	I_{REF} = I6	(Digital 1 = 15 V)	02,05	-2	-0.5	mA
	I_{IL}	8	+15 V	+10 V	0000 0000 00	1111 1111 1111 1111	None	7	I7	μA	I_{IL} = I7	(Digital 0 = 0 V)	02	-1	1	μA
		9	"	"	"	"	"	8	I8	"	I_{IL} = I8	"	"	"	"	"
		10	"	"	"	"	"	9	I9	"	I_{IL} = I9	"	"	"	"	"
		11	"	"	"	"	"	10	I10	"	I_{IL} = I10	"	"	"	"	"
		12	"	"	"	"	"	11	I11	"	I_{IL} = I11	"	"	"	"	"
		13	"	"	"	"	"	12	I12	"	I_{IL} = I12	"	"	"	"	"
		14	"	"	"	"	"	13	I13	"	I_{IL} = I13	"	"	"	"	"
		15	"	"	"	"	"	14	I14	"	I_{IL} = I14	"	"	"	"	"
		16	"	"	"	"	"	15	I15	"	I_{IL} = I15	"	"	"	"	"
		17	"	"	"	"	"	16	I16	"	I_{IL} = I16	"	"	"	"	"
		8 thru 17	For device type 05, conditions are the same as indicated above, except V_{IL} = 0.0 V.									(Digital 0 = 0 V)	05	-200	1	μA
		8 thru 17	For device type 05, conditions are the same as indicated above, except V_{IL} = 0.8 V.									(Digital 0 = 0.8 V)	05	-200	1	μA
	I_{IH}	18	+15 V	+10 V	1111 1111 11	1111 1111 1111 1111	None	7	I17	μA	I_{IH} = I17	(Digital 1 = 15 V)	02	-1	1	μA
		19	"	"	"	"	"	8	I18	"	I_{IH} = I18	"	"	"	"	"
		20	"	"	"	"	"	9	I19	"	I_{IH} = I19	"	"	"	"	"
		21	"	"	"	"	"	10	I20	"	I_{IH} = I20	"	"	"	"	"
		22	"	"	"	"	"	11	I21	"	I_{IH} = I21	"	"	"	"	"
		23	"	"	"	"	"	12	I22	"	I_{IH} = I22	"	"	"	"	"
		24	"	"	"	"	"	13	I23	"	I_{IH} = I23	"	"	"	"	"
		25	"	"	"	"	"	14	I24	"	I_{IH} = I24	"	"	"	"	"
		26	"	"	"	"	"	15	I25	"	I_{IH} = I25	"	"	"	"	"
		27	"	"	"	"	"	16	I26	"	I_{IH} = I26	"	"	"	"	"
		18 thru 27	For device type 05, conditions are the same as indicated above, except $V_{IH} = V_{DD}$.									(Digital 1 = V_{DD})	05	-1	100	μA
		18 thru 27	For device type 05, conditions are the same as indicated above, except V_{IH} = 2.4 V.									(Digital 1 = 2.4 V)	05	-1	100	μA
	I_{ZS}	28	+15 V	+10 V	0000 0000 00	1111 1111 1111 1111	K1	38	E2	mV	I_{ZS} = 2 (E2 - E1)		02,05	-100	100	nA
	$I_{ZS'}$	29	+15 V	+10 V	1111 1111 11	1111 1111 1111 1111	K1, K3	38	E3	mV	$I_{ZS'}$ = 2 (E3 - E1)		02,05	-100	100	nA
	$+d_{VFS}$	30	+15 V	+10 V	1111 1111 11	0000 0000 0011 1111	None	21	E4	V	$+d_{VFS}$ = 0.01 (E4)		02,05	-1	1	%VFS
	$-d_{VFS}$	31	+15 V	-10 V	1111 1111 11	0000 0000 0011 1111	K5	21	E5	V	$-d_{VFS}$ = 0.01 (E5)		02,05	-1	1	%VFS

TABLE III. Group A inspection for device types 02 and 05 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 4	5	7 thru 16	22 thru 37	Energized relays	Measured pin No.	Value	Unit	Equation	Device type	Limits Min	Max	Unit
1 T_A = 25°C	+PSS	32	+15 V +16 V	+10 V +10 V	1111 1111 11 "	0000 0000 0011 1111 "	None "	21 "	E6 E7	V V	+PSS = 1000 (E7 - E6)	02	-130	130	ppm VFS/V
	-PSS	33	+14 V	+10 V	"	"	"	"	E8	V	-PSS = 1000 (E8 - E6)	"	"	"	"
		32 and 33	For device type 05, conditions are the same as indicated above.									05	-20	20	" " "
	VOS	34	+15 V	+10 V	0000 0000 00	1111 1111 1111 1111	None	21	E9	V	VOS = E9/100 VOS is the DUT zero scale gain error	02,05	---	---	V
	LE	35	+15 V	+10 V	0001 0000 00	1110 1111 1111 1111	None	21	E10	V	For each input code N, calculate the corresponding linearity error in % VFS. LE = 10[(EA/100) - (NK + VOS)] Where: EA = Measured value E10 thru E31. N = DUT input digital code word in decimal form. Thus for 10 bits N = $(A1)2^9 + (A2)2^8 + \ldots + (A10)2^0$ A1,A2, ... A10 are 0 or 1. K = Actual volts/count scale factor. K = $(+d_{VFS} - VOS)/1023$ $+d_{VFS}$ = E4/100 VOS = E9/100	02,05	-.05	.05	%VFS
		36	"	"	0010 "	1101 "	"	"	E11	"		"	"	"	"
		37	"	"	0011 "	1100 "	"	"	E12	"		"	"	"	"
		38	"	"	0100 "	1011 "	"	"	E13	"		"	"	"	"
		39	"	"	0101 "	1010 "	"	"	E14	"		"	"	"	"
		40	"	"	0110 "	1001 "	"	"	E15	"		"	"	"	"
		41	"	"	0111 "	1000 "	"	"	E16	"		"	"	"	"
		42	"	"	1000 "	0111 "	"	"	E17	"		"	"	"	"
		43	"	"	1001 "	0110 "	"	"	E18	"		"	"	"	"
		44	"	"	1010 "	0101 "	"	"	E19	"		"	"	"	"
		45	"	"	1011 "	0100 "	"	"	E20	"		"	"	"	"
		46	"	"	1100 "	0011 "	"	"	E21	"		"	"	"	"
		47	"	"	1101 "	0010 "	"	"	E22	"		"	"	"	"
		48	"	"	1110 "	0001 "	"	"	E23	"		"	"	"	"
		49	"	"	1111 "	0000 "	"	"	E24	"		"	"	"	"
		50	+15 V	+10 V	0000 0000 01	1111 1111 1011 1111	None	21	E25	V		"	"	"	"
		51	"	"	" 0000 10	" 1111 0111 "	"	"	E26	"		"	"	"	"
		52	"	"	" 0001 00	" 1110 1111 "	"	"	E27	"		"	"	"	"
		53	"	"	" 0010 00	" 1101 1111 "	"	"	E28	"		"	"	"	"
		54	"	"	" 0100 00	" 1011 1111 "	"	"	E29	"		"	"	"	"
		55	"	"	" 1000 00	" 0111 1111 "	"	"	E30	"		"	"	"	"
		56	+15 V	+10 V	The DUT code word and Ref. D/A complement shall correspond to the most positive error combination of the most significant upper four bits and all of the lower order bits with positive errors.		None	21	E31	V		"	"	"	"
		57	+15 V	+10 V	Starting with the code word for test 56, complement each of the lower order bits one at a time and measure the corresponding errors.		None	21	E32	V	For each input code N, calculate the corresponding linearity error in % VFS. LE = 10[(EA/100) - (NK + VOS)] Where: EA = Measured value E32 thru E58	"	"	"	"
		58	"	"			"	"	E33	"		"	"	"	"
		59	"	"			"	"	E34	"		"	"	"	"
		60	"	"			"	"	E35	"		"	"	"	"
		61	"	"			"	"	E36	"		"	"	"	"
		62	"	"			"	"	E37	"		"	"	"	"
		63	+15 V	+10 V	The DUT code word and Ref. D/A complement shall correspond to the most negative error combination of the most significant upper four bits and all of the lower order bits with negative errors.		None	21	E38	V	N = DUT input digital code word in decimal form. Thus for 10 bits N = $(A1)2^9 + (A2)2^8 + \ldots + (A10)2^0$ A1, A2, ... A10 are 0 or 1. K = Actual volts/count scale factor. K = $(+d_{VFS} - VOS)/1023$ $+d_{VFS}$ = E4/100 VOS = E9/100	"	"	"	"
		64	+15 V	+10 V	Starting with the code word for test 63, complement each of the lower order bits one at a time and measure the corresponding errors.		None	21	E39	V		"	"	"	"
		65	"	"			"	"	E40	"		"	"	"	"
		66	"	"			"	"	E41	"		"	"	"	"
		67	"	"			"	"	E42	"		"	"	"	"
		68	"	"			"	"	E43	"		"	"	"	"
		69	"	"			"	"	E44	"		"	"	"	"
		70 thru 83	+15 V	-10 V	Apply the same code combinations to the DUT and Ref. D/A as described for tests 56 thru 69.		K5	21	E45 thru E58	V	The above equations apply except K is computed from the negative full scale error $(-d_{VFS})$ = E5/100.	"	"	"	"

TABLE III. Group A inspection for device types 02 and 05 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 4	5	7 thru 16	22 thru 37	Energized relays	Measured pin No.	Value	Unit	Equation	Device type	Limits Min	Max	Unit
1 $T_A = 25^\circ C$	MCE	84	+15 V	+10 V	0111 1111 11	1000 0000 0011 1111	None	21	E59	V	For each set of major carry codes	02,05	-0.1	0.1	%VFS
					1000 0000 00	0111 1111 1111 "	"	"	E60	"	N and N+1, calculate the	"	"	"	"
		85	"	"	0011 1111 11	1100 0000 0011 "	"	"	E61	"	associated error in %VFS as	"	"	"	"
					0100 0000 00	1011 1111 1111 "	"	"	E62	"	follows:	"	"	"	"
		86	"	"	0001 1111 11	1110 0000 0011 "	"	"	E63	"	MCE = 10[(EB - EA)/100 - 0.00976$]	"	"	"	"
					0010 0000 00	1101 1111 1111 "	"	"	E64	"	Where:	"	"	"	"
		87	"	"	0000 1111 11	1111 0000 0011 "	"	"	E65	"	EB = Measured value E60, E62,	"	"	"	"
					0001 0000 00	1110 1111 1111 "	"	"	E66	"	E64, etc.	"	"	"	"
		88	"	"	0000 0111 11	1111 1000 0011 "	"	"	E67	"		"	"	"	"
					" 1000 00	" 0111 1111 "	"	"	E68	"	EA = Measured value E59, E61,	"	"	"	"
		89	"	"	" 0011 11	" 1100 0011 "	"	"	E69	"	E63, etc.	"	"	"	"
					" 0100 00	" 1011 1111 "	"	"	E70	"		"	"	"	"
		90	"	"	" 0001 11	" 1110 0011 "	"	"	E71	"		"	"	"	"
					" 0010 00	" 1101 1111 "	"	"	E72	"		"	"	"	"
		91	"	"	" 0000 11	" 1111 0011 "	"	"	E73	"		"	"	"	"
					" 0001 00	" 1110 1111 "	"	"	E74	"		"	"	"	"
		92	"	"	" 0000 01	" 1111 1011 "	"	"	E75	"		"	"	"	"
					" 0000 10	" 1111 0111 "	"	"	E76	"		"	"	"	"
		93	"	"	" 0000 00	" 1111 1111 "	"	"	E77	"		"	"	"	"
					" 0000 01	" 1111 1011 "	"	"	E78	"		"	"	"	"
2 $T_A = 125^\circ C$		94 thru 186	Same tests, terminal conditions, and limits as for subgroup 1, tests 1 thru 93, except $T_A = 125^\circ C$. Measured values are E79 to E156 and I27 to I53.												
3 $T_A = -55^\circ C$		187 thru 279	Same tests, terminal conditions, and limits as for subgroup 1, tests 1 thru 93, except $T_A = -55^\circ C$ and I_{DD} = 2.5 mA for all conditions of V_{IL} and V_{IH}. Measured values are E157 to E234 and I54 to I80.												
7 $T_A = 25^\circ C$	LE	280	+15 V	+10 V	0000 0000 00	1111 1111 1111 1111	None	21	E235	V	For each input code N, calculate				
		281	"	"	0000 0000 01	1111 1111 1011	"	"	E236	"	the corresponding linearity error				
			"	"	0000 0000 10	1111 1111 0111	"	"		"	in %VFS.				
			"	"	...	...	"	"		"					
			"	"			"	"		"					
			"	"	1111 1111 01	0000 0000 1011	"	"		"	LE = 10[(EA/100) - (NK + VOS)]				
			"	"	1111 1111 10	0000 0000 0111	"	"		"	Where:				
			"	"	1111 1111 11	0000 0000 0011	"	"		"	EA = Measured value E235				
					This subgroup checks all digital input codes.						thru E1258				
											N = DUT input digital code word in decimal form. Thus for 10 bits $N = (A1)2^9 + (A2)2^8 + \ldots + (A10)2^0$ A1, A2,... A10 are 0 or 1.				
											K = Actual volts/count scale factor.				
											K = (+d_{VFS} - VOS)/1023 VOS = E235/100				
											Worst positive error		-	.05	%FS
											Worst positive code		-	-	LSB
											Worst negative error		-.05	-	%FS
											Worst negative code		-	-	LSB
8 $T_A = 125^\circ C$	LE	282	Same tests, terminal conditions, and limits as for subgroup 7, tests 280 and 281, except $T_A = 125^\circ C$.									02,05	-	.05	%VFS
													-	-	LSB
		283											-.05	-	%VFS
													-	-	LSB
	d_{VFS}/d_t	284	Calculate d_{VFS}/d_t = (+d_{VFS} at 125°C - +d_{VFS} at 25°C)/100°C from tests 123 and 30, respectively.									02,05	-10	10	ppm VFS/°C
8 $T_A = -55^\circ C$	LE	285	Same tests, terminal conditions, and limits as for subgroup 7, tests 280 and 281, except $T_A = -55^\circ C$.									02,05	-	.05	%VFS
													-	-	LSB
		286											-.05	-	%VFS
													-	-	LSB
	d_{VFS}/d_T	287	Calculate d_{VFS}/d_t = (+d_{VFS} at -55°C - +d_{VFS} at 25°C)/80°C from tests 216 and 30, respectively.									02,05	-10	10	ppm VFS/°C

TABLE III. Group A inspection for device types 02 and 05 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers: 4	5	7 thru 16	22 thru 37	Energized relays	Measured pin: No.	Value	Unit	Equation	Device type	Limits: Min	Max	Unit
12 T_A = 25°C	FTE	3354	V_{REF} = 20 Vpp at 100 kHz. All digital inputs = 0 V. See figure 7.					6	V1	mVpp	FTE = V1	02 05	--- ---	10 25	mVpp mVpp
	t_{SLH}	3355	All digital inputs switched simultaneously from logic low to logic high. For each device type, output settling is to within 1/2 LSB of the rated accuracy. See figure 8.					6	t1	µs	t_{SLH} = t1	02,05	---	1	µs
	t_{SHL}	3356	All digital inputs switched simultaneously from logic high to logic low. For each device type, output settling is to within 1/2 LSB of the rated accuracy. See figure 8.					6	t2	µs	t_{SHL} = t2	02,05	---	1	µs
	C_o	3357	All digital inputs set at V_{DD}. V_a = 100 mVpp at 1 MHz is applied thru a 1 kΩ resistor to the output under test. See figure 9.					6	V2	mVpp	$C_o = 159\sqrt{(V_a/V_o)^2 - 1} - C_o'$ Where: V_o = The measured output. C_o' = The fixture capacitance.	02 05	--- ---	200 300	pF "
		3358						7	V3	mVpp		05 02	--- ---	100 75	" "
	C_o	3359	All digital inputs set at 0 V. V_a = 100 mVpp at 1 MHz is applied thru a 1 kΩ resistor to the output under test. See figure 9.					6	V4	mVpp	$C_o = 159\sqrt{(V_a/V_o)^2 - 1} - C_o'$ Where: V_o = The measured output. C_o' = The fixture capacitance.	02 05	--- ---	75 100	pF "
		3360						7	V5	mVpp		05 02	--- ---	300 200	" "

TABLE III. Group A inspection for device types 03, 04, 06, and 07.

Subgroup	Symbol	Test no.	Adapter pin numbers: 4	5	7 thru 18	22 thru 37	Energized relays	Measured pin: No.	Value	Unit	Equation		Device type	Limits: Min	Max	Unit
Calibration		1	Adjust P6 with all bits at 0 V				K1, K4	38	E1	μV	E_{cal} = E1		All	---	100	μV
1 T_A = 25°C	I_{DD}	2	+15 V	+10 V	0000 0000 0000	1111 1111 1111 1111	None	4	I1	μA	I_{DD} = I1	(Digital 0 = 0 V)	03,04	---	100	μA
										mA			06,07	---	2	mA
		3	"	"	1111 1111 1111	"	"	"	I2	μA	I_{DD} = I2	(Digital 1 = 15 V)	03,04	---	100	μA
										mA			06,07	---	2	mA
		4	"	"	0000 0000 0000	"	"	"	I3	mA	I_{DD} = I3	(Digital 0 = 0.8 V)	All	---	2	mA
		5	"	"	1111 1111 1111	"	"	"	I4	mA	I_{DD} = I4	(Digital 1 = 2.4 V)	All	---	2	mA
	I_{REF}	6	+15 V	+10 V	1111 1111 1111	1111 1111 1111 1111	K2	20	I5	mA	I_{REF} = I5	(Digital 1 = 15 V)	All	0.5	2	mA
	I_{REF}	7	+15 V	-10 V	1111 1111 1111	1111 1111 1111 1111	K2	20	I6	mA	I_{REF} = I6	(Digital 1 = 15 V)	All	-2	-0.5	mA
	I_{IL}	8	+15 V	+10 V	0000 0000 0000	1111 1111 1111 1111	None	7	I7	μA	I_{IL} = I7	(Digital 0 = 0 V)	03,04	-1	1	μA
		9	"	"	"	"	"	8	I8	"	I_{IL} = I8	"	"	"	"	"
		10	"	"	"	"	"	9	I9	"	I_{IL} = I9	"	"	"	"	"
		11	"	"	"	"	"	10	I10	"	I_{IL} = I10	"	"	"	"	"
		12	"	"	"	"	"	11	I11	"	I_{IL} = I11	"	"	"	"	"
		13	"	"	"	"	"	12	I12	"	I_{IL} = I12	"	"	"	"	"
		14	"	"	"	"	"	13	I13	"	I_{IL} = I13	"	"	"	"	"
		15	"	"	"	"	"	14	I14	"	I_{IL} = I14	"	"	"	"	"
		16	"	"	"	"	"	15	I15	"	I_{IL} = I15	"	"	"	"	"
		17	"	"	"	"	"	16	I16	"	I_{IL} = I16	"	"	"	"	"
		18	"	"	"	"	"	17	I17	"	I_{IL} = I17	"	"	"	"	"
		19	"	"	"	"	"	18	I18	"	I_{IL} = I18	"	"	"	"	"
		8 thru 19	For device types 06 and 07, conditions are the same as indicated above, except V_{IL} = 0.0 V.									(Digital 0 = 0 V)	06,07	-200	1	μA
		8 thru 19	For device types 06 and 07, conditions are the same as indicated above, except V_{IL} = 0.8 V.									(Digital 0 = 0.8 V)	06,07	-200	1	μA
	I_{IH}	20	+15 V	+10 V	1111 1111 1111	1111 1111 1111 1111	None	7	I19	μA	I_{IH} = I19	(Digital 1 = 15 V)	03,04	-1	1	μA
		21	"	"	"	"	"	8	I20	"	I_{IH} = I20	"	"	"	"	"
		22	"	"	"	"	"	9	I21	"	I_{IH} = I21	"	"	"	"	"
		23	"	"	"	"	"	10	I22	"	I_{IH} = I22	"	"	"	"	"
		24	"	"	"	"	"	11	I23	"	I_{IH} = I23	"	"	"	"	"
		25	"	"	"	"	"	12	I24	"	I_{IH} = I24	"	"	"	"	"
		26	"	"	"	"	"	13	I25	"	I_{IH} = I25	"	"	"	"	"
		27	"	"	"	"	"	14	I26	"	I_{IH} = I26	"	"	"	"	"
		28	"	"	"	"	"	15	I27	"	I_{IH} = I27	"	"	"	"	"
		29	"	"	"	"	"	16	I28	"	I_{IH} = I28	"	"	"	"	"
		30	"	"	"	"	"	17	I29	"	I_{IH} = I29	"	"	"	"	"
		31	"	"	"	"	"	18	I30	"	I_{IH} = I30	"	"	"	"	"
		20 thru 31	For device types 06 and 07, conditions are the same as indicated above, except V_{IH} = V_{DD}.									(Digital 1 = V_{DD})	06,07	-1	100	μA
		20 thru 31	For device types 06 and 07, conditions are the same as indicated above, except V_{IH} = 2.4 V.									(Digital 1 = 2.4 V)	06,07	-1	100	μA
	I_{ZS}	32	+15 V	+10 V	0000 0000 0000	1111 1111 1111 1111	K1	38	E2	mV	I_{ZS} = 2 (E2 - E1)		03,06	-100	100	nA
													04,07	-50	50	"
	$I_{ZS'}$	33	+15 V	+10 V	1111 1111 1111	1111 1111 1111 1111	K1, K3	38	E3	mV	$I_{ZS'}$ = 2 (E3 - E1)		03,06	-100	100	"
													04,07	-50	50	"
	$+d_{VFS}$	34	+15 V	+10 V	1111 1111 1111	0000 0000 0000 1111	None	21	E4	V	$+d_{VFS}$ = 0.01 (E4)		All	-.4	.4	VFS
	$-d_{VFS}$	35	+15 V	-10 V	1111 1111 1111	0000 0000 0000 1111	K5	21	E5	V	$-d_{VFS}$ = 0.01 (E5)		All	-.4	.4	VFS

TABLE III. Group A inspection for device types 03, 04, 06, and 07 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 4	5	7 thru 18	22 thru 37	Energized relays	Measured pin No.	Value	Unit	Equation	Device type	Limits Min	Max	Unit
1 T_A = 25°C	+PSS	36	+15 V	+10 V	1111 1111 1111	0000 0000 0000 1111	None	21	E6	V	+PSS = 1000 (E7 - E6)	03,04	-130	130	ppm
			+16 V	+10 V	"	"	"	"	E7	V					VFS/V
	-PSS	37	+14 V	+10 V	"	"	"	"	E8	V	-PSS = 1000 (E8 - E6)	"	"	"	"
		36 and 37	For device types 06 and 07, conditions are the same as indicated above.									06,07	-20	20	"
	VOS	38	+15 V	+10 V	0000 0000 0000	1111 1111 1111 1111	None	21	E9	V	VOS = E9/100 VOS is the DUT zero scale gain error	A11	---	---	V
	LE	39	+15 V	+10 V	0001 0000 0000	1110 1111 1111 1111	None	21	E10	V	For each input code N, calculate the corresponding linearity error in % VFS.	03,06	-.05	.05	%VFS
		40	"	"	0010 "	1101 "	"	"	E11	"		04,07	-.012	.012	"
		41	"	"	0011 "	1100 "	"	"	E12	"		"	"	"	"
		42	"	"	0100 "	1011 "	"	"	E13	"		"	"	"	"
		43	"	"	0101 "	1010 "	"	"	E14	"	LE = 10[(EA/100) - (NK + VOS)]	"	"	"	"
		44	"	"	0110 "	1001 "	"	"	E15	"	Where:	"	"	"	"
		45	"	"	0111 "	1000 "	"	"	E16	"	EA = Measured value E10 thru E33.	"	"	"	"
		46	"	"	1000 "	0111 "	"	"	E17	"		"	"	"	"
		47	"	"	1001 "	0110 "	"	"	E18	"	N = DUT input digital code word in decimal form. Thus for 12 bits	"	"	"	"
		48	"	"	1010 "	0101 "	"	"	E19	"	$N = (A1)2^{11} + (A2)2^{10} + \ldots + (A12)2^{0}$	"	"	"	"
		49	"	"	1011 "	0100 "	"	"	E20	"		"	"	"	"
		50	"	"	1100 "	0011 "	"	"	E21	"	A1,A2, ... A12 are 0 or 1.	"	"	"	"
		51	"	"	1101 "	0010 "	"	"	E22	"		"	"	"	"
		52	"	"	1110 "	0001 "	"	"	E23	"		"	"	"	"
		53	"	"	1111 "	0000 "	"	"	E24	"	K = Actual volts/count scale factor.	"	"	"	"
		54	+15 V	+10 V	0000 0000 0001	1111 1111 1110 1111	None	21	E25	V	$K = (+d_{VFS} - VOS)/4095$	"	"	"	"
		55	"	"	" 0010	" 1101 "	"	"	E26	"	$+d_{VFS} = E4/100$	"	"	"	"
		56	"	"	" 0100	" 1011 "	"	"	E27	"	VOS = E9/100	"	"	"	"
		57	"	"	" 1000	" 0111 "	"	"	E28	"		"	"	"	"
		58	+15 V	+10 V	0000 0001 0000	1111 1011 1111 1111	None	21	E29	V		"	"	"	"
		59	"	"	" 0010 "	" "	"	"	E30	"		"	"	"	"
		60	"	"	" 0100 "	" "	"	"	E31	"		"	"	"	"
		61	"	"	" 1000 "	" "	"	"	E32	"		"	"	"	"
		62	+15 V	+10 V	The DUT code word and Ref. D/A complement shall correspond to the most positive error combination of the most significant upper four bits and all of the lower order bits with positive errors.		None	21	E33	V		"	"	"	"
		63	+15 V	+10 V	Starting with the code word for test 62, complement each of the lower order bits one at a time and measure the corresponding errors.		None	21	E34	V	For each input code N, calculate the corresponding linearity error in % VFS.	"	"	"	"
		64	"	"			"	"	E35	"		"	"	"	"
		65	"	"			"	"	E36	"		"	"	"	"
		66	"	"			"	"	E37	"		"	"	"	"
		67	"	"			"	"	E38	"	LE = 10[(EA/100 - (NK + VOS)]	"	"	"	"
		68	"	"			"	"	E39	"		"	"	"	"
		69	"	"			"	"	E40	"	Where:	"	"	"	"
		70	"	"			"	"	E41	"		"	"	"	"
											EA = Measured value E34 thru E68	"	"	"	"
		71	+15 V	+10 V	The DUT code word and Ref. D/A complement shall correspond to the most negative error combination of the most significant upper four bits and all of the lower order bits with negative errors.		None	21	E42	V	N = DUT input digital code word in decimal form. Thus for 12 bits	"	"	"	"
											$N = (A1)2^{11} + (A2)2^{10} + \ldots + (A12)2^{0}$	"	"	"	"
											A1, A2, ... A12 are 0 or 1.	"	"	"	"
		72	+15 V	+10 V	Starting with the code word for test 71, complement each of the lower order bits one at a time and measure the corresponding errors.		None	21	E43	V	K = Actual volts/count scale factor.	"	"	"	"
		73	"	"			"	"	E44	"		"	"	"	"
		74	"	"			"	"	E45	"	$K = (+d_{VFS} - VOS)/4095$	"	"	"	"
		75	"	"			"	"	E46	"	$+d_{VFS} = E4/100$	"	"	"	"
		76	"	"			"	"	E47	"	VOS = E9/100	"	"	"	"
		77	"	"			"	"	E48	"		"	"	"	"
		78	"	"			"	"	E49	"		"	"	"	"
		79	"	"			"	"	E50	"		"	"	"	"
		80 thru 97	+15 V	-10 V	Apply the same code combinations to the DUT and Ref. D/A as described for tests 62 thru 79.		K5	21	E51 thru E68	V	The above equations apply except K is computed from the negative full scale error $(-d_{VFS})$ = E5/100.	"	"	"	"

TABLE III. Group A inspection for device types 03, 04, 06, and 07 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers 4	5	7 thru 18	22 thru 37	Energized relays	Measured pin No.	Value	Unit	Equation	Device type	Limits Min	Max	Unit
1 T_A = 25°C	MCE	98	+15 V	+10 V	0111 1111 1111	1000 0000 0000 1111	None	21	E69	V	For each set of major carry codes	03,06	-0.1	0.1	%VFS
			"	"	1000 0000 0000	0111 1111 1111 "	"	"	E70	"	N and N+1, calculate the	04,07	-.025	.025	"
		99	"	"	0011 1111 1111	1100 0000 0000 "	"	"	E71	"	associated error in %VFS as	"	"	"	"
			"	"	0100 0000 0000	1011 1111 1111 "	"	"	E72	"	follows:	"	"	"	"
		100	"	"	0001 1111 1111	1110 0000 0000 "	"	"	E73	"	MCE = 10[(EB - EA)/100 - 0.002441]	"	"	"	"
			"	"	0010 0000 0000	1101 1111 1111 "	"	"	E74	"	Where:	"	"	"	"
		101	"	"	0000 1111 1111	1111 0000 0000 "	"	"	E75	"	EB = Measured value E70, E72,	"	"	"	"
			"	"	0001 0000 0000	1110 1111 1111 "	"	"	E76	"	E74, etc.	"	"	"	"
		102	"	"	0000 0111 1111	1111 1000 0000 "	"	"	E77	"		"	"	"	"
			"	"	" 1000 0000	" 0111 1111 "	"	"	E78	"	EA = Measured value E69, E71,	"	"	"	"
		103	"	"	" 0011 1111	" 1100 0000 "	"	"	E79	"	E73, etc.	"	"	"	"
			"	"	" 0100 0000	" 1011 1111 "	"	"	E80	"		"	"	"	"
		104	"	"	" 0001 1111	" 1110 0000 "	"	"	E81	"		"	"	"	"
			"	"	" 0010 0000	" 1101 1111 "	"	"	E82	"		"	"	"	"
		105	"	"	" 0000 1111	" 1111 0000 "	"	"	E83	"		"	"	"	"
			"	"	" 0001 0100	" 1110 1011 "	"	"	E84	"		"	"	"	"
		106	"	"	" 0000 0111	" 1111 1000 "	"	"	E85	"		"	"	"	"
			"	"	" 0000 1000	" 1111 0111 "	"	"	E86	"		"	"	"	"
		107	"	"	" 0000 0011	" 1111 1100 "	"	"	E87	"		"	"	"	"
			"	"	" 0000 0100	" 1111 1011 "	"	"	E88	"		"	"	"	"
		108	"	"	" 0000 0001	" 1111 1110 "	"	"	E89	"		"	"	"	"
			"	"	" 0000 0010	" 1111 1101 "	"	"	E90	"		"	"	"	"
		109	"	"	" 0000 0000	" 1111 1111 "	"	"	E91	"		"	"	"	"
			"	"	" 0000 0001	" 1111 1110 "	"	"	E92	"		"	"	"	"
2 T_A = 125°C		110 thru 218	Same tests, terminal conditions, and limits as for subgroup 1, tests 1 thru 109, except T_A = 125°C. Measured values are E93 to E184 and I31 to I61.												
3 T_A = -55°C		219 thru 327	Same tests, terminal conditions, and limits as for subgroup 1, tests 1 thru 109, except T_A = -55°C and I_{DD} = 2.5 mA for all conditions of V_{IL} and V_{IH}. Measured values are E185 to E276 and I62 to I92.												
7 T_A = 25°C	LE	328	+15 V	+10 V	0000 0000 0000	1111 1111 1111 1111	None	21	E277	V	For each input code N, calculate	03,06			
		329	"	"	0000 0000 0001	1111 1111 1110 "	"	"	E278	"	the corresponding linearity error	04,07			
			"	"	0000 0000 0010	1111 1111 1101 "	"	"		"	in %VFS.	"			
			"	"	...	... "	"	"		"		"			
			"	"			"	"		"		"			
			"	"	1111 1111 1101	0000 0000 0010 "	"	"		"	LE = 10[((EA/G1) + (N)(K) - (VOS))]	"			
			"	"	1111 1111 1110	0000 0000 0001 "	"	"		"	Where:	"			
			"	"	1111 1111 1111	0000 0000 0000 "	"	"		"	EA = Measured value E277	"			
					This subgroup checks all digital input codes.						thru E4372				
											N = DUT input digital code word in decimal form. Thus for 12 bits $N = (A1)2^{11} + (A2)2^{10} + \ldots + (A12)2^0$ A1, A2, ... A12 are 0 or 1.				
											K = Actual volts/count scale factor.				
											$K = (+d_{VFS} - VOS)/4095$ $+d_{VFS}$ = E4372/100				
											VOS = E277/100				
											Worst positive error	03,06	-	.05	%VFS
												04,07	-	0.12	"
											Worst positive code	03,06	-	-	OCT
												04,07	-	-	OCT
											Worst negative error	03,06	-.05	-	%VFS
												04,07	-.012	-	"
											Worst negative code	03,06	-	-	OCT
												04,07	-	-	"
8 T_A = 125°C	LE	330	Same tests, terminal conditions, and limits as for subgroup 7, tests 328 and 329, except T_A = 125°C.									03,06	-	.05	%VFS
												04,07	-	0.12	"
		331										03,06	-	-	OCT
												04,07	-	-	OCT
												03,06	-.05	-	%VFS
												04,07	-.012	-	"
												03,06	-	-	OCT
												04,07	-	-	"
	d_{VFS}/dt	332	Calculate d_{VFS}/dt = ($+d_{VFS}$ at 125°C - $+d_{VFS}$ at 25°C)/100°C from tests 143 and 34, respectively.									All	-10	10	ppm VFS/°C

TABLE III. Group A inspection for device types 03, 04, 06, and 07 - Continued.

Subgroup	Symbol	Test no.	Adapter pin numbers: 4	5	7 thru 18	22 thru 37	Energized relays	Measured pin: No.	Value	Unit	Equation	Device type	Limits: Min	Max	Unit
8 T_A = -55°C	LE	333 334	Same tests, terminal conditions, and limits as for subgroup 7, tests 328 and 329, except T_A = -55°C.									03,06 04,07 03,06 04,07 03,06 04,07 03,06 04,07	- - - - -.05 -.012 - -	.05 0.12 - - - - - -	%VFS " OCT OCT %VFS " OCT "
	d_{VFS}/dt	335	Calculate d_{VFS}/dt = ($^{+}d_{VFS}$ at -55°C - $^{+}d_{VFS}$ at 25°C)/80°C from tests 252 and 34, respectively.									All	-10	10	ppm VFS/°C
12 T_A = 25°C	FTE	336	V_{REF} = 20 Vpp at 100 kHz. All digital inputs = 0 V. See figure 7.					6	V1	mVpp	FTE = V1	03,04 06,07	-- --	10 25	mVpp mVpp
	t_{SLH}	337	All digital inputs switched simultaneously from logic low to logic high. For each device type, output settling is to within 1/2 LSB of the rated accuracy. See figure 8.					6	t1	µs	t_{SLH} = t1	All	---	1	µs
	t_{SHL}	338	All digital inputs switched simultaneously from logic high to logic low. For each device type, output settling is to within 1/2 LSB of the rated accuracy. See figure 8.					6	t2	µs	t_{SHL} = t2	All	---	1	µs
	C_o	339 340	All digital inputs set at V_{DD}. V_a = 100 mVpp at 1 MHz is applied thru a 1 kΩ resistor to the output under test. See figure 9.					6 7	V2 V3	mVpp mVpp	$C_o = 159\sqrt{((V_a/V_o)^2 - 1)} - C_o'$ Where: V_o = The measured output. C_o' = The fixture capacitance.	06,07 06,07 03,04	--- --- --- ---	200 300 100 75	pF " " " "
	C_o	341 324	All digital inputs set at 0 V. V_a = 100 mVpp at 1 MHz is applied thru a 1 kΩ resistor to the output under test. See figure 9.					6 7	V4 V5	mVpp mVpp	$C_o = 159\sqrt{((V_a/V_o)^2 - 1)} - C_o'$ Where: V_o = The measured output. C_o' = The fixture capacitance.	06,07 06,07 03,04	--- --- --- ---	75 100 300 200	pF " " " "

c. The percent defective allowable (PDA) for class S and class B devices shall be as specified in MIL-M-38510, based on failures from group A, subgroup 1 test after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. If interim electrical parameter tests are performed prior to burn-in, failures resulting from pre burn-in screening may be excluded from the PDA. If interim electrical parameter tests prior to burn-in are omitted, then all screening failures shall be included in the PDA. The verified failures of group A, subgroup 1 after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA for the applicable device class.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, 6, 9, 10, and 11 shall be omitted.

c. Subgroup 12 shall be added to group A inspection as specified in table III herein. The lot tolerance percent defective (LTPD) for subgroup 12 shall be 10 for all classes.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883 and as follows:

a. Electrical parameters shall be as specified in table II herein. For class S devices, delta limits shall apply only to subgroup 5 of group B inspection.

b. Steady state life test for class S devices shall be in accordance with table IIa of method 5005 of MIL-STD-883, using the circuit shown on figure 4. If the alternate burn-in conditions are used, the circuit shown on figure 5 shall be used.

TABLE IV. Group C delta limits T_A = 25°C.

Parameter	Device type		Unit
	01,02,03,05,06	04,07	
I_{ZS}	±50	±25	nA
$+d_{VFS}$, $-d_{VFS}$	±0.25	±0.25	%VFS

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein. Delta limits shall apply only to subgroup 1 of group C inspection for class B devices.

b. Steady state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A using the circuit shown on figure 5; or test condition D using the circuit shown on figure 4.

(2) T_A = 125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical parameters shall be as specified in table II herein. This group shall be measured only for initial qualification, and thereafter for group D tests at 25°C.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables. Electrical tests circuits as prescribed herein or in the referenced test methods of MIL-STD-883 shall be acceptable. Other test circuits shall require the approval of the qualifying activity.

4.5.1 Voltage and current. All voltage values given are referenced to the ground terminal of the device under test DUT. Currents given are conventional current and positive when flowing into the referenced terminal.

4.5.2 Life test and burn-in cooldown procedure. When devices are measured at 25°C following application of the steady-state life or burn-in test condition, they shall be cooled to within 10°C of their power stable condition prior to removal of the bias.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Ordering data. The contract or purchase order should specify the following:

a. Complete part number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inpection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, if applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of method 5003 of MIL-STD-883), corrective action, and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special carriers, lead lengths, or lead forming, if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requirements will not apply to direct purchase by or direct shipment to the Government.

h. Requirements for "JAN" marking.

6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and as follows:

BIT 1 - - - - - - - - - - -	Most significant bit = full scale /2.
BIT 2 - - - - - - - - - - -	2nd most significant bit = full scale /4.
BIT N - - - - - - - - - - -	Least significant bit for an N-bit converter.
CMOS - - - - - - - - - - -	Complementary metal oxide semiconductor.
$^{+}d_{VFS}$ - - - - - - - - - - -	Full-scale error between the DUT output voltage (I_{OUT1} * Rf) with V_{REF} = +10 V and a precision reference D/A. The reference D/A is assumed ideal and all error is charged against the DUT.
$^{-}d_{VFS}$ - - - - - - - - - - -	Same as $^{+}d_{VFS}$ except V_{REF} = -10 V.
d_{VFS}/dt - - - - - - - - - -	VFS drift with temperature expressed in ppm of VFS/°C.
FTE - - - - - - - - - - - -	Feedthrough error is input to output coupling when all of the bit switches are in the off state.
GND - - - - - - - - - - - -	Ground zero voltage potential.
I_{DD} - - - - - - - - - - - -	Current supplied to the V_{DD} terminal of the DUT for a given supply voltage (usually +15 V).
I_{OUT1} - - - - - - - - - - -	Sum of all R-2R ladder currents going through V_{IH} commanded switches.
I_{OUT2} - - - - - - - - - - -	Sum of all R-2R ladder currents going through V_{IL} commanded switches.
I_{REF}- - - - - - - - - - -	Current supplied to the V_{REF} terminal of the DUT with terminals IOUT1 and IOUT2 grounded.
I_{ZS} - - - - - - - - - - - -	Zero offset current through the IOUT1 terminal with V_{IL} applied to all bit inputs.
I_{ZS}'- - - - - - - - - - - -	Zero offset current through the IOUT2 terminal with V_{IH} applied to all bit inputs.
LE - - - - - - - - - - - -	Bit linearity error is the deviation between the output voltage and a point on a straight line passing through the zero to full scale end points for any digital input code. It can be expressed in mV for a 10 V input reference or in %VFS.

LSB - - - - - - - - - - - - Least significant bit = full scale /2expN.

MCE - - - - - - - - - - - - Major carry error is the differential linearity error at each of the major code transitions (i.e., from 11110000 to 11110111).

MSB - - - - - - - - - - - - Most significant digital input bit.

+PSS- - - - - - - - - - - - Change in full-scale output level for a change in power supply voltage expressed in ppm VFS/V. +PSS is for a positive one volt change.

-PSS- - - - - - - - - - - - Same as +PSS except -PSS is for a negative one volt change.

Rf- - - - - - - - - - - - - Feedback resistor for an external op amp.

V_{DD} - - - - - - - - - - - - Positive supply voltage (usually +15 V).

V_{IH} - - - - - - - - - - - - Digital high state input voltage.

V_{IL} - - - - - - - - - - - - Digital low state input voltage.

V_{REF}- - - - - - - - - - - - Analog reference input voltage.

6.4 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2) and lead material and finish C (see 3.3). Longer length leads and lead forming shall not affect the part number.

6.5 Substitutability. The cross-reference information below is presented for the convenience of users. Microcircuits covered by this specification will functionally replace the listed generic-industry type. Generic-industry microcircuit types may not have equivalent operational performance characteristics across military temperature ranges or reliability factors equivalent to MIL-M-38510 device types and may have slight physical variations in relation to case size. The presence of this information shall not be deemed as permitting substitution of generic-industry types for MIL-M-38510 types or as a waiver of any of the provisions of MIL-M-38510.

Military-device type	Generic-industry type
01	7523
02	7520
03	7521
04	7541
05	1020
06	1220
07	1218

6.6 Handling. MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static build-up. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surfaces.

b. Ground test equipment and tools.

c. Do not handle devices by the leads.

d. Store devices in conductive foam or carriers.

e. Avoid use of plastic, rubber, or silk in MOS areas.

f. Maintain relative humidity above 50 percent, if practical.

g. Unused logic inputs should be connected to logic high or logic low but not left open.

h. Disconnect all low impedance equipment and input signals from the device before switching off dc power supplies.

i. Switch off power supplies before inserting or removing devices from circuits.

6.7 Changes from previous issue. Asterisks are not used in this revision to identify changes with respect to the previous issue due to the extensiveness of the changes.

Custodian:
Army - ER
Navy - EC
Air Force - 17

Review activities:
Army - AR, MI
Navy - OS, SH
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Civil Agencies Coordinating Activities:
NASA - NA

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-0823)

(TO DETACH THIS FORM, CUT ALONG THIS LINE.)

STANDARDIZATION DOCUMENT IMPROVEMENT PROPOSAL

(See Instructions – Reverse Side)

1. DOCUMENT NUMBER	2. DOCUMENT TITLE
MIL-M-38510/127A	Microcircuits, Linear, CMOS Multiplying D/A Converters, Monolithic Silicon

3a. NAME OF SUBMITTING ORGANIZATION	4. TYPE OF ORGANIZATION *(Mark one)*
	☐ VENDOR
b. ADDRESS *(Street, City, State, ZIP Code)*	☐ USER
	☐ MANUFACTURER
	☐ OTHER *(Specify)*: _____

5. PROBLEM AREAS

a. Paragraph Number and Wording:

b. Recommended Wording:

c. Reason/Rationale for Recommendation:

6. REMARKS

7a. NAME OF SUBMITTER *(Last, First, MI)* – Optional	b. WORK TELEPHONE NUMBER *(Include Area Code)* – Optional
c. MAILING ADDRESS *(Street, City, State, ZIP Code)* – Optional	8. DATE OF SUBMISSION *(YYMMDD)*

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