ENGINEERING PRACTICES STUDY

TITLE: Engineering Practices Study to Develop Requirements and Verifications for Printed Boards Designed for Space and Launch Vehicle Applications.

01 October 2008

PROJECT NUMBER: 5998-2007-003

FINAL REPORT

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ATTCH 1

I. OBJECTIVES: To solicit input from custodians, review activities, users, and manufacturers on a proposed new specification sheet to MIL–PRF–31032 addressing printed boards designed to be used in outer space and on launch vehicles.

II. BACKGROUND: Printed boards designed and fabricated for outer space and use on launch vehicles are a small but important part of DoD applications. Currently, printed boards of this design and construction would have to be classified as a "custom" technology under QML–31032. They are classified as "custom" technology because many of the specialized acceptance, performance, and verification requirements that are unique to these designs are not covered in any of the existing MIL–PRF–31032 specification sheets. This proposed new specification sheet will attempt to classify and address the acceptance, performance, and verification requirements needed for printed boards designed and constructed for space and launch vehicle use. The following approach was used for this EP study:

a. All known "custom" technology requirements and verifications related to space and launch vehicle printed boards not covered in current MIL–PRF–31032 specification sheets were presented in a new specification sheet format. The unique "custom" requirements were highlighted in yellow to aid reviewers in determining the differences.

b. The military departments, users, and manufacturers were requested to review the attached proposed specification sheet. Any needed requirements or verifications that are not addressed in the proposed specification sheet were requested to be submitted for inclusion in the document.

III. RESULTS: Following the distribution of the EP Study with its attachment, comments from several activities were received. Their comments were incorporated into the draft and highlighted in green (new or additional material) and purple with strike-out text (material to be deleted).

IV. CONCLUSION: Upon completion of this study, a separate project should be initiated to create a new specification sheet for MIL–PRF–31032 using a scrubbed version (the highlighted colors and strike-out text sections removed) of the final engineering practices study attachment as the initial draft. This proposed initial draft should be circulated to the entire QML–31032 distribution list for review and comment.

V. RECOMMENDATION: This final EP study report will be forwarded to all agencies and parties both in military and industry who expressed interest to document the comments.

NOTE: This draft, dated 30 September 2008 prepared by DLA–CC, has not been approved and is subject to modification. DO NOT USE PRIOR TO APPROVAL. Attachment to PROJECT 5998–2007-003

METRIC

MIL–PRF–31032/SR
PROPOSAL

Additions or modifications from MIL-PRF-31032/1 are highlighted in yellow text.
Deletions from MIL-PRF-31032/1 are highlighted in red and strike-through text (e.g. ~~red text~~).
Additions or modifications from 26 June 2008 draft are highlighted in green text.
Deletions from 26 June 2008 draft are highlighted in purple and strike-through text (e.g. ~~purple text~~).

PERFORMANCE SPECIFICATION SHEET

PRINTED WIRING BOARD, RIGID, MULTILAYERED, FOR SPACE AND LAUNCH VEHICLE APPLICATIONS, WITH OR WITHOUT BLIND AND BURIED PLATED THROUGH HOLES, FOR SOLDERED PART MOUNTING

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-31032.

1. SCOPE

1.1 Scope. This specification sheet covers the performance requirements for rigid, multilayered (three or more conductor layers) printed wiring boards (hereafter designated printed board) with plated holes, that will use soldering for component/part mounting intended for use in outer space and other extreme environment applications (see 6.1.1). This specification sheet has four product levels as detailed in 1.2.1. Additional QM processes may be required when supplying complaint printed boards to this specification sheet (see 4.6 and appendix A).

1.2 Classification. Printed boards covered by this specification sheet are of classified by the following types, surface and knee continuous copper plating, and product levels, as specified (see 6.2).

1.2.1 Printed board type. Printed boards covered by this specification sheet are of the following types:

3 – Rigid multilayer board without blind or buried vias.

4 – Rigid multilayer board with blind and/or buried vias.

5 – Rigid multilayer board without blind and/or buried vias, with metal core or metal backing external heatsink.

6 – Rigid multilayer with blind and/or buried vias, with metal core or metal backing external heatsink.

1.2.2 ~~Surface and knee continuous~~ Copper wrap plating thickness. The ~~surface and knee continuous~~ copper wrap plating grade designation is defined by the amount of plated-through hole surface and knee continuous copper plating thickness remaining after surface processing. The grades are as follows:

A – Printed boards of this grade have 90 percent or more of the specified plated-through hole ~~surface and knee continuous~~ copper wrap plating thickness on the surface and knee after surface processing.

B – Printed boards of this grade have 50 percent or more of the specified plated-through hole ~~surface and knee continuous~~ copper wrap plating thickness on the surface and knee after surface processing.

C – Printed boards of this grade have 25 percent or more of the specified plated-through hole ~~surface and knee continuous~~ copper wrap plating thickness on the surface and knee after surface processing.

Comments, suggestions, or questions on this document should be addressed to: Defense Supply Center, Columbus, ATTN: DSCC/VAC, P. O. Box 3990, Columbus, OH 43218-3990 or emailed to 5998.Documents@dscc.dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at http://assist.daps.dla.mil/.

1.2.3 Product level. This specification sheet makes provision for four product levels. The product level is identified by a single letter. Three of these product levels, in lowest to highest order, S, T, and E, are as defined below and in appendix A. The fourth product level, level C, is a custom product level defined in appendix B and whose requirements are detailed in the printed board procurement documentation.

Product level S – Product level S covers high reliability space applications.

Product level T – Product level T covers high reliability space applications with additional testing and assurance.

Product level E – Product level E covers extreme purpose applications.

Product level C – Product level C covers printed boards for custom applications which are based upon one of the other product levels (S, T, or E) with either exceptions taken to the requirements of that level or with additional requirements and verifications added (see appendix B). See table IV for a summary of differences between the different product levels.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, or handbooks. The following specifications, standards, or handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 – Electronic and Electrical Component Parts

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA).

NASA 1124 – Outgassing Data for Selecting Spacecraft Materials.

(Hard copies of this document are no longer available from NASA or DAPS. This information is only available at http://outgassing.nasa.gov.

2.3 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

~~ASTM B487~~	~~–~~	~~Standard Test Method for Measurement of Metal and Oxide Coating Thicknesses by Microscopical Examination of a Cross Section.~~
ASTM B567	–	Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
ASTM B568	–	Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.
ASTM E53	–	Standard Test Method for Determination of Copper in Unalloyed Copper by Gravimetry.
ASTM E345	–	Standard Test Methods of Tension Testing of Metallic Foil.
ASTM E595	–	Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment.

(Copies of this document are available online at http://www.astm.org or from the ASTM International, 100 Barr Harbor Drive, P. O. Box C700, West Conshohocken. PA 19428-2959).

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-T-50	–	Terms and Definitions for Interconnecting and Packaging Electronic Circuits.
IPC-A-600	–	Acceptability of Printed Boards.
IPC-OI-645	–	Standard for Visual Optical Inspection Aids.
IPC-TM-650	–	Test Methods Manual.
~~IPC-CC-830~~	~~–~~	~~Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies.~~
IPC-2220	–	2220 Series of Design Documents.
IPC-2221	–	Generic Standard on Printed Board Design.
IPC-2222	–	Sectional Design Standard for Rigid Organic Printed Boards.
~~IPC-7905~~ IPC-7095	–	Design and Assembly Process Implementation for BGAs.
IPC-9252	–	Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards.
J-STD-003	–	Solderability Tests for Printed Boards.

(Copies of this document are available online at http://www.ipc.org or from the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015–1249).

(Non–Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Printed board detail requirements. Printed boards delivered under this specification sheet shall be in accordance with the requirements as specified herein, and documented in the printed board procurement documentation.

3.1.1 Conflicting requirements. The order of precedence of conflicting requirements shall be in accordance with 2HMIL-PRF-31032.

3.1.2 Reference to printed board procurement documentation. For the purposes of this specification sheet, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable printed board procurement documentation.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in IPC-T-50 and those contained herein.

3.2 Qualification. Printed boards furnished under this specification sheet shall be technologies that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see 4.2 and 6.3).

3.2.1 Validation (certification). Validation of a manufacturing line for production of printed boards for use in space systems shall be accomplished by a team headed by DSCC with observers solicited from NASA, Air Force Space and Missiles Center, the services, and customers.

3.2.2 QML line shutdown. If an extended period of non-production or unscheduled shutdown of a QML certified/qualified flow is necessary, the TRB shall assess and ensure that the process is still capable when production is resumed or retarted. The TRB shall create a plan for restarting the production line and this plan shall be reviewed by the qualifying activity prior to implementation.

3.3 Design (see 3.1 and 6.2). Printed boards shall be of the design specified. Unless otherwise noted herein, if individual design parameters are not specified in the printed board procurement documentation, then the baseline design parameters shall be as specified in appendix C, IPC-2221 and IPC-2222, performance class 3. Test coupons design shall be as specified in the applicable design standard and shall reflect worst–case design conditions of the printed boards that they represent. Test coupon quantity and placement shall be as specified in appendix A. Additional test coupons will be needed for product levels T and E, and may be needed for product level C for correlation and design verification purposes (see appendices A and B).

3.4 Printed board materials. All materials used in the construction of compliant printed boards shall comply with the applicable specifications referenced in the printed board procurement documentation. If materials used in the production of printed boards are not specified, then it is the manufacturer's responsibility to use materials which will meet the performance requirements of this specification sheet. Acceptance or approval of any printed board material shall not be construed as a guarantee of the acceptance of the completed printed board.

3.4.1 Prohibited materials (see 6.5). Lead-free tin (which includes electroplated tin and immersion tin) and electroplated silver shall not be used as a finish either externally, internally, or as an undercoat. Lead-free tin is any tin or tin alloy containing more than 97 percent tin. The use of tin-lead (Sn-Pb) finishes is acceptable provided that the minimum lead content is greater than 3 percent.

3.4.2 Metals. Metal surfaces shall be corrosion resistant or shall be plated or treated to resist corrosion. Metal surfaces to be used for component attachment shall meet the requirements specified in 3.7.4.5.

3.5 Visual and dimensional requirements. Printed board test specimens (the finished printed boards, unfinished internal layers, and supporting test coupons, as applicable) shall conform to the requirements specified in 3.5.1 through 3.5.4. After solder ~~resist~~ mask application, the printed board test specimens shall also conform to the requirements of 3.5.4 through 3.5.5. Scratches, dents, and tool marks shall not bridge or expose signal conductors, expose base metal, expose or disrupt reinforcement fibers, reduce dielectric properties and spacing below minimum requirements. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of externally observable accept/reject conditions of test specimens.

3.5.1 Base material.

3.5.1.1 Edges of base material. Burrs, chips, ~~delaminations,~~, haloing, nicks, and other penetrations along the base material edges of completed printed boards shall be acceptable provided the ~~defect~~ imperfection does not reduce the edge spacing specified by more than 50 percent. If no edge spacing requirement is specified, the imperfection penetration shall not exceed 2.5 mm (.0984 inch). Base material edges include the external edge of the printed board, the edges of cutouts, and the edges of non-plated through holes. Loose metallic burrs shall not be acceptable.

3.5.1.2 Surface appearance. There shall be no resin starved or scorched areas, reinforcement exposure, foreign materials, blistering, or other visual defects detrimental to the performance of the base material. Localized concentration of these defects may occur, but they shall be no closer than 6.5 mm (.26 inch) to any conductor. Unless otherwise specified, reinforcement texture and reinforcement areas exposed by mechanical fabrication operations are acceptable.

3.5.1.3 Surface imperfections. Imperfections in the surface of the base material such as blistering, burrs, cuts, ~~dents, exposed reinforcement material fibers~~, foreign materials, gouges, nicks, pits, resin scorched areas, resin starved areas, scratches, tool marks, voids, or other visual defects detrimental to the performance of the base material shall be acceptable in localized concentrations providing the following conditions are met:

a. The imperfections (except for weave texture) do not bridge between conductors.

b. The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimum conductor spacing requirements.

c. The base material reinforcement material (woven or non-woven) is not cut, disrupted, disturbed, or exposed. Weave exposure shall not be acceptable.

d. Surface voids shall be acceptable provided they do not exceed 0.8 mm (.031 inch) in the longest dimension; bridge conductors; or exceed 5 percent of the total printed board area per side.

3.5.1.3.1 Exposed or disrupted fibers. Exposed or disrupted fibers shall not bridge conductors and shall not reduce the conductor spacing below the minimum conductor spacing requirements.

3.5.1.3.2 Surface pits and voids. Surface pits and voids in the base material shall be acceptable providing the following conditions are met:

a. Surface voids are no bigger than 0.8 mm (.031 inch) in the longest dimension

b. The surface voids do not bridge conductors.

c. The total area of all surface voids does not exceed 5 percent of the total printed board area.

d. The surface void does not affect the performance of the base material.

3.5.1.4 Subsurface imperfections. Subsurface imperfections (such as crazing, ~~blistering, delamination,~~ foreign inclusions, ~~haloing~~, and laminate voids~~, etc.~~) shall be acceptable providing the following conditions are met:

a. The imperfections do not reduce conductor spacing or dielectric spacing between adjacent conductors that are not electrically common below the specified minimum requirements. If no minimum is specified, the imperfection does not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed wiring board area on each side shall be affected.

b. The imperfections do not propagate as a result of testing (such as rework simulation, ~~solder float thermal stress~~ resistance to soldering heat, or thermal ~~shock~~ cycling).

c. The longest dimension of any single imperfection is no greater than 0.80 mm (.032 inch). In non–circuitry areas, the maximum size shall not be greater than 2.00 mm (.079 inch) in the longest dimension or 0.01 percent of the printed board area, maximum.

d. Color variations or mottled appearance in bond enhancement treatments shall be acceptable. Random missing areas of treatment shall not exceed 10 percent of the total conductor surface area of the affected layer.

e. Blistering, delamination, and haloing shall be acceptable providing that the longest dimension of any single imperfection is no greater than 0.08 mm (.003 inch).

3.5.1.5 Foreign inclusions. Foreign inclusions shall be permitted when they meet the following:

a. The foreign inclusions are translucent and trapped within the base material. Opaque foreign inclusions shall not be acceptable.

b. The foreign inclusion shall not bridge adjacent conductors.

c. The foreign inclusion does not reduce the dielectric spacing between adjacent conductors to below the minimum conductor spacing specified. If not specified, the inclusion does not reduce the conductor spacing by more than 50 percent or 0.125 mm (.005 inch), whichever is less.

d. The foreign inclusions longest dimension is no greater than .0.8 mm (.032 inch) in circuitry areas. Inclusions in non-circuitry areas have no maximum dimension requirement.

e. If the base material specification allows for more or larger inclusions, those inclusions are allowed in the finished printed board, up to the size and quantity defined by the base material specification provided that the inclusion does not violate the conductor spacing requirements of 3.5.1.2.

3.5.2 Conductor pattern.

3.5.2.1 Annular ring, external. The minimum external annular ring limit shall be as specified in appendix C. Unless already at the specified minimum limit, ~~the external annular ring may have, in isolated areas,~~ a 20 percent reduction of the specified external annular ring due to defects such as pits, dents, nicks, pinholes, or splay, in isolated areas, shall be acceptable. Note: Buried vias are considered to be an external layer and are assessed in-process before multilayer lamination.

3.5.2.2 Bonding of conductor to base material and lifted lands. There shall be no peeling or lifting of any land or conductor patterns from the base material. The completed printed board shall not exhibit any lifted land. (NOTE: See 3.6.7 for allowances for the acceptable lifting of terminal pads, i.e. lifted lands, following the ~~solder float thermal stress~~ resistance to soldering heat, rework simulation, and thermal ~~shock~~ cycling testing.)

3.5.2.3 Conductor finish. The conductor finish shall be as specified. Unless otherwise specified, the following requirements shall apply.

3.5.2.3.1 Coverage. Unless otherwise specified herein, conductor finish shall ~~completely~~ cover the exposed conductor pattern. Complete coverage does not apply to the vertical conductor edges.

3.5.2.3.1.1 Edge board contacts. Unless otherwise specified, these requirements apply to the critical contact area. The critical contact area for edge board contacts shall be as specified.

a. Defects or surface imperfections in the edge board contact finish shall not expose base metal in critical contact area.

b. There shall be no nodules or metal bumps in the edge board contact finish in the critical contact area.

c. Pits, dents, or depressions in the edge board contact finish shall not exceed 0.15 mm (.0059 inch) in their longest dimension. There shall be no more than three occurrences for each edge board contact, and no more than 30 percent of the contacts shall be affected.

3.5.2.3.1.2 Plating junctions. Unless otherwise specified, these requirements apply to all junctions of different platings or coatings.

a. There shall be no exposed copper in the junction of metallic platings or coatings.

b. An overlap of metallic platings or coatings shall be acceptable if it is no greater than 0.8 mm (.032 inch) in length.

c. When both solder coating and gold plating are present at a plating junction, a discolored or gray-black area at that plating overlap zone shall be acceptable.

3.5.2.3.2 Conductor finish plating and coating voids in plated–through holes. Any plating and coating voids in the conductor finish shall not exceed the following limits:

a. No more than one void in any plated–through hole.

b. Not more than 5 percent of the plated–through holes shall have voids.

c. Any void present is not more than 5 percent of the plated–through holes length.

d. Any void present is less than 90 degrees of the circumference of the plated–through hole.

3.5.2.3.3 Whiskers. There shall be no whiskers of solder or other platings on the surface of the conductor pattern.

3.5.2.4 Component mounting. Imperfections on surface mount lands or wire bond pads shall not exceed the requirements specified herein.

3.5.2.4.1 Rectangular surface mount lands. Defects such as nicks, dents, and pin holes along the external edge of the land shall not exceed 20 percent of either the length or width of the land and shall not encroach the pristine area, which is defined by the central 80 percent of the land width by 80 percent of the land length as shown on figure 1. Defects internal to the land shall not exceed 10 percent of the length or width of the land and shall remain outside of the pristine area of the surface mount land. One electrical test probe ‘‘witness’’ mark is allowed within the pristine area.

3.5.2.4.2 Round surface mount lands (ball grid arrau [BGA] pads). Defects such as nick, dents and pin holes along the edge of the land shall not radially extend towards the center of the land by more than 10 percent of the diameter of the land and shall not extend more than 20 percent around the circumference of the land as shown on figure 2. There shall be no defects within the pristine area which is defined by the central 80 percent of the land diameter. One electrical test probe ‘‘witness’’ mark is allowed within the pristine area.

3.5.2.4.3 Wire bond pads. The maximum conductor finish roughness (surface roughness) for pads or areas designated for wire bonding shall be no greater than 0.8 micrometers (32 micro inches). Unless otherwise specified, the wire bond pad bonding area shall be defined as the pristine area as shown on figure 1 for rectangular pads or on figure 2 for round pads. There shall be no pits, nodules, scratches, electrical test probe ‘‘witness’’ marks, or other defects in the pristine area that exceed the surface roughness limits.

3.5.2.5 Conductor pattern imperfections (see figure 3). The conductor pattern shall contain no cracks, splits, or tears. Unless otherwise specified, any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce each conductor width by more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent reductions greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less. Unless otherwise specified, the length of any imperfection shall not exceed the design width of the conductor. Imperfections that penetrate more than 20 percent of the conductor thickness shall be unacceptable.

3.5.2.5.1 Cuts and scratches. A scratch of any length or width is permissible on ground or voltage planes, provided the dielectric is not exposed. Scratches on non-critical conductors may be of any length, but no deeper than 20 percent of the total conductor thickness.

3.5.2.5.2 Dents. A dent of any length or width on ground planes shall be acceptable provided the clad surface is not torn. Dents on conductive patterns may be of any length, but no deeper than 0.013 mm (.0005 inch).

3.5.2.5.3 Pinholes. Pinholes in ground or voltage planes in non-critical areas shall be acceptable provided they have no single diameter greater than 0.5 mm (.0197 inch) and do not exceed three for each 25 mm (1 inch) diameter. A pinhole in a conductive pattern shall be acceptable, provided they do not reduce the width of a conductive pattern by 10 percent. Pinholes shall be limited to no more than one for each 25 mm (1 inch) of conductive length.

3.5.2.5.4 Pits. Pits in ground or voltage planes shall be acceptable provided they do not exceed 25 percent of the surface area. Any pit in the conductive pattern is acceptable provided the outline dimension does not exceed 10 percent of the conductor width, and there is no more than one pit for each 25 mm (1 inch) of the conductor length.

3.5.2.5.5 Superfluous metal. Unless otherwise specified, small particles of metal such as residual copper or subsequent plating after etching which remain affixed to areas that are intended to be free of conductive material shall be acceptable providing the following conditions are met:

a. The superfluous metal are no closer than 6.4 mm (.25 inch) to any conductor.

b. The superfluous metal are smaller than 0.13 mm (.005 inch) at their greatest diameter.

3.5.2.6 Conductor spacing. Conductor spacing shall be as specified.

3.5.2.7 Conductor width. Conductor width shall be as specified.

3.5.2.8 Width and spacing imperfections.

3.5.2.8.1 Critical-controlled signal conductor width imperfections. Unless otherwise specified, conductor width imperfections on direct opposite sides of a critical-controlled signal conductor, when combined, shall not exceed 10 percent of the specified conductor width. A single conductor width deviation along any 25 mm (1 inch) segment of a specified critical-controlled signal conductor shall be acceptable. The maximum length of any conductor width imperfection shall be no greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.8.2 Critical-controlled signal conductor spacing imperfections. Unless otherwise specified, isolated protrusions on multiple critical controlled signal conductors shall not exceed 10 percent of the specified spacing. Unless otherwise specified, conductor protrusions in proximity of, or directly opposite to, adjacent conductor protrusions shall not reduce the specified spacing by more than 10 percent. A single such protrusion is allowed along any 25 mm (1 inch) segment of the signal conductor pattern with width specified. The maximum length of any conductor protrusions shall be no greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.8.3 Non-critical conductor pattern width imperfections. The conductor pattern shall contain no cracks, splits, or tears. Any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce non-critical conductor widths by more than 20 percent. There shall be no occurrence of the acceptable reductions greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.3 Interface and physical dimension requirements. The printed boards shall meet the interface and physical dimensions specified. The dimensional requirements includes items such as cutouts, overall thickness, periphery, and other design features as specified. In the event that a dimensional characteristics is not specified, the applicable class 3 of IPC-2221 design default for that characteristic shall apply.

3.5.3.1 Ball grid array (BGA) lands. BGA lands using copper–defined lands, solder ~~resist~~ mask-defined lands, or solder dam designs shall comply with ~~IPC-7905~~ IPC-7905.

3.5.3.2 Conductor pattern feature accuracy. Conductor pattern feature accuracy shall be as specified.

3.5.3.3 Edge board contacts edge condition. The end or beveled edge of edge board contacts shall be smooth with no burrs, roughness, or lifted plating. There shall be no separation of the edge board contacts from the base material or any loose fibers on the beveled edge. Exposed copper on the end or beveled edge of the edge board contact shall be acceptable. Conductor finish plating or coating shall comply with the requirements of 3.5.2.3.

3.5.3.4 Hole pattern accuracy. The size and location of the hole pattern in the printed board shall be as specified.

3.5.3.5 Hole size. The hole size and tolerance shall be as specified. Unless otherwise specified, hole size tolerance shall be applied after plating. Only specific dimensioned holes, to include both nonplated–through and plated–through, shall be inspected for hole pattern accuracy to meet board dimensional requirements of 3.5.3.2. Nodules or rough plating in plated–through holes shall not reduce the hole diameter below the minimum limits specified.

3.5.4 Solder ~~resist~~ mask. The cured solder ~~resist~~ mask shall not exhibit any chalking, crazing, peeling, skipping, softening, swelling, or wrinkles in excess of the limits specified herein. Unless otherwise specified, the following solder ~~resist~~ mask conditions ~~below~~ shall apply.

3.5.4.1 Coverage. Solder ~~resist~~ mask coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the following conditions are met:

a. The solder ~~resist~~ mask coverage imperfection shall not expose two adjacent electrically isolated lands or conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.

b. In areas containing parallel conductors, the solder ~~resist~~ mask coverage imperfection shall not expose two adjacent isolated conductors whose spacing is less than 0.5 mm (.02 inch) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.

c. The exposed conductor(s) shall not be bare copper.

d. The solder ~~resist~~ mask coverage imperfection does not expose ~~tented via~~ plated-through holes required to be tented.

e. There shall be no visible soda straw voids between the solder ~~resist~~ mask and the printed board base material surface and the edges of the conductor patterns.

3.5.4.2 BGA lands. BGA lands using copper–defined lands, solder ~~resist~~ mask -defined lands, or solder dam designs shall comply with the class 3, “acceptable” conditions of IPC-A-600.

3.5.4.3 Discoloration. Discoloration of metallic surfaces under the cured solder ~~resist~~ mask is acceptable.

3.5.4.4 Registration. The solder ~~resist~~ mask shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified. If no requirements are specified, the following apply:

a. Unless otherwise specified, solder ~~resist~~ mask shall not encroach onto surface mount lands.

b. Solder ~~resist~~ mask misregistration onto component plated–through hole lands (plated–through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements. Misregistration shall not expose adjacent, electrically isolated lands or conductors.

c. Solder ~~resist~~ mask shall not encroach into plated–through hole barrels or onto other surface features (such as edge board contacts ~~connector fingers~~ or lands of unplated holes) to which solder connections will be made.

d. Solder ~~resist~~ mask is permitted in vias or plated–through holes in which no lead is to be soldered.

e. Test points which are intended for assembly testing shall be free of solder ~~resist~~ mask unless a partial coverage allowance is specified.

f. On areas where the conductor pattern continues under solder ~~resist~~ mask, there shall be no exposed copper at the conductor finish to solder ~~resist~~ mask interface. Unless otherwise specified, conductor finish plating or coating may extend 0.25 mm (.00984 inch) maximum under the edge of the solder ~~resist~~ mask.

g. Unless otherwise specified, solder ~~resist~~ mask encroachment onto surface mount lands shall comply with the following:

(1) On surface mount lands with a pitch of 1.25 mm (.05 inch) or greater, encroachment is on one side of the land only and does not exceed 0.05 mm (.002 inch).

(2) On surface mount lands with a pitch less than 1.25 mm (.05 inch), encroachment is on one side of the land only and does not exceed 0.025 mm (.000984 inch).

3.5.4.5 Thickness. Solder ~~resist~~ mask thickness shall be as specified.

3.5.4.6 Solder ~~resist~~ mask cure. The cured solder ~~resist~~ mask coating shall not exhibit tackiness, blistering, or delamination.

3.5.4.7 Soda straw voids. There shall be no visible soda straw voids between the solder ~~resist~~ mask and the printed board base material surface and the edges of the conductor patterns.

3.5.5 Plated–through holes (external visual). There shall be no evidence of exposed copper, lifted lands, or plating voids. Plating nodules shall be acceptable provided they do not reduce the hole diameter below the minimum hole diameter specified.

3.6 Plated–through hole structural requirements. Vertical cross sections of printed board test specimens (production printed boards or test coupons) shall conform to the requirements in 3.6.1 through ~~3.6.10~~ 3.6.9 , as applicable (see figures 4 through ~~6~~ 15). Vias (see 6.4) shall meet the requirements of plated–through holes. Butt plating joints, circumferential separations, corner cracks, and cracked copper plating shall not be acceptable. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of cross sectioned test specimens.

3.6.1 Base material.

3.6.1.1 Delamination. Printed wiring boards shall have no delaminations.

3.6.1.2 Dielectric thickness.

3.6.1.2.1 Dielectric layer thickness (see ~~figure 6~~ figure 4). The minimum dielectric thickness separating the conductor layers of the printed wiring boards shall be as specified (see A.3.1.1). If not specified on the master drawing, the minimum dielectric spacing base materials should not be less than the value specified in the IPC's 2220 series of documents for the design of rigid printed boards. On the date of publication of this document, the minimum dielectric spacing dimension for rigid base materials shall not be less .0035 inch (0.089 mm).

3.6.1.2.2 Heatsink plane hole fill material (see ~~figure A–7~~ figure 5 and 6). Defects such as radial cracks, wicking, or voids in the dielectric material used to insulate a heatsink plane or metal core from circuitry and plated through holes shall not reduce by 75 percent the specified lateral spacing between adjacent conductive surfaces. If not specified on the master drawing, the minimum lateral spacing between adjacent conductive surfaces, nonfunctional lands, or plated-through hole and the heatsink plane should not be less than the value specified in the IPC's 2220 series of documents for the design of rigid printed boards. On the date of publication of this document, the minimum d lateral spacing for heatsink planes shall not be less than 0.10 mm (.004 inch). Wicking of copper and radial cracks from the plated–through hole edge into the hole–fill insulation material shall not exceed 0.076 mm (.003 inch).

3.6.1.3 Laminate cracks and voids (see ~~figure 4~~ figure 7). Laminate voids with the longest dimension of 0.08 mm (.003 inch) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified. After undergoing rework simulation (see 3.7.4.5), ~~solder float thermal stress~~ resistance to soldering heat (see 3.7.6.2) or thermal ~~shock~~ cycling (see 3.7.6.3), laminate voids are not evaluated in zone A (see figure 4).

3.6.1.3.1 As received condition. Laminate cracks and voids located wholly or partially in zones A or B shall not be acceptable.

3.6.1.3.2 After stress condition. Laminate cracks and voids in zone B shall not exceed a length of 0.08 mm (.003 inch), shall not bridge adjacent uncommon conductors, and shall not reduce dielectric spacing, either laterally or vertically, below the specified minimum. Multiple laminate cracks and voids located between two adjacent plated-through holes or vias in the same plane shall not have a combined length in excess of 0.08 mm (.003 inch), shall not bridge adjacent uncommon conductors, and shall not reduce dielectric spacing, either vertically or horizontally, below the minimum specified spacing.

3.6.1.4 Resin recession (see figure 7).

3.6.1.4.1 Stressed specimens (after rework simulation, ~~solder float thermal stress~~ resistance to soldering heat, or thermal ~~shock~~ cycling testing). Resin recession at the outer surface of the plated hole barrel shall be permitted and is not cause for rejection.

3.6.1.4.2 Non-stressed specimens. Resin recession at the outer surface of the plated hole barrel wall shall be permitted provided the maximum depth as measured from the barrel wall does not exceed 0.08 mm (.003 inch) and the resin recession on any side of the plated-through hole does not exceed 40 percent of the cumulative base material thickness (sum of the dielectric layer thickness being evaluated) on the side of the plated-through hole being evaluated.

3.6.1.5 Via fill of blind and buried vias. Unless otherwise specified, the fill requirements for blind vias shall be 75 percent minimum. Unless otherwise specified, buried vias shall be at least 95 percent filled with the laminating resin or similar via filling material.

3.6.2 Conductor finish. A conductor finish plating or coating material shall be used that enables the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified, the conductor finish conditions specified below shall apply.

3.6.2.1 Dewetting. For tin alloys, reflowed tin-lead, or solder coated surfaces, dewetting is not permitted on any conductive surface where a solder connection will be required. Dewetting on conductors, ground, or voltage planes shall meet the requirements of J-STD-003.

3.6.2.2 Nonwetting. For tin alloys, reflowed tin-lead, solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required.

3.6.2.3 Outgrowth and overhang. There shall be no outgrowth on the conductor edges when finished with fused tin-lead or solder coating. The maximum permissible outgrowth on conductor edges finished with surface finish metals other than tin-lead or solder shall be 0.025 mm (.001 inch).

3.6.2.4 Thickness (plating or coating). The plating or coating thickness of the conductor finish shall be as specified. Voids in any conductor finish plating coating shall meet the requirements of 3.6.2.1.

3.6.2.5 Protective finishes for internal metal cores. The plating, coating, or surface treatment type and thickness of internal metal cores materials shall be as specified (see 3.1).

3.6.3 Conductor thickness. The conductor thickness shall be as specified.

3.6.3.1 Minimum thickness of copper foil with copper plating (external and internal for sequential laminated multilayer designs). When a conductor thickness is specified, the conductor thickness (copper foil and copper plating) shall be equal to or greater than the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (copper foil and copper plating) shall be within the specified tolerance for the specified thickness. If only a starting copper foil weight requirement is specified, the thickness limits for conductors with plating shall meet the class 3 requirements for "External conductor thickness after plating" table of IPC-2221. If only final copper foil weight requirement is specified, the limits for minimum conductor thickness shall be as defined by the procuring activity. The minimum continuous hole-knee-surface copper thickness shall be as specified (see 1.2.2)

3.6.3.2 Minimum thickness of copper foil (without plating) (internal on multilayer designs). When a minimum conductor thickness is specified, the conductor thickness (copper foil) shall be equal to or greater than the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (copper foil) shall be within the specified tolerance for the specified thickness. If only a starting copper foil weight requirement is specified, the limits for minimum internal layer foil thickness after processing shall be in accordance with "Internal layer foil thickness after processing" table of IPC-2221.

3.6.4 Conductor width. The conductor thickness shall be as specified.

3.6.4.1 Annular ring, internal. The minimum internal annular ring shall be as specified in appendix C.

3.6.4.2 Undercutting. Undercutting at the edge of conductors shall not exceed the total thickness of the copper foil and plated copper, or 10 percent of the conductor width, whichever is least.

3.6.5 Hole preparation prior to metalization. The internal conductors of drilled holes shall be processed to remove resin smear. When etchback is not specified, drilled holes shall be desmeared.

3.6.5.1 Desmear (resin smear removal). Desmear shall not remove more than 0.025 mm (.001 inch) of base material from the hole walls. Random tears or drill gouges which produce isolated areas where the smear removal depth limit is exceeded shall not be cause for rejection.

3.6.5.2 Etchback (when specified, see 3.1) (see figures ~~6 and 7~~ 8 and 9). When specified for multilayered designs, production panels shall be etched back for the lateral removal of base material (resin, reinforcement material, etc.) from the drilled hole walls and internal conductors prior to plating. Unless otherwise specified, the positive etchback shall be a minimum of 0.005 mm (.0002 inch) and no greater than the specified minimum internal annular ring or 0.04 mm (.0016 inch), whichever is less, with a preferred depth of 0.013 mm (.0005 inch) when measured at the internal copper contact area protrusion. The etchback shall be effective on at least the top or bottom (or both) surface of each internal conductor to provide at least a two point contact with the subsequent hole plating. Negative etchback is not acceptable when etchback is specified. Wicking shall meet the requirements of 3.6.8.5.

3.6.6 Lifted lands (see figure ~~8~~ 10).

3.6.6.1 Non-stressed specimens (as received condition). There shall be no lifted lands on the as received test specimen. When inspected in accordance with 4.7.2.1 and lifted lands are present, the lot shall be 100 percent visually inspected in accordance with 4.7.1 for separation of the lands from the base material.

3.6.6.2 Stressed specimens (After rework simulation, ~~solder float thermal stress~~, or thermal ~~shock~~ cycling testing). After undergoing rework simulation (see 3.7.4.5), ~~solder float thermal stress~~ resistance to soldering heat (see 3.7.6.2), or thermal ~~shock~~ cycling (see 3.7.6.3), the maximum allowed distance from the base material surface to the bottom of the outer lower edge of the lifted land or pad shall be no greater than the total land thickness. The total land thickness is equal to the combined thickness of the metal foil and any copper plating on that land.

3.6.7 Metallic cracks. There shall be no cracks in the platings, coatings, or conductive foils (internal or external). ~~Cracks are permissible in the external layer (outer) copper foil provided they do not extend into the plated copper.~~

3.6.8 Plated–through hole ~~wall~~ and via copper plating. Copper plating thickness applies to the hole wall, the surface land, and the knee of plated–through holes and vias.

3.6.8.1 Copper plating thickness. Unless otherwise specified, the copper plating thickness in plated–through holes, including the land surface and knee of the hole, shall be in accordance with appendix C. Any hole wall copper plating thickness less than ~~80~~ 90 percent of the specified thickness shall be treated as a void. Unless otherwise specified, the plated–through hole surface and knee continuous copper plating (wrapped around plating) thickness shall not be reduced by more than 50 percent of the specified copper plating thickness due to planarization or other processing (see figures 7, 8, and 9).

3.6.8.1.1 Copper plating voids. There shall be no copper plating voids, regardless of length or size. There shall be no plating voids evident at the interface of any conductive layer and plated–through hole wall. Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated–through hole exhibiting this condition shall be counted as having one void for panel acceptance purposes.

3.6.8.2 Copper plating defects. Nodules, plating folds, plating inclusions, or plated reinforcement material protrusions that project into the hole wall copper plating ~~plated-through-hole~~ shall be acceptable provided that the hole diameter and the plated copper thickness are not reduced below their specified limits.

3.6.8.3 Conductive interface separations. The term conductive interfaces shall be used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of copper or metal foil. The interface between platings and coating (electroless copper, direct metallization copper, and non–electroless electroless copper substitutes, and electrolytic copper, whether panel or pattern plated) shall also be considered a conductive interface.

3.6.8.3.1 Copper to copper interfaces. There shall be no separations or contamination between the hole wall conductive interfaces.

3.6.8.3.2 Dissimilar metal interfaces. On metal core boards with dissimilar metals, contamination at the conductive interface shall not exceed 20 percent of the thickness of the dissimilar metal. Conductive interface separations along the vertical edge of non–copper metals such as copper–invar–copper shall be acceptable to 20 percent of their thickness.

3.6.8.3.3 Plated barrel to hole wall dielectric separation. There shall be no separations between the plated–through hole barrel and dielectric wall or resin recession in the as received test specimens. Resin recession greater than 0.08 mm (.003 inch) depth or more than 40 percent of cumulative dielectric thickness shall be acceptable in the post stress test specimens.

3.6.8.4 Miscellaneous hole wall deficiencies. Nodules, burrs, plating folds, or plated reinforcement material fibers that project into the copper plating shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below their specified limits.

3.6.8.5 Wicking. Wicking of copper plating extending ~~0.08 mm (.003 inch)~~ 0.05 mm (.002 inch) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified.

3.6.9 Solder ~~resist~~ mask thickness. The minimum solder ~~resist~~ mask thickness shall be as specified.

3.7 Performance requirements. The performance requirements specified in 3.7.1 through 3.7.6.4 shall be verified by the test methods detailed in 4.7. Unless otherwise specified by the Technical Review Board (TRB), test optimization in accordance with MIL-PRF-31032 may be used on products levels S and T, but the printed boards shall meet all of the performance requirements specified and herein, regardless of the verification method used.

3.7.1 Acceptability (visual and dimensional acceptability of printed boards). When examined as specified in 4.7.1, the printed boards shall conform to the acceptance requirements specified in 3.3 (design), 3.4 (material), 3.5 (external visual and dimensional), 3.8 (marking), 3.9 (traceability), and 3.11 (workmanship), inclusive.

3.7.2 Destructive physical analysis (DPA) by microsectioning of printed board test specimens.

3.7.2.1 Vertical cross sections (via microsectioning). When printed board test specimens (completed printed boards, supporting test coupons, or qualification test specimens) are vertically cross sectioned and examined as specified in 4.7.2.1, the requirements specified in 3.1, 3.3, and 3.6 shall be met. Non-stressed test specimens shall be evaluated when examination of the stressed cross sections suggest that a failure condition may exist in the completed boards (prior to ~~solder float thermal stress~~ resistance to soldering heat).

3.7.2.2 Horizontal cross sections (when specified) (for metal core printed boards). When specified, metal core printed boards which have clearance between the plated-through holes and the metal core shall require a horizontal cross section prepared to view the metal core hole fill insulation. When inspected in accordance with 4.7.2.2, the presence of wicking, radial cracks, lateral spacing, or voids in the hole-fill insulation material shall not reduce the dielectric spacing between adjacent conductive surfaces to less than 50 percent of the specified spacing. Test coupons or production boards shall have been subjected to ~~solder float thermal stress~~ resistance to soldering heat in accordance with 3.7.6.2 prior to horizontal microsectioning.

3.7.3 Chemical requirements.

3.7.3.1 Ionic contamination ~~(cleanliness)~~. When printed board test specimens are tested in accordance with 4.7.3.1, the levels of ionic contamination shall be in accordance with the requirements of 3.7.3.1.1, ~~3.7.1.2~~ 3.7.3.1.2, or 3.7.3.1.3, as applicable.

3.7.3.1.1 Prior to the application of solder ~~resist~~ mask. Unless otherwise specified, prior to the application of solder ~~resist~~ mask, the level of ionic contamination shall not exceed 0.78 micrograms/square centimeter (5.03 micrograms/square inch).

3.7.3.1.2 Internal layers prior to lamination (when specified, see 3.1 and 6.2.1.a). The levels of ionic contamination for completed internal layers prior to subsequent lamination shall be as specified.

3.7.3.1.3 Completed printed boards (when specified, see 3.1 and 6.2.1.a). The levels of ionic contamination for completed printed boards shall be as specified.

3.7.3.2 Copper plating characteristics.

3.7.3.2.1 Elongation. When copper plating is tested in accordance with 4.7.3.2.1, the elongation shall be 18 percent minimum.

3.7.3.2.2 Tensile strength. When copper plating is tested in accordance with 4.7.3.2.2, the tensile strength shall be 276 Megapascals (40,000 psi) minimum.

3.7.3.2.3 Purity of copper. When copper plating is tested in accordance with 4.7.3.2.3, the purity of the copper shall be 99.50 percent minimum.

3.7.3.4 Permanency of marking ink or paint. Following the test specified in 4.7.3.4, all required markings (see 3.8) shall be legible. Any specified markings which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure.

3.7.4 Physical requirements.

3.7.4.1 Adhesion, marking. After marking is tested in accordance with 4.7.4.1, any specified markings which are missing in whole or in part, faded, shifted (dislodged), or smeared to the extent that it is no longer legible shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

3.7.4.2 Adhesion, plating. When tested as specified in 4.7.4.2, there shall be no part of the conductor pattern or copper plating protective finish (coating or plating) removed from the printed board test specimen except for those related to outgrowth, overhang, or slivers.

3.7.4.3 Adhesion, solder ~~resist~~ mask (when applicable). When tested as specified in 4.7.4.3, the maximum percentage of cured solder ~~resist~~ mask lifted from the surface of the base material, conductors, and lands of the coated printed board test specimen shall not exceed the following limits:

a. Bare copper or base material: 0 percent.

b. Non–melting metals (e.g., gold or nickel plating): 5 percent.

c. Melting metals (e.g., tin–lead plating, solder coating, indium, bismuth, and others): 10 percent.

3.7.4.4 Bow and twist. When printed boards are tested as specified in 4.7.4.4, the maximum limit for bow and twist shall be as specified. When multiple printed board designs are grouped on a panel for assembly purposes, the bow and twist requirements shall be as specified.

3.7.4.5 Component attachment.

3.7.4.5.1 Solderability (see 6.2.1.b). Printed boards that require soldering during assembly processes require solderability testing. Printed boards using only surface mount component do not require hole solderability testing. When required by the procurement documentation, accelerated conditioning for coating durability shall be in accordance with J-STD-003. The default category of coating durability of J-STD-003 is category 2.

3.7.4.5.1.1 Hole solderability. After undergoing the test specified in 4.7.4.5.1, the holes on the printed board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.4.5.1.2 Surface solderability. After undergoing the test specified in 4.7.4.5.1, the lands on the printed board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.4.5.2 Wire bond pull strength (when specified, see 3.1). When inspected as specified in 4.7.4.5.2, plated bonding areas shall be capable of meeting the requirements of table I of method number 2.4.42.3 of IPC-TM-650 without incurring any of the following failures:

a. Wire bond failure (interface between wire and conductive layer).

b. Separation of conductive layers on the bonding area.

c. Bonding area lifted from the base material.

3.7.4.5.2.1 Failure criteria. Any bond pull which results in separation of bonds at the bond interface at an applied stress less than the specified stress for the applicable material and construction shall constitute a failure. Unless otherwise specified, the applied nondestructive pull stress shall be 80 percent of the minimum bond strengths for the applicable material, size and construction given in table I of method number 2.4.42.3 of IPC-TM-650.

3.7.4.6 Rework simulation.

3.7.4.6.1 Plated–through holes. After undergoing the test specified in 4.7.4.6.1, the printed board test specimens shall undergo DPA by microsectioning and evaluation of test specimen in accordance with 4.7.2.1 and the requirements specified in 3.1, 3.3, and 3.6 shall be met.

3.7.4.6.2 Surface mount lands. After undergoing the test specified in 4.7.4.6.2, the surface mount lands of the printed board test specimens shall meet a 3.45 Megapascals (500 PSI) of vertical pull 90 degrees (tension) to the printed board surface.

3.7.4.7 Surface conductor to base material bond or peel strength.

3.7.4.7.1 Bond strength of unsupported component hole lands. After undergoing the test specified in 4.7.4.7.1, the unsupported component hole lands shall withstand 2 kg or 35 kg/cm2, whichever is less.

3.7.4.7.2 Laminated surface foil peel strength (for foil laminated construction only). When tested as specified in 4.7.4.7.2, surface conductors shall yield an average peel strength greater than or equal to the values specified by the applicable base material specification. Unless otherwise specified, the peel strength values shall correspond to "after ~~solder float thermal stress~~ resistance to soldering heat" condition, the foil profile, and the base material thicknesses equal to or less than 0.50 mm (.0197 inch). When applicable, the foil type and starting weight, if addresses by the base material specification, shall apply. This requirement is only applicable to foil laminated printed boards that have surface conductors or surface mount lands. Printed wiring boards with no external circuitry (external terminal land or pads only) do not require peel strength testing.

3.7.4.7.3 Surface mount land pull strength. When tested as specified in 4.7.4.7, surface mount lands shall with stand a minimum of 3.45 MPa (500 psi) vertical pull after completion of the five cycles of soldering and four cycles of desoldering.

3.7.5 Electrical requirements.

3.7.5.1 Continuity. When tested in accordance with 4.7.5.1, unless otherwise specified, there shall be no circuit whose resistance exceeds 10 ohms. For referee purposes, ~~0.5~~ 0.25 ohm maximum per 25.0 mm (.98 inch) of circuit length shall apply. Printed boards with embedded resistive components shall meet the resistance requirements specified.

3.7.5.2 Isolation (circuit shorts). When tested as specified in 4.7.5.2, the resistance between mutually isolated conductors shall be greater than ~~2~~ 100 megohms.

3.7.5.2.1 Circuit or plated–through hole shorts to metal core substrate. When printed board designs with metal cores are tested in accordance with 4.7.5.2.1, the test specimen shall be capable of withstanding 500 volts DC product levels “S” and “T” and 750 volts DC for product level “E” between circuitry/plated–through holes and the metal core substrates. There shall be no flashover or dielectric breakdown. Electrical access to the metal core substrate must be provided when this test is to be run.

3.7.5.3 Dielectric withstanding voltage.

3.7.5.3.1 DC voltage, after MIR. When tested as specified in 4.7.5.3.1, printed boards shall withstand the application of the specified voltage for the specified duration without any dielectric breakdown, flashover, or sparkover between conductors.

3.7.5.3.2 AC voltage (hi-pot). When tested as specified in 4.7.5.3.2, printed boards shall withstand the application of the specified voltages for the specified duration without arcing, breakdown of insulation, or damage. There shall be no leakage current greater than that specified.

3.7.5.4 Insulation resistance (as received). When tested as specified in 4.7.5.4, the printed board test specimen shall have a minimum of 500 megohms of resistance between conductors. Additional insulation resistance requirements are detailed after environmental exposure to moisture (see 3.7.6.1).

3.7.5.5 Impedance testing (when specified). When impedance resistance values are specified, all printed boards shall be electrically tested in accordance with 4.7.5.5 to the values specified.

3.7.6 Environmental requirements.

3.7.6.1 Moisture and insulation resistance. When tested as specified in 4.7.6.1, the printed board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed board test specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in 3.5.1.

3.7.6.2 Resistance to soldering heat.

3.7.6.2.1 Solder float thermal stress (single cycle, for through hole designs). After undergoing the test specified in 4.7.6.2.1, the printed board test specimen shall be inspected in accordance with 4.7.2.1 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.6.2.2 Convection air oven solder reflow test (3 to 6 cycle thermal stress). After undergoing the test specified in 4.7.6.2.2, the printed board test specimen shall be inspected in accordance with 4.7.2.1 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.6.3 Thermal ~~shock~~ cycling.

3.7.6.3.1 Environmental chamber (air-to-air). After undergoing the test specified in 4.7.6.3.1, the printed board test specimens shall meet the following requirements:

a. Visual inspection: When inspected as specified in 4.7.1, there shall be no evidence of plating cracks, blistering, crazing, or delamination ~~in excess of that allowed in 3.5~~.

b. Resistance change: The change in resistance between the first high temperature cycle and the last high temperature cycle shall not be more than 10 percent.

c. DPA by microsectioning: The printed board test specimen shall be vertically cross sectioned and inspected in accordance with 4.7.2.1 and the requirements specified in 3.1, 3.3, and 3.6 shall be met.

3.7.6.3.2 Direct current induced. After undergoing the test specified in 4.7.6.3.2, the printed board test specimens shall meet the following requirements: For capability verification inspection testing, the following conditions shall apply:

a. Number of samples: 6

b. Test temperature: 150 degrees Celsius.

c. Resistance change: 10 percent.

d. Maximum number of cycles: 250 for each 24 hour period.

e. Data collection frequency: 10 cycles

f. Cooling ratio: 0.66

g. Table selection: System.

3.7.6.4 Outgassing. When inspected as specified in 4.7.6.4, unless otherwise specified, the printed board test specimens shall meet the following requirements:

a. Total mass loss (TML) shall not exceed 1.0 percent.

b. Volatile condensable material (VCM) shall not exceed 0.1 percent.

3.7.6.4.1 Outgassing test data. Data listed in NASA Publication 1124 may be used in lieu of actual test data for applicable materials.

3.8 Marking. Conductive legends or marking shall be no closer to the conductive pattern of the printed wiring board than the spacing requirements specified.

3.8.1 Product identification. Product identification marking shall be in accordance with MIL-PRF-31032. The individual printed boards, each set of quality conformance test circuit (QCTC) strips, and individual test coupons shall be marked with the lot date code (as specified below), the traceability serial number, the printed board identification or part number, and unless otherwise specified, the manufacturers CAGE code. Additional marking on the printed wiring boards is allowed provided it does not interfere with the required marking.

3.8.2 Legend. Legends on printed wiring boards shall be as specified.

3.8.3 Legibility. All marking shall be able to withstand solder fluxes, cleaning solutions, and molten solder encountered in the manufacture of printed wiring boards, shall remain legible after all tests, and in no manner affect printed wiring board performance. After any or all tests, product identification or tracebility marking shall comply with the class 3, acceptable conditions detailed in IPC–A–600.

3.8.4 Lot date code. The lot date code is a unique code to identify the period during which the printed wiring boards were manufactured. Unless otherwise specified by the TRB or by the acquiring activity (see 3.1), the first two numbers in the lot date code shall be two digits of the number of the year, and the third, fourth and fifth numbers shall be three digits indicating the Julian date of the final copper plating. When the number of the day is a single or double digit date, it shall be proceeded by zeros or a zero reading from left to right or from top to bottom, the code number shall designate the year and day, in that order. Example of a date code for January 12, 2021 would be "21012".

3.9 Traceability. The TRB shall establish and maintain traceability for all printed boards in the lot. This traceability shall reflect the exact disposition of each printed board. Printed boards that are rejected, and the reason for the rejection shall also be maintained. Each QCTC shall be traceable to the production printed board produced on the same panel. All separated individual test coupons shall have their traceability maintained back to the QCTC from which it was separated. Traceability records shall include printed board and test coupon position on the inspection panel.

3.9.1 Quality–conformance test circuitry, test coupons, and microsection mounts. Each quality–conformance test circuitry (QCTC) shall be identifiable with those corresponding production printed wiring boards produced on the same inspection panel that also produced the QCTC. Unless otherwise specified, each QCTC shall be traceable to its originating position on the panel. All individual test coupons (including those in microsection mounts) separated from its QCTC, or qualification test specimen, shall have its traceability maintained back to the inspection panel, QCTC, or qualification test specimen from which the test coupons originated. When a QCTC or test coupon is representative of more than one printed board design (multiple designs on each panel), it shall be traceable to those printed boards fabricated on that inspection panel. When a microsection mount contains more than one specimen, an orientation mark or other identification marking shall identify layer one of the first specimen. Also, unless otherwise listed on the multiple specimen microsection mount, traceability identifying all specimens contained in a mount shall be maintained.

3.9.2 Printed board materials. Traceability shall be such that for each printed wiring board, all printed board materials specified or used shall be traceable to a material production lot, inspection lot, or other specified grouping.

3.9.3 Serialization. When the contract requires the printed wiring boards to be serialized, each printed wiring board or qualification test specimen shall be marked with a unique serial number assigned consecutively within the inspection lot, allowing traceability of the printed wiring board and its test results.

3.10 Repair. Printed boards shall not be repaired or reveal any evidence of repair.

3.11 Workmanship. Printed boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability, or appearance. There shall be no contamination, oil, corrosive substance, salt, grease, finger print, mold generating source, foreign materials, dirt, corrosion, corrosion product, soot, mold release agent, flux residues or defects which could affect the function, performance and reliability of printed wiring boards.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

a. Qualification inspection (see 4.2).

b. Conformance inspection (see 4.3 and tables I and II).

c. Capability verification inspection (see 4.6).

4.1.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-PRF-31032, and as specified herein.

4.1.2 Standard test and inspection conditions. Unless otherwise specified by the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

4.1.3 Implementation of this specification sheet. All printed boards offered and shipped in compliance with this specification sheet shall meet the performance requirements specified for the applicable product level. The manufacturer shall verify that printed boards meet the design and performance requirements of the applicable product level. The manufacturer is responsible for developing a verification program which will meet this requirement. Additional quality management steps for product levels T and E are outlined in appendix A.

4.2 Qualification inspection. Unless otherwise specified by the TRB approved qualification test plan, qualification inspection shall be in accordance with MIL-PRF-31032 and as specified herein.

4.2.1 Qualification test vehicles. The qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with the TRB approved qualification test plan and the applicable qualification test vehicle specification(s).

4.2.2 Sample. The number of qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with TRB approved qualification test plan.

4.2.3 Test routine. The qualification test vehicle(s) shall be subjected to the inspections and tests specified in tables I and II in addition to thermal ~~shock~~ cycling in accordance with 3.7.6.3 and 4.7.6.3.

4.2.4 Qualification by similarity. Not applicable to this specification sheet. Only parameters actually verified during qualification shall be considered qualified.

4.2.5 Substitutability of product levels. A manufacturer may supply printed boards to those product levels lower than to which they are qualified. Printed boards verified to a higher product level are substitutable, with the acquiring agency approval, for a lower specified product level.

4.3 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-31032 and shall consist of lot conformance inspection (see 4.4) and periodic conformance inspection (see 4.5).

4.3.1 Inspection of product for delivery. Unless otherwise specified, product level S shall be the default product level.

4.3.1.1 Product level S. Inspection of product for delivery shall consist of lot conformance inspection.

4.3.1.2 Product level T. Inspection of product for delivery shall consist of lot conformance inspection and periodic conformance inspections. These inspections shall be performed on production lot basis.

4.3.1.3 Product level E. Inspection of product for delivery shall consist of lot conformance inspection and periodic conformance inspections and shall be performed on production lot basis. Test optimization (the reduction or elimination or verifications) which may be granted for product levels S and T, is not allowed for this level of product.

4.4 Lot conformance inspection. Lot conformance inspection shall be in accordance with 2HMIL-PRF-31032 and table I herein. Panels and printed boards to be delivered in accordance with this specification sheet shall have been subjected to and passed all applicable inspections and tests of table I prior to delivery of product. Lot conformance inspection testing by subgroup or within a subgroup may be performed in any sequence.

4.4.1 Subgroup 1 inspections (panel acceptance). The panel acceptance test shall be in accordance with 2HMIL-PRF-31032, and as specified in table I, subgroup 1.

4.4.1.1 Sampling, type 3 designs. For product level S, a minimum of two test coupons (one A and one B test coupon) per completed panel shall be tested for type 3 designs. The two test coupons shall be taken from opposite corners of the panel. After the test, one of the test coupons shall be vertically cross sectioned in the panel's length (X direction) and the other shall be vertically cross sectioned along the panel's width (Y direction). Product levels T and E shall have additional center of panel test coupons for when more than one printed board is on the production panel (see appendix A).

4.4.1.2 Sampling, type 4 designs. In addition to the sampling required in 4.4.1.1, type 4 printed boards shall have one additional ~~thermal stressed~~ resistance to soldering heat coupon vertically cross sectioned for each copper plating process used. See 6.6 for additional guidance.

4.4.1.3 Percent defective allowable (PDA) limits. The PDA limits for panel acceptance shall be 32 percent.

4.4.1.4 Failure mode observations. If the ~~microsection evaluation~~ results of DPA by microsectioning of test specimens indicate a potential failure mode in the non–stressed printed board test specimens (i.e., propagation of subsurface imperfections, lifted lands within post–~~thermal stress~~ resistance to soldering heat acceptance criteria, or other indicators), additional DPA by microsectioning examination of non–stressed test specimens shall be performed.

4.4.2 Subgroup 2 inspections (100 percent inspections). The subgroup 2 inspections shall be in accordance with 2HMIL-PRF-31032, and as specified in table I, subgroup 2. Electrical continuity testing of all connections is recommended on internal layers both prior to lay up and at the completed bare board level. Electrical isolation should be established by hi-pot testing, minimum 1500 volts.

4.4.2.1 PDA limits. The PDA limits for subgroup 2 inspections shall be 50 percent. ~~Any lot of a single part number with more than 5 percent rejects or 1 reject, whichever is greater, shall not be furnished on the contract or purchase order.~~

TABLE I. Lot conformance inspection.

Inspection	Requirement paragraph	Method paragraph	Specimen to test 1/				Sample plan 2/
			PWB	THM	SMT	MIX	
Subgroup 1 (panel acceptance)							
Solder float thermal stress	3.7.6.2.1	4.7.6.2.1		A & B	A & B	A & B	See 4.4.1.1 and 4.4.1.2
As received	3.7.2	4.7.2		A	A	A	
Subgroup 2 (100 percent)							
Continuity	3.7.5.1	4.7.5.1	X				100 percent
Isolation (circuit shorts)	3.7.5.2	4.7.5.2	X				100 percent
Subgroup 3a (Sample)							
Acceptability 3/ 4/	3.7.1	4.7.1	X				Plan BH
Subgroup 3b (Sample)							
Chemical:							
Ionic contamination 5/	3.7.3.1.1	4.7.3.1	X				Plan BN or TN 6/
Subgroup 3c (Sample)							
Physical:							
Adhesion, marking	3.7.4.1	4.7.4.1	X	7/	7/	7/	Plan BH or TJ 6/
Adhesion, plating 8/	3.7.4.2	4.7.4.2	X	C	C	C	Plan BH or TJ 6/
Adhesion, solder ~~resist~~ mask	3.7.4.3	4.7.4.3	X	G	G 9/	G 9/	Plan BH or TJ 6/
Bow and twist	3.7.4.4	4.7.4.4	X				Plan BH
Solderability							
Hole	3.7.4.5.1.1	4.7.4.5.1		S or A		A or S	Plan TJ
Surface	3.7.4.5.1.2	4.7.4.5.1			C or M	C or M	Plan TJ

1/ Test coupons are in accordance with IPC-2221. PWB is a production board; THM is a through–hole mount test coupon; SMT is a surface mount PWB test coupon; MIX is for printed board designs containing both through–hole and surface mount components test coupon.
2/ See 2HMIL-PRF-31032 for C = 0 sampling plans.
3/ Design (3.3), conductor spacing (3.5.2.5), conductor width (3.5.2.6), conductor imperfections (3.5.2.3) and workmanship (3.9) shall be inspected on both the internal layers containing conductors prior to lamination and the completed printed board.
4/ Surface imperfections (3.5.1.2) and subsurface imperfections (3.5.1.3) shall be inspected prior to solder ~~resist~~ mask application.
5/ Inspection shall be performed prior to solder ~~resist~~ mask application. Additional inspections on completed printed boards may be specified.
6/ Test coupon, production panel, or production printed board, manufacturer option.
7/ See 4.7.4.1 for test specimen description and quantity.
8/ All surface platings or coatings shall be inspected.
9/ Test coupon T shall be used when production printed boards have tented via holes.
10/ When using the “S” test coupon, the number of samples to be tested shall be based on a statistical sample of the inspection panels in the lot using plan TJ. When using the “A” test coupon, the number of samples to be tested shall be based on the same statistical sample as the “S” test coupon, but a multiple of 4 shall be applied to the resulting sample size. “A” test coupons shall be selected in groups of 4, taken from the same inspection panel.

4.4.3 Subgroup 3 inspections (sample). Panels and printed boards to be delivered in accordance with this specification sheet shall have been subjected to and passed all the inspections of table I, subgroups 3a, 3b, and 3c.

4.4.3.1 Sampling. A sample of printed boards (or test coupons that represent the printed boards) shall be randomly selected from each inspection lot.

4.4.3.2 PDA limits. When 100 percent of a production lot is inspected, either in lieu of sampling or due to rejection of a sample inspection lot, the PDA limits for this 100 percent inspection shall be 50 percent.

4.5 Periodic conformance inspection. Periodic conformance inspection shall be in accordance with TRB approved periodic conformance inspection plan or table II herein.

TABLE II. Periodic conformance inspection baseline test coverage.

Inspection 1/	Requirement paragraph	Method paragraph	Sample size	Frequency
Elongation Tensile strength Purity	3.7.3.2.1 3.7.3.2.2 3.7.3.2.3	4.7.3.2.1 4.7.3.2.2 4.7.3.2.3	1/ 1/ 3/	Monthly Monthly Monthly
Rework simulation Bond strength of unsupported component hole Bond strength of surface mount lands Laminated surface foil peel strength	3.7.4.6 3.7.4.7.1 3.7.4.7.2 3.7.4.7.3	4.7.4.6 4.7.4.7.1 4.7.4.7.2	3/ 3/ 3/ 2/	Monthly Monthly Monthly Monthly
Moisture and insulation resistance Dielectric withstanding voltage 2/	3.7.6.1 3.7.5.3	4.7.6.1 4.7.5.3	3/ 3/	Monthly Monthly

1/ A minimum of ten test specimens (five lengthwise and five crosswise) shall be inspected.
2/ A minimum of eight test specimens (four each from two lots) shall be inspected.
3/ A minimum of two test specimens shall be inspected.

4.6 Capability verification inspection (see 6.8). Capability verification inspection shall be in accordance with the TRB approved capability verification inspection plan or table III herein. The frequency of this verification shall be at the time of qualification and as a minimum every 2 years thereafter. Each base material type qualified shall be verified.

TABLE III. Capability verification inspection baseline test coverage.

Inspection 1/	Requirement Paragraph	Method Paragraph	Frequency
Thermal cycling	3.7.6.3	4.7.6.3	

1/ A minimum of two test specimens per inspection shall be tested.

4.7 Methods of inspection.

4.7.1 Visual and dimensional inspection. The visual and dimensional features of the printed wiring board test specimen shall be inspected using either test method number 2.2.1 or 2.2.2 of IPC-TM-650, as applicable. Unless otherwise specified, the magnifications in table IV shall be used for the conductor width or land diameter/width of features under inspection. Referee inspection needed to confirm a suspected defect of the specimen features shall be accomplished at a magnification of up to 30X, as applicable to confirm the suspected defect. Characteristics not observable through solder ~~resist~~ mask shall be evaluated prior to its application. Verification of printed board dimensional parameters using automated inspection technology (AOI and AXI) shall be acceptable.

TABLE IV. Inspection magnification.

Conductor width or land diameter/width	Magnification 1/		IPC-OI-645 grade
	Standard inspection	Referee inspection	
Greater than 1.0 mm	1.75 x	4x	IV & V
0.5 to 1.0 mm	4x	10x	V & VI
0.25 to 0.5 mm	10x	20x	VI & VII
Less than 0.25 mm	20x	40x	VII & VIII

1/ Referee conditions are used to verify printed boards rejected at the standard inspection magnification power. For printed board designs with mixed conductor and land diameters and widths, the greater magnification power may be used for the inspection of the entire printed board.

4.7.1.1 Annular ring, external (see 3.5.2.1). The measurement of the annular ring on external layers is from the inside surface (within the hole) of the plated hole or unsupported hole to the outer edge of the annular ring on the surface of the printed wiring board.

4.7.1.2 Overall printed board thickness (see 3.5.3). Unless otherwise specified, the overall printed board thickness measurement shall be inspected by any micrometer or by vertical cross section in accordance with 4.7.2.

4.7.1.2.1 With edge-board contacts. Printed boards with edge-board contacts shall have the overall thickness measured across the board on the final finish plated surfaces of opposite contacts.

4.7.1.2.2 Without edge-board contacts. Printed boards without edge-board contacts shall have the overall thickness measured across the board from plated copper surface to plated copper surface not including the final finish plating.

4.7.1.3 Solder ~~resist~~ mask thickness (see 3.5.4.5). Solder ~~resist~~ mask thickness shall be inspected by any micrometer or by microsection in accordance with 4.7.2.

4.7.1.4 Registration, nondestructive, via radiography (X-ray). Registration may be assessed by radiographic techniques **using** test method number 2.6.10 of IPC-TM-650.

4.7.1.5 Wire bond pad surface roughness. The printed board specimen shall be inspected for surface roughness in accordance with test method number 2.4.15 of IPC-TM-650. Only the pristine area shall be evaluated.

4.7.1.6 Alternate plating and coating measurement techniques. When a plating or coating is less than 0.00125 mm (.00005 inch) in thickness, the verification of thickness shall be performed in accordance with one of the following test methods:

a. ASTM B567, measurement of thickness by the Beta Backscatter Method.

b. ASTM B568, measurement of thickness by X-ray spectrometry.

These methods can also be used to verify plating and coating thicknesses greater than 0.001 mm (.00004 inch).

4.7.1.7 Materials inspection. Prior to any fabrication, materials inspection shall consist of certification supported by verification data, which verifies that the materials specified (see 3.1) used in fabricating the printed boards enable the printed boards to meet the requirements of this specification sheet.

4.7.1.8 Workmanship. The printed board specimen shall be inspected in accordance with test method number 2.1.8 of IPC-TM-650, except that the magnification shall be 1.75x (3 diopters), minimum.

4.7.2 Destructive physical analysis (DPA) by microsectioning and evaluation of printed board test specimens. Automatic microsectioning techniques may be used in lieu IPC-TM-650 methods specified in 4.7.2.1 or 4.7.2.2.

4.7.2.1 Vertical cross sections.

4.7.2.1.1 Mount preparation. Test specimen mount preparation shall be accomplished by using methods in accordance with either numbers 2.1.1 or 2.1.1.2 of IPC-TM-650. The following details shall apply:

a. Number of holes per specimen. A minimum at least three plated–through holes cross sectioned vertically shall be made for each test specimen required. Each side of the three plated–through holes shall be viewed independently.

b. Accuracy. All three plated–through holes of each test specimen shall be sectioned, ground, and polished to within ±10 percent of the center of the drilled diameter of the hole.

c. Pre–microetch evaluations. The plated–through holes shall be evaluated for plating separations prior to microetching.

d. When more than two test specimens are contained in a mount (gang mounting), the following shall apply:

(1) The test specimens shall not contact any other specimen. The recommended distance between test specimens in a mount is 0.025 to 0.157 mm (.010 to .062 inch).

(2) An orientation mark or other identification marking shall identify layer one of the first test specimen. Also, unless otherwise listed on the mount, traceability identifying all specimens contained in a mount shall be available.

4.7.2.1.2 Mount examination and inspection. The examination and inspection of the plated–through hole structure of the test specimens in the mount to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, etc., shall be accomplished in accordance with test method number 2.2.5 of IPC-TM-650. The following details shall apply:

a. Magnifications. The test specimens shall be inspected at magnifications specified in test method number 2.2.5 of IPC-TM-650. Referee inspections shall be accomplished at a magnification of 400X ±5 percent.

b. Evaluations. The plated–through holes shall be evaluated for foil and plating cracks and plating separations prior to and after microetching the surface of the test specimens in the mount. Pre and post microecthing evaluations for the criteria of 3.1, 3.3, and 3.6 shall be accomplished at magnifications specified above.

c. Measurements. Measurements shall be averaged from at least three determinations for each side of each plated–through hole of each test specimen. The copper plating thickness of the plated–through hole wall shall be determined from the average of three measurements, approximately equally spaced, taken on each side of the plated–through hole. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in 3.6.5.1.1.

d. Plating and coatings that are less than 0.00125 mm (.00005 inch) in thickness shall not be measured using metallographic techniques. See 4.7.1.6 for alternate measurement techniques.

4.7.2.2 Horizontal cross section preparation and inspection. Horizontal cross section preparation shall be accomplished by using methods in accordance with either test method number 2.1.1 or 2.1.1.2 of IPC-TM-650. The following details shall apply:

a. Number of holes per test specimen. A minimum at least one plated–through hole for each layer using hole fill insulation material of the associated printed board shall be prepared.

b. Accuracy. All three plated–through holes shall be sectioned, ground, and polished to within ± 25 percent.

c. Magnifications. The test specimens shall be inspected at magnifications of 80 to 120X ±5 percent. Referee inspections shall be accomplished at a magnification of 200X ±5 percent.

d. Evaluations. The requirements of 3.6 shall be met.

4.7.2.3 Registration, destructive, via vertical cross section of plated through holes. Measurement of annular rings is from the inside of the drilled hole to the edge of the internal land. Buried vias are considered to be an external layer and are assessed in-process before multilayer lamination. Internal registration and annular ring measurements may be determined during DPA by microsection evaluation.

4.7.2.4 Plated hole inspection details (see 3.6). When plated holes are inspected in accordance with 4.7.1, the following details shall apply:

a. Annular ring (internal) (see 3.6.4.1). The measurement of the annular ring on internal layers is from the inside drilled surface (within the hole) of the plated hole or unsupported hole to the outer edge of land. This measurement shall apply to all internal lands for all three holes.

b. Dielectric layer thickness (see 3.6.1.1). The dielectric layer thickness shall be inspected between all conductor layers present in the test specimen.

c. Conductor thickness (see 3.6.3). The external and internal metal foil thickness shall be inspected on all conductor layers present in the test specimen.

d. Copper plating and surface finish thickness (see 3.6.5 and 3.6.2.4). Isolated thick or thin sections shall not be used for averaging. However, isolated areas of reduced copper thickness shall be measured for compliance with the requirements of 3.6.5.1.1.

e. Copper plating voids (see 3.6.5.1.1). Any plated hole in the microsection failing the plating void criteria of 3.6.5.1.1 subparagraphs a, b, or c, shall be cause for the entire inspection panel of printed wiring boards associated with the microsection to be rejected. The following details apply if a single plating void is found:

(1) Type 2: If the plating void does not exceed the conditions of 3.6.5.1.1, the entire lot (100-percent panel inspection) shall have test specimens from each inspection panel microsectioned and inspected for voids. If a plating void is present in any microsection mount representing an inspection panel, a referee microsection shall be performed using an A or B test coupon from the opposite corner of that inspection panel. If the referee has no plating voids, that panel is acceptable, however, if a plating void is present in that microsection, that inspection panel of printed wiring boards shall be rejected.

(2) Type 3: If the plating void does not exceed the conditions of 3.6.5.1.1, a referee microsection shall be performed using an A or B test coupon from the opposite corner of the inspection panel. If the referee has no plating voids, the panel is acceptable, however, if a plating void is present in that microsection, that inspection panel of printed wiring boards shall be rejected.

f. Heatsink planes (see A.3.6.4.1 and figure A–7). The lateral dielectric spacing between the heatsink planes and adjacent conducting surfaces, nonfunctional lands, or plated-through holes shall be measured at the closest point between these surfaces.

4.7.3 Chemical test methods.

4.7.3.1 Ionic contamination. The printed board specimen shall be inspected for ionic contamination in accordance with test method number 2.3.25 of IPC-TM-650.

4.7.3.2 Copper plating tests. Samples shall be taken at minimum and maximum current plating densities.

4.7.3.2.1 Elongation of copper. The test for elongation of plated copper shall be performed in accordance with ASTM E345 or test method number 2.4.18.1 of IPC-TM-650. The travel speed of testing shall be 50.0 mm ±1.0 mm (1.97 ±.03 inch) per minute.

4.7.3.2.2 Tensile strength of copper. The test for tensile strength of plated copper shall be performed in accordance with ASTM E345 or test method number 2.4.18.1 of IPC-TM-650. The travel speed of testing shall be 50.0 mm ±1.0 mm (1.97 ±.03 inch) per minute. The mean average cross-sectional area shall be determined using the following:

a. Measure the thickness of the test specimens by use of an optimeter, an electrical type measuring device, or vernier micrometer, provided that the thickness is measured to at least the nearest 2 percent.

b. Measure the test specimen width dimension to the nearest 0.025 mm (.001 in.)

c. The mean average test specimen cross-sectional area shall equal the average thickness multiplied by the average width.

4.7.3.2.3 Purity of copper. The test for purity of plated copper shall be performed in accordance with ASTM E53 or test method number 2.3.15 of IPC-TM-650.

4.7.3.4 Permanency of marking ink or paint (see 3.7.3.4). Printed boards shall be tested in accordance with test method number 2.3.4 of IPC-TM-650. The following details apply:

a. The marked portion of the printed board test specimen shall be brushed. Brush strokes of each solvent solution shall be evenly divided between required markings.

b. After the test, the printed board test specimen shall be visually inspected in accordance with 4.7.1 for legibility of marking and the requirements of 3.7.3.4.

c. Mechanical damage: There shall be no damage to the printed board test specimen at the conclusion of the test sequence.

4.7.4 Physical test methods.

4.7.4.1 Adhesion, marking. Printed board test specimens which represent all types of marking used on the lot (except etched marking) shall be subjected to the solderability test in 4.7.4.6. The side of the test specimen that is marked shall be placed against the solder. After the test, the test specimen shall be examined in accordance with 4.7.1 and the requirements of 3.7.4.1 shall be met.

4.7.4.2 Adhesion, plating. The test for plating adhesion shall be performed in accordance with test method number 2.4.1 of IPC-TM-650. If overhanging metal break off and adheres to the tape, it is evidence of outgrowth, overhang or slivers, but not of plating adhesion failure.

4.7.4.3 Adhesion, solder ~~resist~~ mask. The test for solder ~~resist~~ mask adhesion shall be performed in accordance with test method number 2.4.28.1 of IPC-TM-650.

4.7.4.4 Bow and twist. The tests for bow and twist shall be performed in accordance with test method number 2.4.22 of IPC-TM-650.

4.7.4.5 Component attachment.

4.7.4.5.1 Solderability. The tests for hole or surface solderability shall be performed in accordance with J-STD-003. The default category of coating durability of J-STD-003 is category 2. When required by the procurement documentation, accelerated conditioning for coating durability shall be in accordance with J-STD-003.

4.7.4.5.2 Wire bond pull strength. The wirebond pull strength test shall be performed in accordance with test method number 2.4.42.3 of IPC-TM-650.

4.7.4.6 Rework simulation (see 3.7.4.6).

4.7.4.6.1 Plated–through holes. The rework simulation test shall be performed in accordance with test method number 2.4.36 of IPC-TM-650. The following details shall apply:

a. Unless otherwise specified, method A shall be used initially.

b. For designs with an overall printed board thickness greater than 3.0 mm (.118 inches), one row of plated holes shall be used to assure that the method to be used during the soldering and desoldering operation will produce satisfactory solder connections (the wire is wetted through the entire plated hole within the soldering time limits specified in the test method) for the printed wiring board test specimen design being tested.

c. In case of an unsatisfactory solder connection (an insufficient solder connection is produced or the soldering time exceeds the limits specified in the test method), another plated hole on the row shall be soldered using the soldering temperature of the next higher method (e.g., method B if method A is insufficient, or method C if method B does not suffice) until a satisfactory solder connection is made. If the temperatures of method C still yields unsatisfactory solder connections, consult the qualifying activity for additional guidance before proceeding further with the testing.

d. Once a method that produces satisfactory solder connections has been determined, the soldering and desoldering operation shall proceed using a different row of plated holes which will be evaluated to the acceptance criteria of 3.7.4.6. The final test method selected shall be noted in the test report.

4.7.4.6.2 Surface mount lands. The rework simulation test shall be performed in accordance with method A of test method number 2.4.21 of IPC-TM-650, method C. The following details and exceptions apply:

a. Test specimen design: The test specimen design shall be as specified in table I ("N" in accordance with IPC-2221). At least three lands that are not on the same strip of conductor shall be used.

b. The diameter of the wire shall not exceed the width of the pad and the calculation step use of the area of the rectangular pad.

c. Preparation: Wire shall be soldered to the land.

d. Soldering cycles: The specimens shall be subjected to the five cycles of soldering and four cycles of desoldering, before the pull test.

4.7.4.7 Surface conductor to base material bond strength.

4.7.4.7.1 Bond strength of unsupported component hole land. The unsupported component hole lands shall be tested in accordance with method A of test method number 2.4.21 of IPC-TM-650. Calculations of land area of the unsupported hole do not include the area occupied by the hole.

4.7.4.7.2 Metal foil peel strength (multilayer using foil lamination). The metal foil of printed board test specimens shall be tested in accordance with test condition A of test method number 2.4.8 of IPC-TM-650. The following details and exceptions apply:

a. Test specimens. The specimen shall consist of conductors that provide a minimum test length of 51 mm (2 inches and a conductor width of 3.3 mm (.125 inch). The peel strength test specimen design shall be in accordance with the patterns depicted on test coupon N of IPC-2221 or number 5.8.3 of IPC-TM-650 that provide compliant dimensions.

b. Test specimen preparation. All finishes (plated tin–lead, solder coating, or other plated metallic resist) shall be either prevented from being deposited during manufacturing or chemically removed prior to test. The test specimen shall not be coated with any organic coating for testing purposes.

c. Sample size. At least one test coupon per foil laminated side shall be placed on the panel where space is available. Eight peel strength test specimens shall be selected from two different production lots; four from each lot or 100 percent if the number of coupons available is less than four for a production lot. If only one foil laminated lot is submitted and passes LCI in a calendar month, then peel strength test specimens from that lot shall be submitted for PCI verification.

4.7.5 Electrical test methods.

4.7.5.1 Continuity (see 3.7.5.1). Printed boards shall be tested for continuity in accordance with IPC-9252. Unless otherwise specified, printed boards shall be net list tested at a voltage potential of 250 volts dc, minimum. ~~A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed those specified in the applicable design standard for the smallest conductor in the circuit.~~

4.7.5.2 Isolation (circuit shorts). The test for isolation shall address the parameters required by the level C requirements of IPC-9252. A test voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The test voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. If the maximum rated voltage of the printed board is not specified, the test voltage shall be 250 volts dc, minimum.

4.7.5.2.1 Circuit or plated–through hole shorts to metal substrate. The printed wiring board test specimen shall be tested in accordance with test method number 2.5.7 of IPC-TM-650. The following details and exceptions apply:

a. Test specimen: The test specimen shall be the production printed board.

b. The voltage: The polarizing voltage shall be 750 +15/-0 volts DC for product level E and 500 +15/-0 volts DC for all other product levels.

c. Points of application: The polarizing voltage shall be applied between conductor patterns of each layer and the electrically isolated heatsink in a manner that each net is tested.

d. Unless otherwise specified, a current leakage greater than 1 microampere shall constitute a failure.

4.7.5.3 Dielectric withstanding voltage.

4.7.5.3.1 DC voltage, after MIR (atmospheric pressure). The printed wiring board test specimen shall be tested in accordance with test condition B of test method number 2.5.7 of IPC-TM-650. The following details and exceptions apply:

a. Test specimen: The test specimen shall be as identified in table II and shall been subjected to the moisture and insulation resistance test.

b. Test specimen preparation: This portion of the test method shall be skipped. DWV testing shall be performed once the test specimen has stabilized to laboratory ambient temperatures, however the testing shall begin no later than 2 hours after removal of specimen from the moisture chamber.

c. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

d. Examination after test: During the tests, the leakage current shall be monitored and the test specimens examined for evidence of arcing and breakdown. At the conclusion of the test, test specimens shall be examined for evidence of damage.

4.7.5.3.2 AC voltage (hi-pot). When specified, the printed wiring board test specimen shall be tested in accordance with test method number 2.5.7 of IPC-TM-650. The following details and exceptions apply:

a. Test specimen: The test specimen shall be the production printed board.

b. Specimen preparation: Unless otherwise specified, the production printed boards shall not be prepared in accordance with the test method.

c. Magnitude of test voltage: The maximum voltage, rate of voltage rise per second, and when applicable, leakage current shall be as specified.

d. Nature of potential: Alternating current.

e. Duration of application of specified test voltage: Unless otherwise specified, a minimum duration of 5 seconds for quality conformance inspection, 1 minute for qualification inspection.

f. Points of application: Unless otherwise specified, the specified voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

4.7.5.4 Insulation resistance (As received). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.3 of IPC-TM-650.

4.7.5.5 Impedance testing. Unless otherwise specified, impedance testing shall be performed in accordance with IPC-9252.

4.7.6 Environmental test methods.

4.7.6.1 Moisture and insulation resistance. The test for moisture and insulation resistance shall be performed in accordance with of test method number 2.6.3 of IPC-TM-650. The following details and exceptions apply:

a. Specimen preparation: Method A

b. Test condition: Class 3.

c. The initial and final insulation resistance shall be greater than or equal to 500M ohm when measured at 500 volts (+10, -0 percent) DC.

4.7.6.2 Resistance to soldering heat (see 3.7.6.2).

4.7.6.2.1 Solder float thermal stress (single cycle, for through hole designs). The test for ~~thermal stress~~ resistance to soldering heat shall be performed in accordance with test method number 2.6.8 of IPC-TM-650. The following details and exceptions apply:

a. Test surfaces: The specimen shall be tested equally per surface (half of tests on layer one side and the other half on the bottom side of the specimen, alternating sides per test cycle).

b. Time between tests: Unless otherwise specified (see 3.1), the time between tests shall be 30 to 60 minutes.

c. Storage between test cycles: The specimen shall be placed in a dessicator on a ceramic plate between test cycles.

d. Test conditions: For level S, test condition A shall be used. For levels T and E, test condition B shall be used.

4.7.6.2.2 Convection oven reflow (3 to 6 cycle thermal stress) (see 6.6.4). The test for ~~thermal stress~~ resistance to soldering heat shall be performed in accordance with test method number 210 of 3HMIL-STD-202. The following details and exceptions apply:

a. Reflow chamber. The reflow chamber shall be a convection air oven suitable for reflow soldering. The reflow chamber shall have adequate environmental controls to maintain the temperature on the surface of the test specimen within the tolerance range and limits in the designated reflow profiles.

b. Test surfaces: The test specimen shall be tested equally for each surface (half of test cycles on layer one side and the other half on the bottom side of the test specimen, alternating sides for each thermal cycle).

b. Time between tests: Unless otherwise specified (see 3.1), the time between tests shall be 10 to 15 minutes.

c. Storage between test cycles: The test specimen shall be placed in a dessicator on a ceramic plate between thermal cycles.

d. Test conditions: For level S, test condition I shall be used. For levels T and E, test condition J shall be used.

e. The test specimen shall be placed into the reflow chamber and the temperature of the component ramped at a rate of 1°C/s to 2°C/s as measured by the thermocouple. The assembly shall be above 183°C for 120 seconds and held at the final temperature and time designated by the test condition. The test specimen shall then be allowed to cool to temperature at a rate of 2°C/s to 3°C/s. This constitutes one heat cycle.

f. The specific combination of temperature, preheat, and duration of the oven shall comply with profile condition I for condition I and profile condition J in accordance with figure X.

g. Number of heat cycles: The test specimen shall be exposed to three heat cycles.

h Special preparation of specimens. The test specimens shall not be fluxed nor have solder paste applied. A low mass thermocouple shall be attached tightly to the test specimen at an appropriate position away from the edges.

4.7.6.3 Thermal ~~shock~~ cycling.

4.7.6.3.1 Environmental chamber (air-to-air). The test for thermal ~~shock~~ cycling shall be performed in accordance with test method number 2.6.7.2 of IPC-TM-650 except that the temperature extremes shall be –65 degrees Celsius and +125 degree Celsius.

4.7.6.3.2 DC current induced. The test for DC current induced thermal cycling shall be performed in accordance with test method number 2.6.26 of IPC-TM-650.

4.7.6.4 Outgassing. The test for outgassing mass loss shall be tested in accordance with test method number 2.6.4 of IPC-TM-650 or ASTM E595. Test specimens shall be approximately 1 cubic cm in volume. The test specimens shall be placed in a vacuum chamber capable of achieving 7 x 10E–3 Pa for 24 hours.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-PRF-31032 are applicable to this specification sheet.

6.1.1 Intended use. This specification sheet was developed for the use of verifying the performance of space and launch vehicle level rigid printed boards. Printed boards intended for other uses can be verified to the performance requirements contained in this document, however, the acquiring activity should determine the performance parameters needed and evaluate those of other MIL-PRF-31032 specifications sheets the intended service use.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, revision letter, and date of this specification.

b. The specific issues of individual documents referenced (see section 2).

c. Title, number, and date of applicable printed board procurement documentation or drawing. Identification of the originating design activity and, if applicable, the Government approved deviation list for the printed board procurement documentation or drawing.

d. The complete product procurement documentation part or identifying number (see 3.1).

e. The printed wiring board type classification (type 3 or 4, see 1.2.1 and 3.1).

f. Title, number, revision letter (with amendment number when applicable), and date of the applicable design standard with performance classification.

g. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the product inspection lot to be supplied with each shipment by the QML manufacturer, if applicable.

h. Requirements for certificate of compliance, if applicable.

i. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

j. Levels of packaging required.

k. If special or additional identification marking is required (see 3.8).

6.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the printed board procurement documentation.

a. If any special or additional cleanliness is required (see 3.7.3.1.2).

b. The durability of coating rating (accelerated aging for solderability testing) if other than category 2 (see J-STD-003).

c. Requirements for failure analysis, corrective action and reporting of results.

d. Disposition of lot conformance inspection sample units.

e. Any other special requirements.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 31032) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification sheet. Information pertaining to qualification of products may be obtained from Defense Supply Center, Columbus, ATTN: DSCC–VQE, P.O. Box 3990, Columbus, OH 43218–3990 or e–mail 5998_Qualifications@dscc.dla.mil.

6.4 Blind or buried vias. This specification sheet includes provisions for verifying the performance of types 4, 5, and 6 rigid printed wiring boards.

6.5 Tin finishes. Pure tin platings or coating are prohibited (see 3.4.1) since it may result in tin whisker growth. Tin whisker growth could adversely affect the operation of electronic equipment systems. For additional information on this matter, refer to ASTM B545 (Standard Specification for Electrodeposited Coating of Tin). The use of alloys with tin content greater than 97 percent may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture, and can develop under typical operating conditions on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers.

6.6 Verification discussion.

6.6.1 Organic contamination. The printed board shall be tested in accordance with test method numbers 2.3.38 or 2.3.39 of IPC-TM-650. Test method number 2.3.38 of IPC-TM-650 is a qualitative method in which very pure acetonitrile is dripped across the test coupon or production board and collected on a microscope slide. It is dried and compared with a slide having dried, uncontaminated acetonitrile on it for visual evidence of organic residue. If evidence of organic contamination is detected by this test, then test method number 2.3.39 of IPC-TM-650 shall be used to determine the nature of the contaminant by the use of infrared spectrophotometric analysis using the Multiple Internal Reflectance (MIR) method.

6.6.2 Outgassing. Materials and finishes shall exhibit total mass loss (TKL) of not more than 1.0 percent and shall have a collected volatile condensable material (CVCM) of not more than 0.1 percent. However, if the TML is greater than 1.0 percent, but it can be shown that contributions to the TML in excess of 1.0 percent are due only to absorbed water vapor, the materials shall be acceptable.

6.6.3 Conductive interfaces. The term conductive interfaces shall be used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of copper or metal foil. The interface between platings and coating (electroless copper, direct metallization copper, and non–electroless electroless copper substitutes, etc., and electrolytic copper, whether panel or pattern plated) shall also be considered a conductive interface.

6.6.4 Resistance to solder heat, convection air oven. The test methodology contained herein for 4.7.6.2.2 is based on the work of the IPC's "next generation thermal stress" D-32 Task Group. Since the task group has not completed it's work developing a new and unpublished test method, the method of 4.7.6.2.2 is an interpretation using 3HMIL-STD-202 available method. If a suitable new method is generated by the IPC D-32 Task group, then it will be referenced by this document. The design of the reflow chamber should be flexible enough to facilitate the creation of proper reflow profiles for all test specimen designs encountered and the incorporation within the parameters of reflow profiles given. Some parameters to consider when evaluating ovens are as follows:

a. Conveyor speed (if applicable).

b. Cooling down rate.

c. Environmental control capability (heating and cooling).

d. Heating ramp rate.

e. Oven programming capability.

f. Oven profile memory.

g. Preheating capabilities.

h. Thermal mass compensation capability (energy vs. time).

i. Time above liquidus (TAL).

6.7 Supporting documents. The following document is not directly referenced herein, but should be used as a guideline.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-HDBK-1547 – Electronic Parts, Materials, and Processes For Space And Launch Vehicles.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

6.8 Product level requirement summary. Table IV contains a summary of differences between the different product levels. This summary was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies. Bidders, contractors, and users are cautioned to evaluate the requirements of this document based on the entire content irrespective of the table. The acquiring activity must realize that the summaries of the requirements of a particular application must be taken into consideration and compared with the advantages and drawbacks of each of the several product levels, before a final choice is made.

TABLE IV. Product level requirement summary.

Requirement or verification	Paragraph	Product level			
		S	T	E	C
Design	3.3	Required	Required	Required	As specified
Materials	3.4	Required	Required	Required	As specified
Visual & Dimensional	3.5	Required	Required	Required	As specified
Plated–through hole structural integrity	3.6	Required	Required	Required	As specified
Circuit or plated–through hole shorts to metal core substrate	3.7.5.2.1	500 V DC	500 V DC	750 V DC	As specified
Thermal stress.	3.7.6.2	Single float	Double float	Quad float	As specified
Product level C requirements	3.7.7	Not required	Not required	Not required	See table V
Qualification by similarity	4.2.4	Not allowed	Not allowed	Not allowed	As specified
Inspection of product for delivery	4.3.1	LCI	LCI and PCI on each lot	LCI and PCI on each lot	As specified
Test optimization	4.3.1.3	Allowed	Allowed	Not allowed	As specified
Test coupon correlation	A.3.1.1	Not required	Required	Required	As specified
Test coupons deliverables.	A.3.3	IPC-2221	IPC-2221 plus 1 breakaway A	IPC-2221 plus 2 breakaway A	As specified
Drilling roadmap	A.3.4.1	Not required	Required	Required	As specified
Drill bit resharpening	A.3.4.4	Allowed	Not allowed	Not allowed	As specified

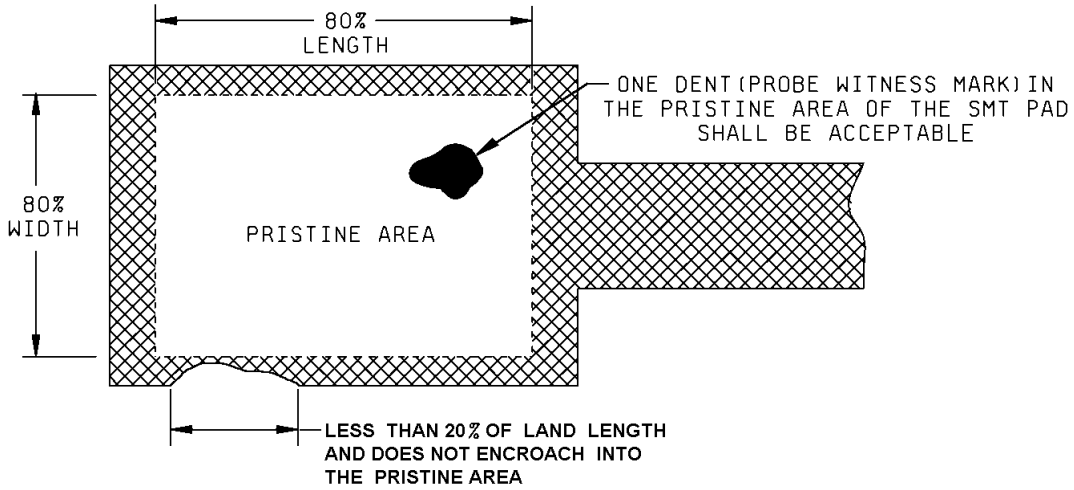


FIGURE 1. Rectangular surface mount lands.

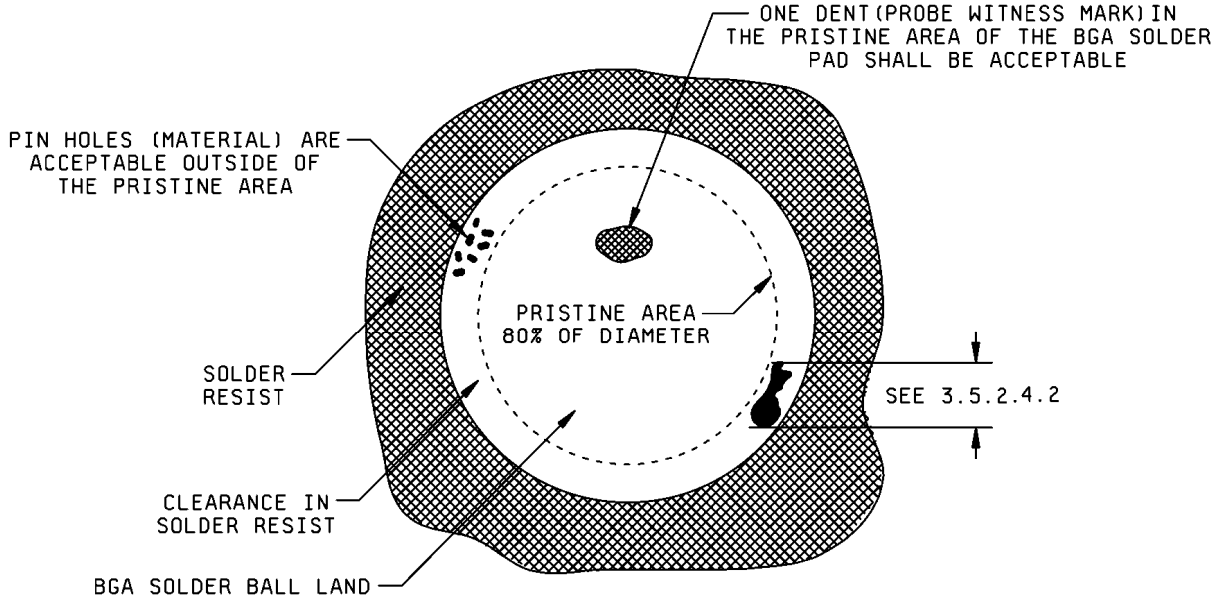


FIGURE 2. Round surface mount lands (BGA pads).

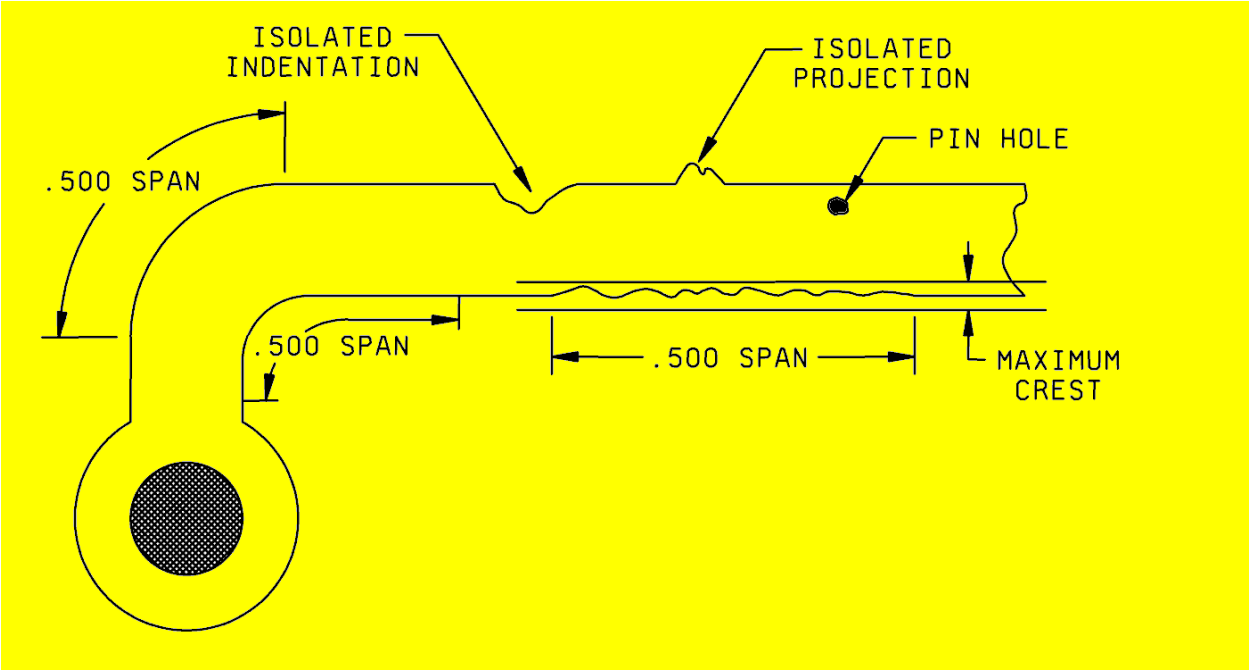


FIGURE 3. Conductor pattern imperfections.

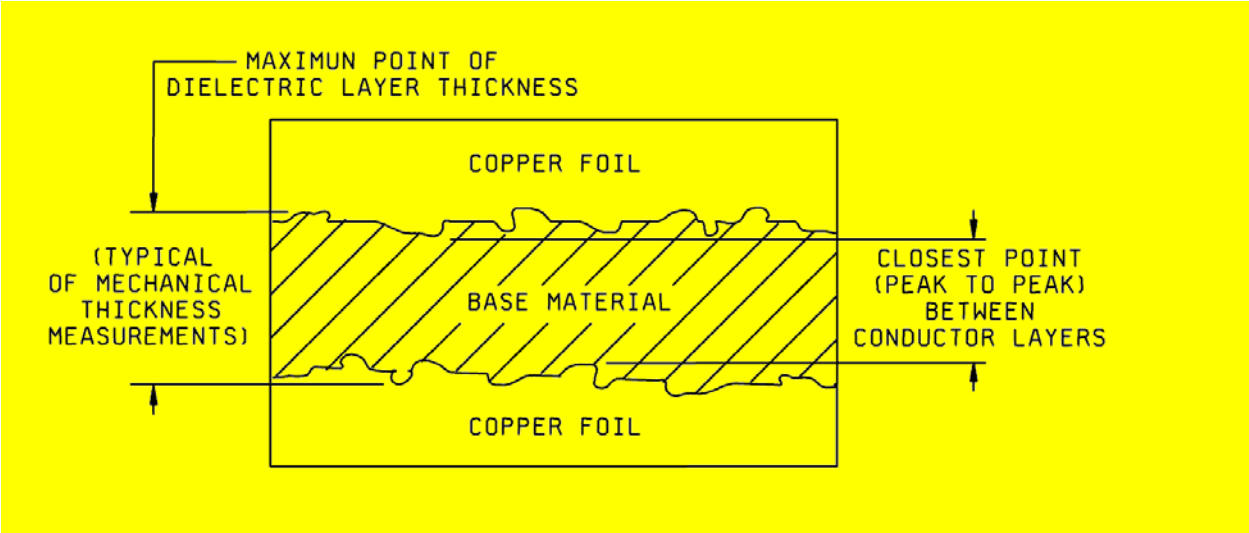


FIGURE 4. Dielectric thickness measurement.

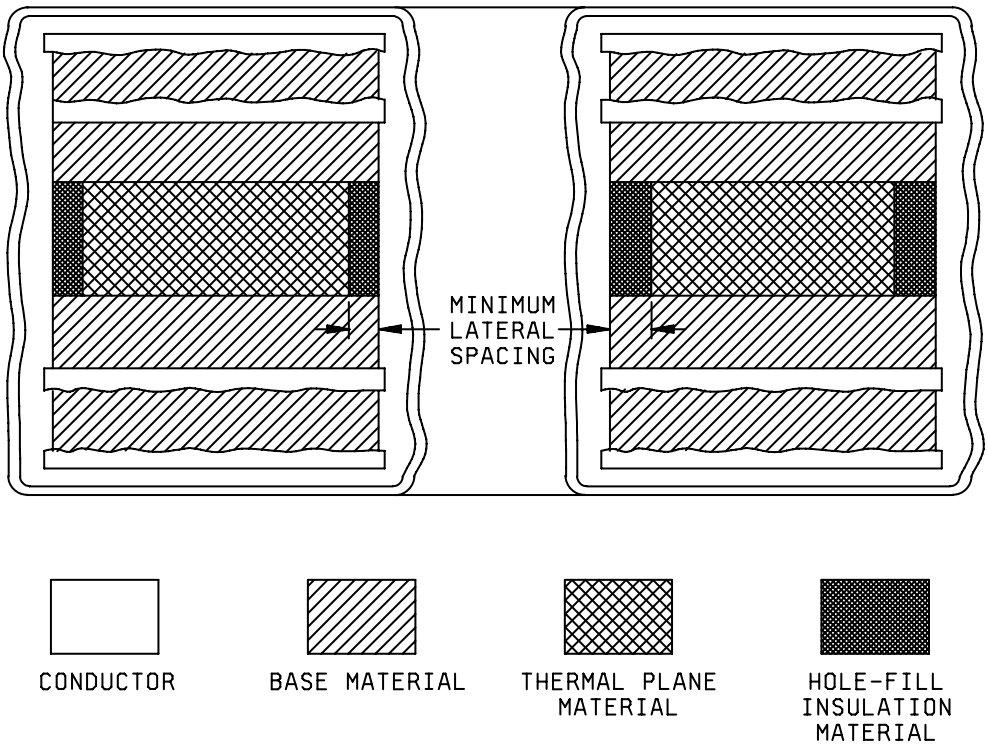


FIGURE 5. Metal core (constraining cores or heatsink plane) details.

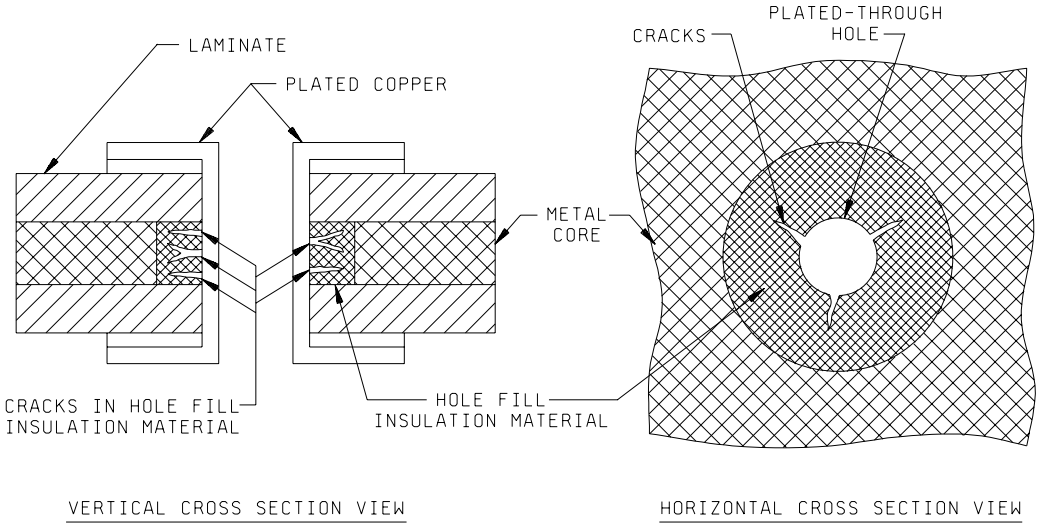
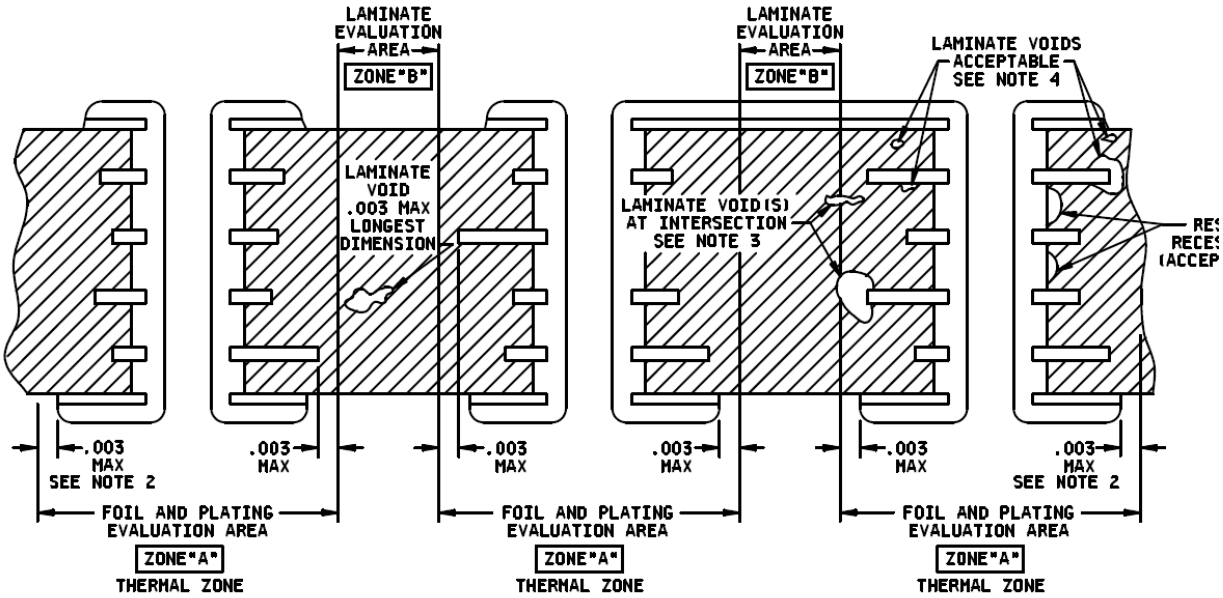


FIGURE 6. Insulation material cracks, metal cores or heatsink planes.



NOTES:

1. Dimensions are in inches.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than .0032 inch (0.08 mm) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.
5. Multiple adhesive voids between two adjacent plated-through holes in the same plane shall not have a combined length exceeding .02 inch (0.5 mm).

FIGURE 7. Typical plated-through hole cross section after ~~thermal stress~~ resistance to soldering heat or rework simulation.

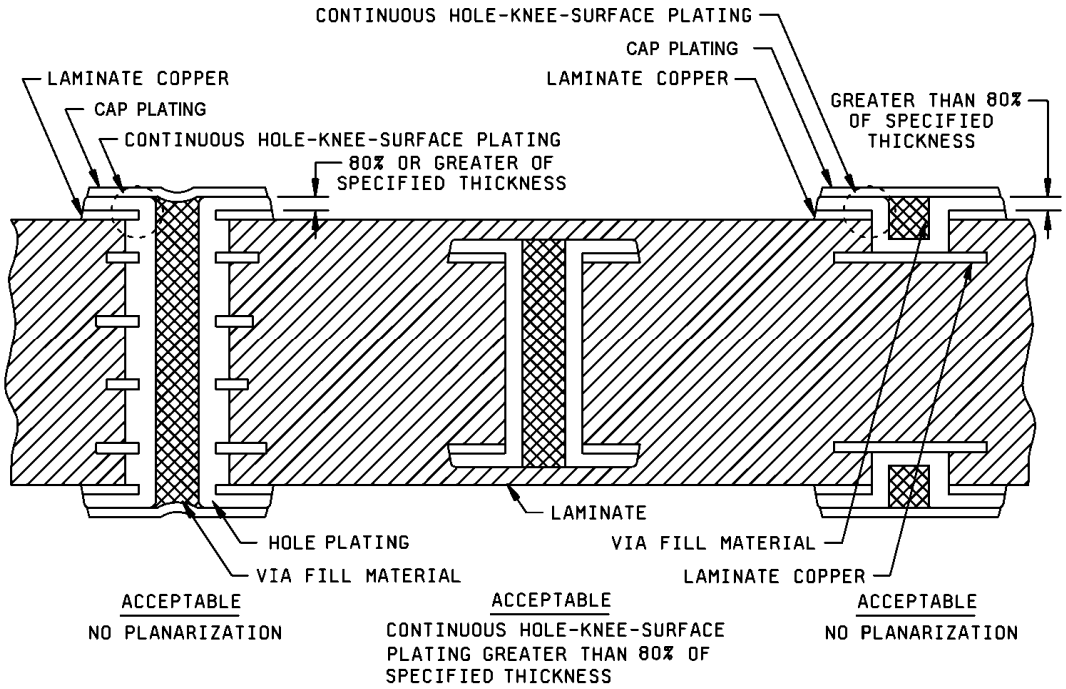


FIGURE ~~7~~ 8. Acceptable plated-through hole continuous hole-knee-surface copper plating.

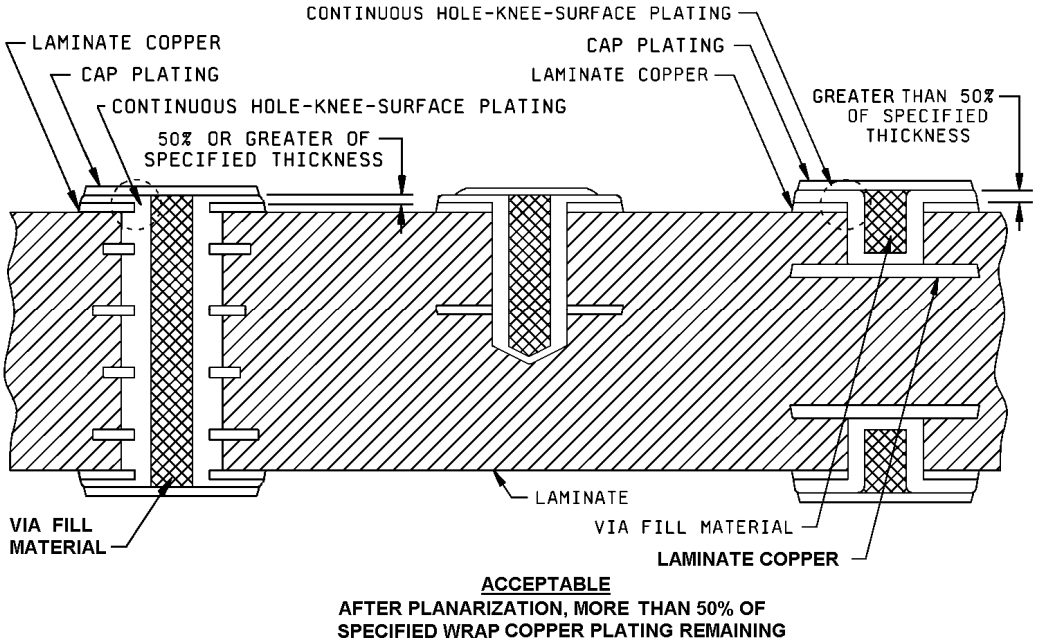


FIGURE ~~8~~ 9. Acceptable planarized plated-through hole continuous hole-knee-surface copper plating.

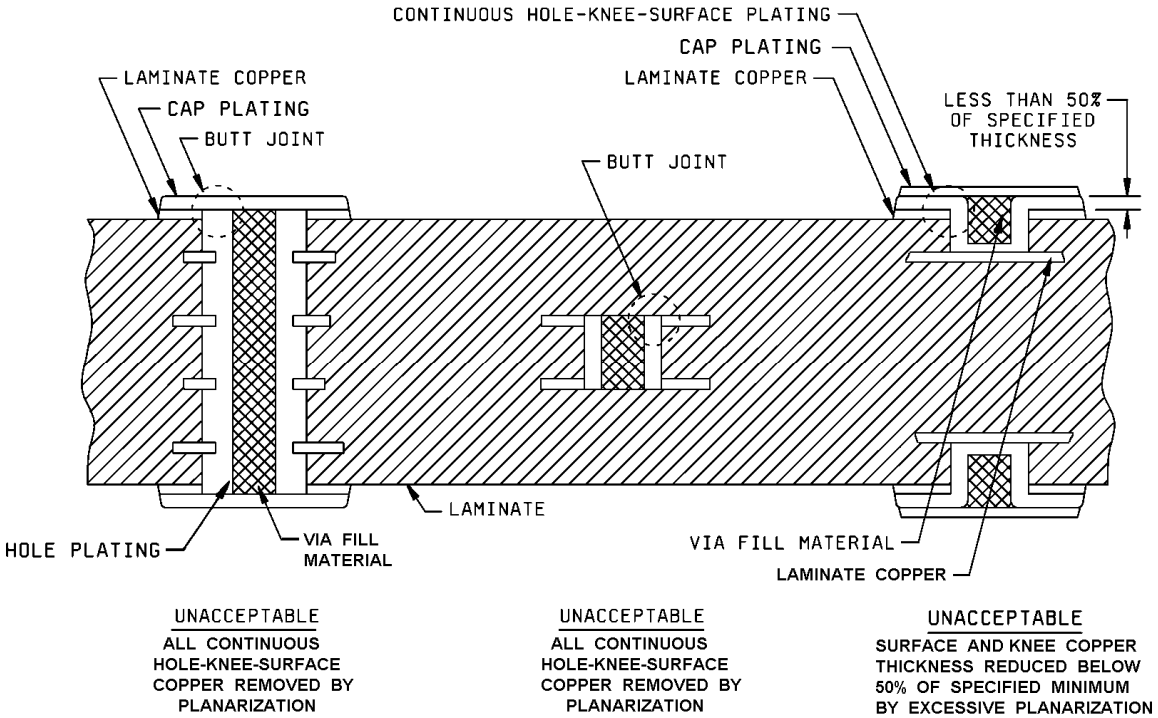


FIGURE ~~9~~ 10. Unacceptable planarized plated-through hole continuous hole-knee-surface copper plating.

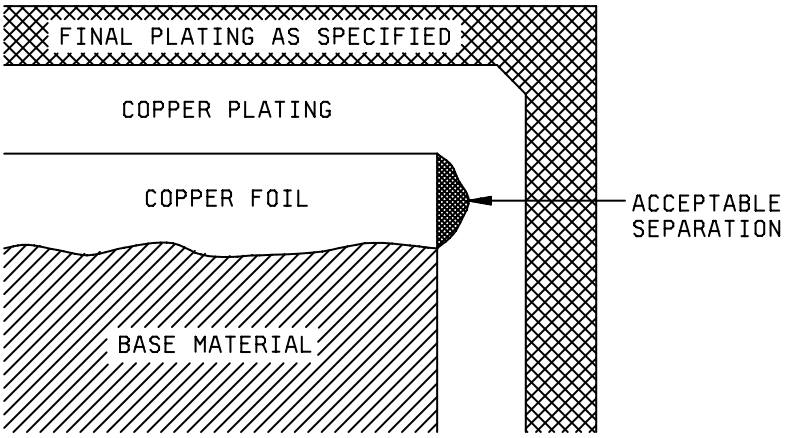


FIGURE 10 11. Acceptable separation at external foil.

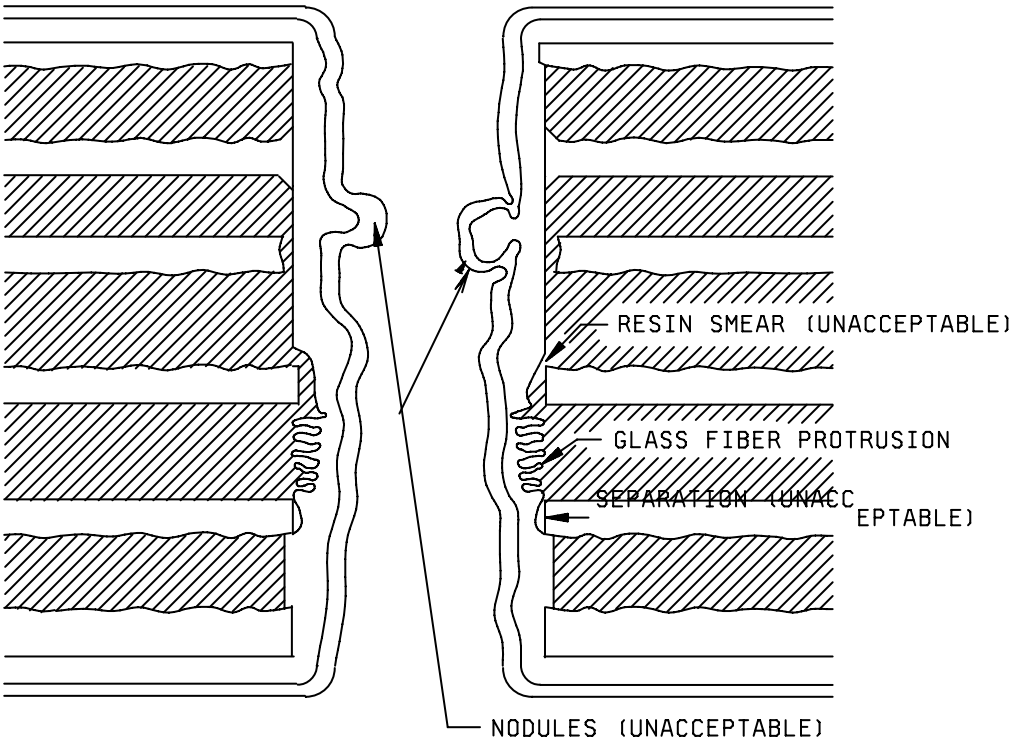


FIGURE 11 12. Plated through hole deficiencies.

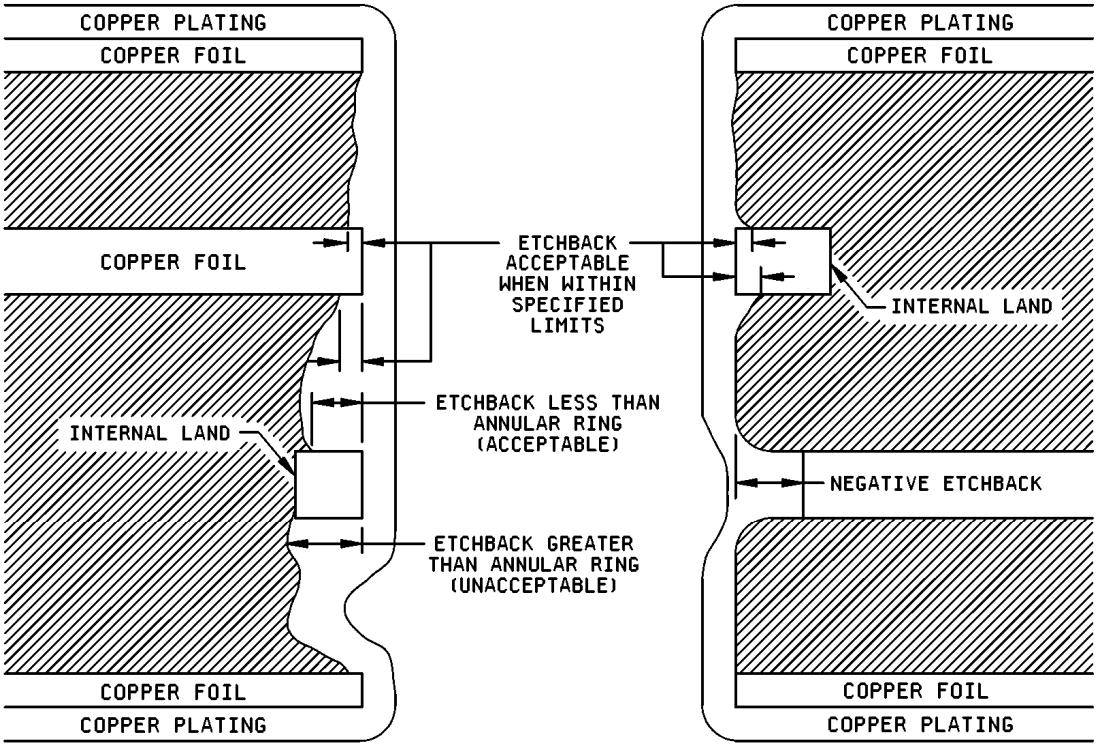


FIGURE 12 13. Etchback.

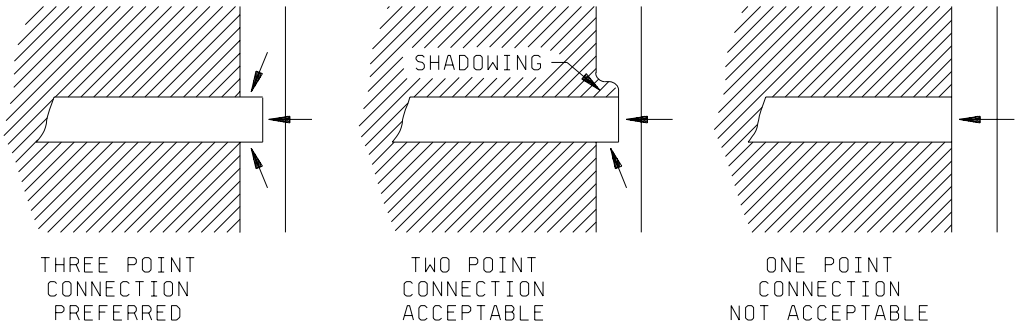


FIGURE 13 14. Forms of plating to internal layer connections.

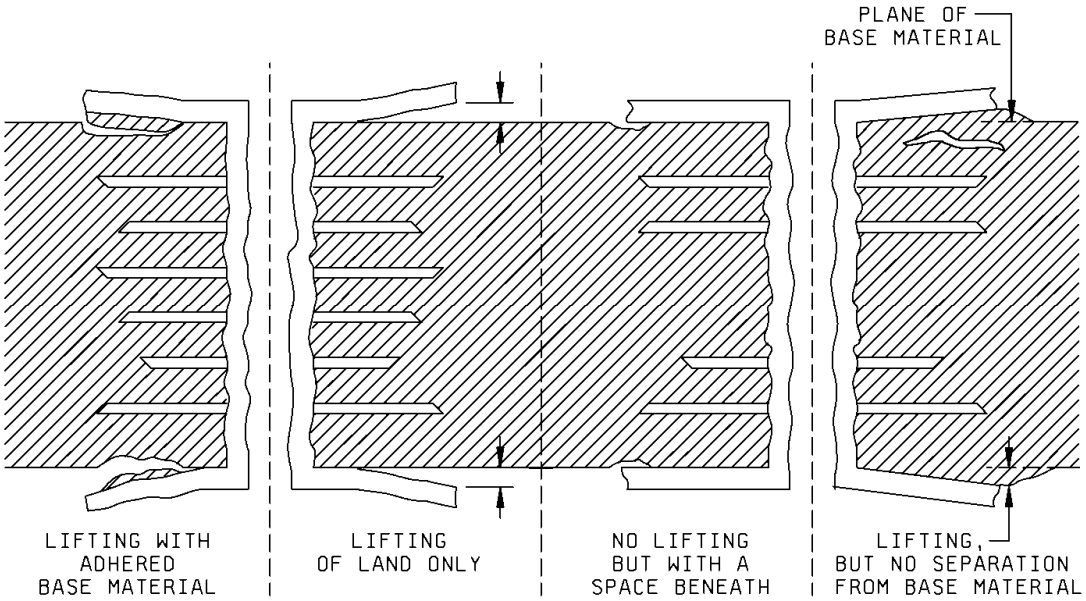


FIGURE 14 15. Lifted lands.

DESIGN, CONSTRUCTION, AND VERIFICATION OF
PRODUCT LEVELS T AND E

A.1 SCOPE

A.1.1 Scope. This appendix outlines additional QM program material that is applicable to products levels T and E for manufacturers of space and launch vehicle printed boards. This appendix is intended to be used by manufacturers in developing additional QM program steps needed to implement product levels T and E of this specification sheet. The QM program shall demonstrate the methods used to assure conformance to the applicable requirements of this appendix. For product levels T and E, this appendix is a mandatory part of this specification. The information contained herein is intended for compliance.

A.2 APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

A.3 REQUIREMENTS

A.3.1 Design and construction.

A.3.1.1 General. Printed board design and construction will be in accordance with the requirements specified herein and the applicable printed board procurement documentation. The design shall be capable of passing all applicable tests and inspections.

A.3.1.2 Base material.

A.3.1.2.1 Dielectric thickness. The minimum dielectric thickness shall be as specified. The dielectric material may be comprised of laminate, prepreg and laminate, or multiple layers of prepreg. Unless otherwise specified, there shall be no less than two layers of reinforcement, prepreg, laminate, or combination thereof, used between each pair of adjacent conductor layers. Unless otherwise specified, printed boards shall have a minimum of 0.089 mm (.0035 inch) of dielectric material between consecutive conductor layers (closest point between conductor layers), when cured.

A.3.1.2.2 Through via plugging. Unless otherwise specified, through via holes shall not be plugged. Vias shall meet the requirements of plated–through holes. When through-via hole plugging is required as specified, the via hole shall be plugged using the specified plugging material.

A.3.1.3 Conductor pattern.

A.3.1.3.1 Annular ring. Unless otherwise specified, the minimum annular ring shall be as specified herein. Unless otherwise specified, the 20 percent reduction allowance of 3.5.2.1 shall not reduce the annular ring below the following limits:

a. Unsupported holes: 0.38 mm (.015 inch) minimum.

b. External and internal annular ring for plated–through holes: 0.05 mm (.002 inch) minimum.

c. External plated–through holes adjoining a conductor: 0.13 mm (.005 inch) minimum.

A.3.1.3.2 Nonfunctional lands (internal layers). Nonfunctional lands shall be included on internal layers whenever clearance requirements permit.

A.3.1.4 Copper plating. Unless otherwise specified, the minimum copper plating thickness shall be as specified herein. Unless otherwise specified, the 10 percent reduction allowance of 3.6.4.1.1 shall not reduce the copper plating thickness below the following limits:

a. Buried via core and blind microvias: 0.02 mm (.0008 inch) minimum.

b. Plated–through holes, blind vias, and buried vias greater than two layers: 0.04 mm (.0015 inch) preferred, 0.03 mm (.0012 inch) minimum.

A.3.1.5 Solder coating thickness. The maximum solder coating thickness shall be as specified. Unless otherwise specified, the minimum solder coating thickness shall not be less than 0.004 mm (.00015 inch).

A.3.1.6 Solder ~~resist~~ mask thickness. The minimum solder ~~resist~~ mask thickness shall be as specified. Unless otherwise specified, the maximum solder ~~resist~~ mask thickness shall not be greater than 0.1 mm (.004 inch). Solder ~~resist~~ mask shall not tent though plated–holes or vias.

A.3.1.7 Tin–lead plating. Unless otherwise specified, tin–lead plating thickness shall be .0003 inch (x.XX mm) before fusing. There shall be no tin–lead plating on any surface that is to be terminated to an insulator, metal frame, heatsink, or stiffener.

A.3.1.8 Tin-lead fusing. Unless otherwise specified, after tin–lead plating and other processes, the printed board shall be fused. Only one fusing operation shall be permitted. The fuse time and temperature of each panel or printed board shall be traceable. After fusing, the solder coating shall be homogeneous and completely cover the conductors with no pitting, pinholes, or non-wetted areas. Touch-up of solder coating is permitted, but limited to no more than 5 percent of lands or pads.

A.4 VERIFICATION

A.4.1 Test coupons.

A.4.1.1 Panelization requirements. The panel position of product levels T and E test coupons shall be as specified by the design standard specified by the printed board procurement documentation, theTRB developed panel acceptance plan, and the requirements herein. Panels complying to product levels T and E shall have additional center of panel test coupons for when more than one printed board is on the production panel (see figure A-I). Acquiring activity supplied phototooling not having the required number, proper placement of test coupons, or having test coupons that do not conform to design parameters shall be reprocessed to correct any deficiencies.

A.4.1.2 Outer edge test coupon to center of panel test coupon plated–through hole correlation. The manufacturer shall define, demonstrate correlation, and utilize methods to verify the measurement and characteristics (plating thickness and plated–through hole quality) of the plated–through holes in test coupons on the edge of the production panel to those corresponding holes in the center of the panel or production printed board.

A.4.1.3 Test coupon to printed board design validation. Prior to lot conformance inspection, the manufacturer shall validate that the production printed board plated–through holes quality correlates with the associated test coupon plated–through hole quality. This requires the destructive physical analysis of at least one printed board and as a minimum shall be done on every product level T and E printed board design.

A.4.1.4 Process control test coupons. As many process control test coupons as necessary to ensure that the manufacturing processes are under statistical process control shall be required on each panel. The number of in-process test coupons will be determined by statistical process control sampling requirements. Unless otherwise specified, process control test coupons shall not be included in the shipment of the deliverable printed boards. Process control test coupons shall be identified and retained by the manufacturer under controlled storage conditions for the length specified (see 3.1). These test coupons may be used for lot conformance verifications.

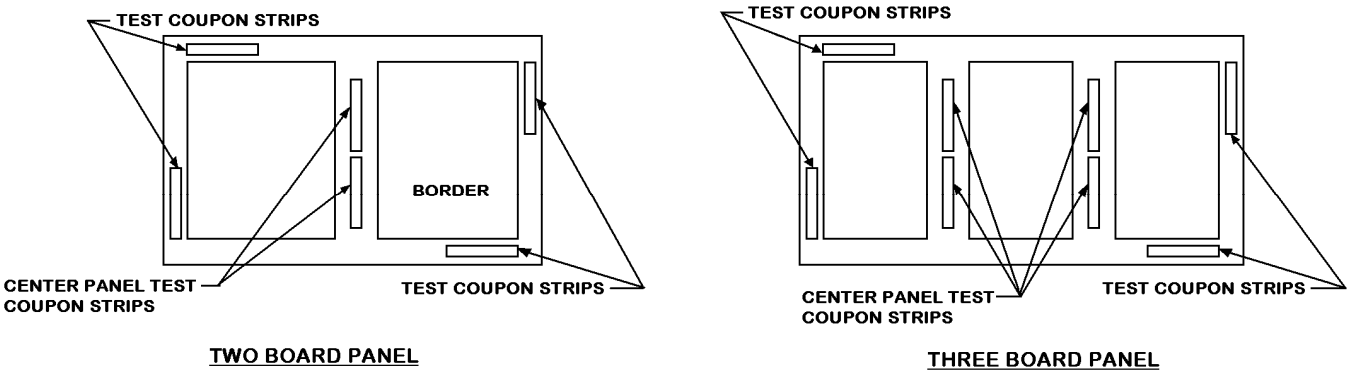


FIGURE A–1 Center of panel test coupons.

A.4.2 Test coupons deliverables. For product levels T and E, breakaway coupons shall be delivered attached to each production printed board. These deliverable test coupons shall be in addition to the MIL–PRF–31032 LCI and PCI test coupons or manufacturer specified process-control test coupons required for each panel.

a. Product level S: The number designated A or B test coupons for each printed board on the panel.

b. Product level T: The number and location shall comply with product level S, plus one additional break-away “A” test coupon for each printed board as a minimum.

c. Product level E: The number and location shall comply with product level S, plus two break-away “A” or “B” test coupons for each printed board.

d. For designs identified as small, two deliverable “A” or “B” test coupons for each 150 square centimeters of panel area shall be produced.

A.4.4 Mechanical drilling and drill bits.

A.4.4.1 Mechanical drilling workmanship test coupon. For product level E, mechanical drilling of component and via holes on the production panel shall be such that the use of each drill bit begins and ends on a designated drilling workmanship test coupon. Unless otherwise detailed in the TRB maintained QM plan, the manufacturer shall either design or specify a test coupon, which is not to be used in LCI or PCI testing, for the first and last drilled holes for each drill bit used on each production panel to verify drilled hole workmanship. Figure A–2 contains an example design for the drilling workmanship test coupon for a panel that uses 7 drill bits for one plated–through hole size.

A.4.4.2 Drilling roadmap The electronic data or program used to control the mechanical drilling process shall be programmed to drill the first and last holes of each drill bit across a row (laterally) starting at row 1, column 1 of the designated drilling workmanship test coupon. The drilling verification program shall be designed so that in the event that more drill bits are used during the manufacturing of a panel than are holes on the designated drilling workmanship test coupon, another test coupon on the panel is used in the same manner as the designated drilling workmanship test coupon.

A.4.4.3 Evaluation. At the completion of panel manufacturing, each row of drilled holes shall be cross sectioned to verify plated–through hole acceptability in accordance with the requirements of 3.6.

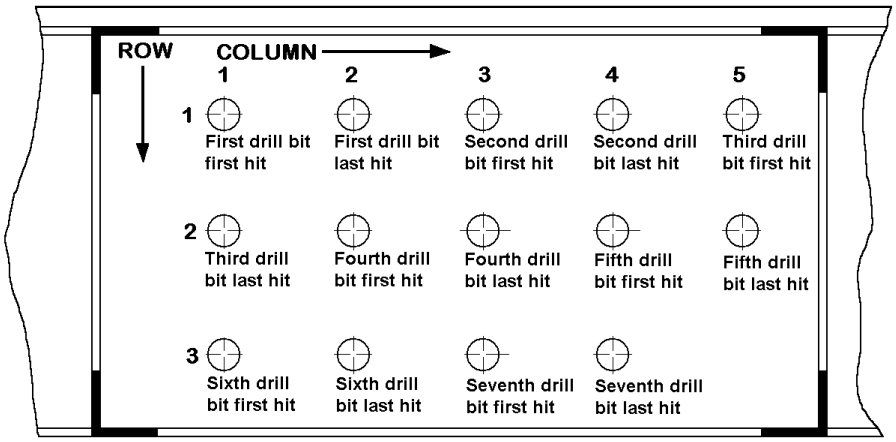


FIGURE A–2. Example of drilling workmanship test coupon.

A.4.4.2 Drill bit limit. The TRB shall develop and maintained a process to define, verify, and maintain a design matrix, which identifies the optimum number of drill hits allowed for the specific types of base materials, hole diameters, number of layers, and thickness of the copper layers used on the printed board.

A.4.4.3 Drill bit changes. All drill bit changes shall be documented. The record may be in the form of a drill tape or any digital storage medium.

A.4.4.4 Drill bit resharpening (product level E). For product level E, resharpened drill bits shall not be used for the drilling of plated–through holes.

A.4.4.5 Stacking. Unless otherwise specified, the stacking of panels during drilling shall not be acceptable.

A.4.5 Materials. The material shall be as specified herein. However, when a definite material is not specified, a material will be used which will enable the printed boards to meet the performance requirements of this specification sheet. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

A.4.5.1 Tin-lead plating thickness. Each printed board that uses tin-lead plating to arrive at a solder coating for a final conductor finish shall have a tin-lead plating thickness test coupon. The tin-lead plating thickness test coupons shall be removed from the inspection panel before fusing. This test coupon shall be used for verifying tin-lead plating thickness. Alternate measuring techniques such as x-ray fluorescence (see) may be used provided the verifying data comply with the traceability requirements of 3.9 and are retrieveable within the time limits specified (see 3.1).

PRODUCT LEVEL C

B.1 SCOPE

B.1.1 Scope. This appendix is intended to be used by users in defining product level C requirements and by manufacturers in understanding those specified requirements. This appendix is not a mandatory part of the specification sheet. The information contained herein is intended for guidance only.

B.2 APPLICABLE DOCUMENTS.

B.2.1 General. The documents listed in this section are specified in sections B.3 or B.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections B.3 or B.4 of this specification, whether or not they are listed.

B.2.2.1 Specifications, standards, or handbooks. The following specifications, standards, or handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 – Test Method Standard, Electronic and Electrical Component Parts.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

B.2.3 Non–Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

IPC-TM-650 – Test Methods Manual.
IPC-CC-830 – Qualification and Performance of Electrical Insulating Compound for Printed Board Assemblies.
IPC-9252 – Guidelines and Requirements for Electrical Testing of Unpopulated Printed Boards.

(Copies of this document are available online at http://www.ipc.org or from the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015–1249).

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD22-A102 – Accelerated Moisture Resistance - Unbiased Autoclave.

(Application for copies of these documents are available online at http://www.eia.org/ or from Electronic Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834)

(Non–Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

B.2.4 Order of precedence. In the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 OPTIONAL PERFORMANCE REQUIREMENTS

B.3.1 General. These optional requirements are specified in the printed board procurement documentation, therefore the documentation should be carefully reviewed to ensure that the exceptions taken will not adversely affect the performance of the printed board.

B.3.2 Reference to printed board procurement documentation. For the purposes of this specification sheet, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable printed board procurement documentation.

B.3.3 Product level C optional requirements.

B.3.3.1 Optional visual requirements.

B.3.3.1.1 Subsurface imperfections (when specified, see 3.1). Subsurface imperfections (such as foreign inclusions, laminate voids, etc.) shall be acceptable providing the following conditions are met:

a. The imperfections do not reduce conductor or dielectric spacing below the specified minimum requirements.

b. The imperfections do not propagate as a result of testing (such as rework simulation, ~~solder float thermal stress~~ resistance to soldering heat, or thermal ~~shock~~ cycling).

c. The longest dimension of any single imperfection is no greater than 0.80 mm (.032 inch). In non–circuitry areas, the maximum size shall not be greater than 2.00 mm (.079 inch) in the longest dimension or 0.01 percent of the printed board area, maximum.

d. Color variations or mottled appearance in bond enhancement treatments shall be acceptable. Random missing areas of treatment shall not exceed 10 percent of the total conductor surface area of the affected layer.

e. Blistering, delamination, haloing, measling, or crazing shall not be acceptable.

B.3.3.1.2 Laser marking legibility test (applicable to laser marked printed boards) (when specified, see 3.1). When printed board specimens are tested as specified in B.4.3.1.1, the marking shall remain legible.

B.3.3.1.3 Surface examination (when specified, see 3.1). When specified, the surface of the printed board specimen shall be inspected for additional criteria detailed in the printed board procurement documentation.

B.3.3.2 Optional dimensional requirements.

B.3.3.2.1 Hole size, drilled (when specified, see 3.1). When drilled holes are inspected in accordance with B.4.7.2.1, the hole size shall be within the specified tolerance.

B.3.3.2.2 Hole size, plated (when specified, see 3.1). When plated–through holes are inspected in accordance with B.4.7.2.2, the hole size shall be within the specified tolerance.

B.3.3.3 Optional chemical requirements.

B.3.3.3.1 Organic contamination (when specified, see 3.1). When non solder ~~resist~~ mask coated printed boards are tested in accordance with B.4.3.1.1, any visual evidence of organic residue shall constitute a failure.

B.3.3.4 Optional physical requirements.

B.3.3.4.1 Coefficient of thermal expansion (CTE) (when specified, see 3.1). When tested as specified in B.4.3.4.1, printed board test specimens that have metal cores or other constraining materials and a requirement to constrain the thermal expansion in the planar directions, the CTE shall be within ± 2 ppm per degree Celsius for the CTE and temperature range specified.

B.3.3.4.2 Die bond adhesion (when specified, see 3.1). When tested as specified in accordance with B.4.3.4.2, the die attach area shall exhibit a minimum shear strength as follow:

a. All die area larger than 4.0 square mm (64x10E-4 square inch) shall withstand a minimum force of 2.5 kg.

b. All die area smaller than or equal to 4.0 square mm (64x10E-4 square inch) shall withstand a minimum force of 62.5 kg per square cm.

B.3.3.4.3 Time to delamination (when specified, see 3.1). When tested as specified in B.4.3.4.3, printed board test specimens shall be tested until the time to delamination. The time to delamination is determined as the time from the onset of the isotherm to failure.

B.3.3.4.4 Wire bond adhesion (when specified, see 3.1). When inspected as specified in B.4.3.4.4, plated bonding areas shall be capable of meeting the requirements of table I of method number 2.4.42.3 of IPC-TM-650 without incurring any of the following failures:

a. Wire bond failure (interface between wire and conductive layer).

b. Separation of conductive layers on the bonding area.

c. Bonding area lifted from the base material.

B.3.3.5 Optional electrical requirements.

B.3.3.5.1 Characteristic impedance of conductors (when specified, see 3.1). When conductors are tested as specified in B.4.3.5.1, the characteristic impedance shall be within the specified tolerance of the nominal impedance (see 3.1).

B.3.3.5.2 Surface insulation resistance (as received)(when specified, see 3.1). When tested as specified in B.4.3.5.2, the resistance between mutually isolated conductors shall be greater than 500 megohms.

B.3.3.6 Optional environmental requirements.

B.3.3.6.1 Accelerated moisture resistance (when specified, see 3.1). After undergoing the test specified in B.4.3.6.1, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. A resistance increase of 10 percent or more shall be considered a reject.

B.3.3.6.2 DC current induced thermal cycling (when specified, see 3.1). After undergoing the test specified in B.4.3.6.2, the printed board test specimen shall be inspected in accordance with 4.7.2 and shall meet the requirements of 3.5.

B.3.3.6.3 Fungus resistance (when specified, see 3.1). All external materials shall be non-nutrient to fungus growth or shall be suitably treated to retard fungus growth. The manufacturer shall certify that all external materials are fungus resistant or shall perform the test specified in B.4.3.6.3. There shall be no evidence of fungus growth on the external surfaces.

B.3.3.6.4 Mechanical shock (specified pulse) (when specified, see 3.1). After undergoing the test specified in B.4.3.6.4, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. The requirements of 3.5 shall be met when specified.

B.3.3.6.5 Radiation hardness (when specified, see 3.1). When printed board specimens are tested as specified in B.4.3.6.5, there shall be no defects such as measling, delamination or weave texture. The insulation resistance between conductors shall be not less than 500MΩ. After the test, the requirements specified in 3.7.5.3 (DWV) shall be satisfied.

B.3.3.6.6 Barometric pressure, reduced (when specified, see 3.1). When printed board specimens are tested as specified in B.4.3.6.6, there shall be no momentary or intermittent arcing or other indication of breakdown, nor shall there be any visible evidence of damage.

B.3.3.6.7 Vibration.

B.3.3.6.7.1 Vibration, sinusoidal (when specified, see 3.1). After undergoing the test specified in B.4.3.6.7.1, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. Unless otherwise specified (see 3.1), the requirements specified in 3.5.1.2, 3.5.1.3, and 3.7.4.4 shall be met.

B.3.3.6.7.2 Vibration, resonance dwell (when specified, see 3.1). After undergoing the test as specified in B.4.3.6.7.2, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. Unless otherwise specified (see 3.1), the requirements specified in 3.5.1.2, 3.5.1.3, and 3.7.4.4 shall be met.

B.4 PRODUCT LEVEL C VERIFICATIONS

B.4.1 General. The verification provided in this section are intended to provide a product level C printed board.

B.4.2 Responsibility for inspection. Unless otherwise specified in the contract or order, the manufacturer is responsible for the performance of all inspection requirements as specified in the printed board procurement documentation.

B.4.2.1 Inspection during manufacture. The manufacturer shall establish and maintain in-process production controls, quality controls and inspections at appropriately located points in the manufacturing process in accordance with the procedures described by its TRB to assure continuous control of quality of materials, subunits, and parts during manufacture and testing. These controls and inspections shall be adequate to assure compliance with the applicable printed board procurement documentation.

B.4.3 Product level C verifications.

B.4.3.1 Optional visual verifications.

B.4.3.1.1 Visual and mechanical inspection. Unless otherwise specified, printed board specimens shall be examined under 30X to 60X magnification. In case of conflict, 30X will be the referee power, unless otherwise specified, to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see 3.1, 3.4, 3.5.1 through 3.5.4.6 inclusive, and 3.9).

B.4.3.1.2 Laser marking legibility test. Printed board specimens shall be coated with 0.13 mm (.005 inch) minimum of silicon resin insulating compound, type SR in accordance with IPC-CC-830. After curing, coated printed board specimens shall be examined for legibility under normal production room lighting by an inspector at 10X magnification.

B.4.3.1.3 Surface examination. The surface of the printed board specimen shall be inspected for workmanship in accordance with test method number 2.1.5 of IPC-TM-650.

B.4.3.1.4 Workmanship. The printed board specimen shall be inspected for workmanship in accordance with test method number 2.1.8 of IPC-TM-650.

B.4.3.2 Optional dimensional verifications.

B.4.3.2.1 Hole size, drilled. The measurement for drilled hole size shall be in accordance with test method number 2.2.6 of IPC-TM-650. Finished hole size tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of measurements for each hole size shall be documented in the QM plan, determined by the TRB to adequately sample the quantity of holes within the population.

B.4.3.2.2 Hole size, plated. The measurement for plated–through hole size shall be in accordance with test method number 2.2.7 of IPC-TM-650. Finished hole size tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of measurements for each hole size shall be documented in the QM plan, determined by the TRB to adequately sample the quantity of holes within the population.

B.4.3.3 Optional chemical verifications.

B.4.3.3.1 Organic cleanliness. The measurement for organic contamination shall be in accordance with test method numbers 2.3.38 and 2.3.39 of IPC-TM-650. If evidence of organic contamination is detected by test method 2.3.38 of IPC-TM-650, then test method number 2.3.39 of IPC-TM-650 shall be used to determine the nature of the contaminant.

B.4.3.4 Optional physical verifications.

B.4.3.4.1 Coefficient of thermal expansion (CTE). The test for CTE shall be performed in accordance with test method number 2.4.41.2 of IPC-TM-650.

B.4.3.4.2 Die bond adhesion. The test for die bond adhesion shall be performed in accordance with test method number 2.4.42.2 of IPC-TM-650.

B.4.3.4.3 Time to delamination. The test for time to delamination resistance shall be performed in accordance with test method number 2.4.24.1 of IPC-TM-650.

B.4.3.4.4 Wire bond adhesion. The test for wire bond adhesion shall be performed in accordance with test method number 2.4.42.3 of IPC-TM-650.

B.4.3.5 Optional electrical verifications.

B.4.3.5.1 Characteristic impedance of conductors. When specified in the applicable printed board procurement documentation, perform characteristic impedance testing for conductors in accordance with test method number 2.5.5.7 of IPC-TM-650. The characteristic impedance shall meet the requirements specified in the applicable printed board procurement documentation.

B.4.3.5.2 Surface insulation resistance (as received). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.3.5 of IPC-TM-650. The following details and exceptions apply:

a. Sample preparation. Test coupons or production printed boards should be conditioned at 50 ±5 degrees Celsius with no added humidity for a period of 24 hours.

b. Test routine. After cooling, the insulation resistance test shall be performed in accordance with the ambient temperature measurements specified in test condition B of test method number 2.6.3 of IPC-TM-650.

B.4.3.6 Optional environmental verifications.

B.4.3.6.1 Accelerated moisture resistance. The accelerated moisture resistance testing of printed board test specimens shall be performed in accordance with test condition C of JESD22-A102. Test exposure times shall be 96 hours. Final measurements shall be made at room temperature.

B.4.3.6.2 DC current induced thermal cycling. The test for DC current induced thermal cycling shall be performed in accordance with test method number 2.6.26 of IPC-TM-650.

B.4.3.6.3 Fungus resistance. The test for fungus resistance shall be performed in accordance with test method number 2.6.1 of IPC-TM-650.

B.4.3.6.4 Mechanical shock. The test for mechanical shock shall be performed in accordance with test method number 2.6.5 of IPC-TM-650. The following details and exceptions apply:

a. Test specimen: The test specimen shall test coupons or production printed boards as specified.

b. Method of mounting: The test specimens shall be restrained from movement as specified or if not specified, secured on all four corners to a rigid fixture.

c. Number and direction of blows: The test specimens shall be subjected to three blows in each of the three mutually perpendicular axes.

d. Shock pulse waveform: The shock pulse shall be 100Gs with a duration of 6.5 ms per pulse.

e. Measurements: Unless otherwise specified, after the test the test specimen shall comply with 3.7.5.

B.4.3.6.5 Radiation hardness. The test specimen shall be exposed to gamma ray irradiation by using cobalt 60 at a rate of 0.5×10E4 Gray to 1×10E4 Gray per hour until the total dose amounts to 1×10E4 Gray. After the irradiation, the test specimen shall be inspected visually to verify that there is no degradation in any part of the specimen. The tests of moisture insulation resistance and dielectric withstanding voltage shall be performed in accordance with 4.7.6.1 and 4.7.5.3, respectively. The insulation resistance shall be measured using the same circuit pattern used for the dielectric withstanding voltage test.

B.4.3.6.6 Reduced barometric pressure for qualification only. Printed board specimens shall be tested in accordance with method 105 of MIL-STD-202. The following details shall apply:

a. Method of mounting: Normal mounting means.

b. Test condition: G (200,000 meterst).

c. Test during subjection to reduced pressure: 150 percent of rated voltage shall be applied between the terminals for not less than 1 minute.

d. Examination after test: Printed board specimens shall be visually examined for evidence of damage.

B.4.3.6.7 Vibration.

B.4.3.6.7.1 Vibration, sinusoidal. The test for vibration, sinusoidal waveform, shall be tested in accordance with test method number 2.6.9 of IPC-TM-650. The following details and exceptions apply:

a. Test specimen: The test specimen shall test coupons or production printed boards as specified.

b. Method of mounting: The test specimens shall be restrained from movement as specified or if not specified, secured on all four corners to a rigid fixture.

c. Waveform: The cycling test shall consist of one sweep from 20 to 2000 Hz performed in 16 minutes. Input acceleration over the 20 to 2000 Hz frequency range shall be maintained to 15 Gs.

d. Measurements: Unless otherwise specified, after the test the test specimen shall show no evidence of delamination and comply with the requirements of 3.7.5.

B.4.3.6.7.2 Vibration, resonance dwell. The test for vibration, resonance dwell, shall be tested in accordance with test method number 2.6.9 of IPC-TM-650. The following details and exceptions apply:

a. Test specimen: The test specimen shall test coupons or production printed boards as specified.

b. Method of mounting: The test specimens shall be restrained from movement as specified or if not specified, secured on all four corners to a rigid fixture.

c. Waveform: Test coupons or production boards shall be subjected to a 30 minute resonance dwell with 25 Gs input or a maximum of 100 Gs output measured at the geometric center of the test coupon or production board. The test coupons or production board shall be restrained from movement by fixturing on all four sides.

d. Measurements: Unless otherwise specified, after the test the test specimen shall show no evidence of delamination and comply with the requirements of 3.7.5.

CRITICAL DESIGN, CONSTRUCTION, AND MATERIALS

C.1 SCOPE

C.1.1 Scope. This appendix contains critical design, construction and material information which will assist manufacturers in producing printed boards which meet the requirements of 3.5 and 3.6. This appendix is not a mandatory part of the specification sheet. The information contained herein is intended for guidance only.

C.2 APPLICABLE DOCUMENTS.

This section is not applicable to this specification sheet.

C.3 DESIGN, CONSTRUCTION, AND MATERIALS

C.3.1 General. Printed board design, construction, and materials should be in accordance with the guidance specified herein.

C.3.2 Design. Printed boards using the design guidelines herein should be capable of passing all applicable tests and inspections.

C.3.2.1 Annular ring. Unless otherwise specified, the minimum annular ring should be as specified herein. Unless otherwise specified, the 20 percent reduction allowance of 3.5.2.1 should reduce the annular ring below the following limits:

a. Unsupported holes: 0.38 mm (.015 inch) minimum.

b. External and internal annular ring for plated–through holes: 0.05 mm (.002 inch) minimum.

c. External plated–through holes adjoining a conductor: 0.13 mm (.005 inch) minimum.

C.3.2.2 Copper plating. Unless otherwise specified, the minimum copper plating thickness should be specified herein. Copper plating thickness below the following limits:

a. Buried via core and blind microvias: 0.02 mm (.0008 inch) minimum.

b. Plated–through holes, blind vias, and buried vias greater than two layers: 0.04 mm (.0015 inch) preferred, 0.03 mm (.0012 inch) minimum. Any copper thickness less than 0.001 inch should considered a void.

c. Blind and buried vias more than three layers should comply with the requirement.

C.3.2.3 Dielectric thickness. The minimum dielectric thickness should as specified. The dielectric material may be comprised of laminate, prepreg and laminate, or multiple layers of prepreg. Unless otherwise specified, there should be no less than two layers of reinforcement, prepreg, laminate, or combination thereof, used between each pair of adjacent conductor layers. Unless otherwise specified, printed boards should have a minimum of 0.089 mm (.0035 inch) of dielectric material between consecutive conductor layers (closest point between conductor layers), when cured.

C.3.2.4 Ground plane distribution. Multilayer printed wiring boards should be configured so as to equalize the distribution of conductive areas in a layer and the distribution of conductive areas among layers. Ground planes should be balanced around the mid point to maintain printed board flatness.

C.3.2.5 Solder coating thickness. The maximum solder coating thickness shall be as specified. Unless otherwise specified, the minimum solder coating thickness should not be less than 0.004 mm (.00015 inch).

C.3.2.6 Solder ~~resist~~ mask thickness. The minimum solder ~~resist~~ mask thickness shall be as specified. Unless otherwise specified, the maximum solder ~~resist~~ mask thickness should not be greater than 0.1 mm (.004 inch). Solder mask should not tent though plated–holes or vias.

C.3.2.7 Wire bond pad roughness. The maximum conductor finish roughness for area designated for wire bonding should be no greater than 0.8 micrometers (32 micro inches).

C.3.2.8 Nonfunctional lands (multilayer designs). Nonfunctional lands should be included on internal layers of multilayer boards whenever clearance requirements permit.

C.3.3 Construction.

C.3.3.1 Copper treatment. The surfaces of the copper on all inner layers of multilayer printed wiring boards to be laminated should be treated or primed prior to lamination to improve the laminate bonding. A copper oxidation technique is an acceptable treatment prior to lamination.

C.3.3.2 Hot air solder leveling. Printed boards should be only hot air leveled once. The solder coating should be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but is limited to no more than 5 percent of lands or pads.

C.3.3.3 Fusing. After tin-lead plating and other processes, unless otherwise specified, the printed wiring board should be fused. Only one fusing operation is permitted. The fuse time and temperature should be documented. After fusing, the solder coating should be homogeneous and completely cover the conductors with no pitting, no pinholes, or non-wet areas. Sidewalls of conductors need not be solder coated. Touch-up is permitted but is limited to no more than 5 percent of lands or pads.

C.3.3.5 Stacking. Stacking is not permitted for multilayered or double sided boards.

C.3.3.6 Through via filling. Unless otherwise specified, through via holes should not be plugged. Vias should meet the requirements of plated–through holes. When through-via hole plugging is required as specified, the via hole should be plugged using the specified plugging material.

C.3.4 Materials.

a. All materials on the delivered printed board should meet the outgassing requirements of NASA 1124.

b. All adhesives. base materials, and solder ~~resists~~ masks materials shall be capable of meeting the solder heat resistance requirements of 288ºC for 10 seconds, and a withstanding voltage of 30kV/mm. Various performance tests should confirm material requirements.

c. Permanent solder mask should comply with IPC-SM-840, class H.

d. Prohibited materials. Pure tin may not be used to coat any surface nor shall it be used as an undercoat. If tin is used as an etch resist, it should be totally removed prior to the final conductor finish application.

Custodians:
Army – CR
Navy – EC
Air Force – 11
DLA – CC

Preparing activity:
DLA – CC

(Project: See EP study cover letter.)

Review activities:
Army – MI
Air Force – 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at http://assist.daps.dla.mil.