ENGINEERING PRACTICE (EP) STUDY

TITLE: Proposed New Class Y (Non-Hermetic Microcircuits For Space Application) Requirements For MIL-PRF-38535.

Study project number: 5962-2011-006

FINAL REPORT

Study Conducted by DLA Land and Maritime-VAC

February 24, 2012

Prepared by:
Muhammad Akbar
DLA Land and Maritime-VAC

EP study on class Y (Non-hermetic microcircuits for space application)

I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study was to obtain input and justification from the military services, microcircuit manufacturers, and space application user communities concerning the addition of new class Y (Non-hermetic microcircuits for space application) to MIL-PRF-38535.

II. BACKGROUND: Design requirements of modern electronics systems are growing faster and moving forward with an advance in complex technologies. Considering complexity of new technologies and device packaging techniques, G-12 formed a task group (TG) for exploring the class Y concept and to develop the requirements for qualification and screening of non-hermetic microcircuits packages for space applications. Accordingly, to bring advancement and adopting new technologies into QML system to MIL-PRF-38535, DLA Land and Maritime was conducted an EP study on the proposed new class Y (Non-hermetic microcircuits for space application) to MIL-PRF-38535.

The goal of this EP study was to develop a consensus document containing standard requirements in appendices, including screening and TCI/QCI requirements for incorporating into MIL-PRF-38535. Proposed class Y requirements will impact many sections, texts, tables and appendices of MIL-PRF-38535.

III. RESULTS: The EP Study initial draft with proposed screening, TCI/QCI requirements along with class Y survey questionnaire was distributed to military services, microcircuit manufacturers, and space application users for review and comment during the time period of July 25, 2011 through September 10, 2011.

Comments received and discussed at the G-12 task group Class Y meeting on October 3, 2011 at the JEDEC conference in Columbus, Ohio. DLA Land and Maritime and the Class Y task group discussed many complex aspects like the definition of class Y, suppliers qualification, requirements for BGA/CGA package including self life issues, underfill materials qualification and electrical test after column attachment at full military temperature ranges for CGA package during JEDEC conference on October 2011 to February 2012. After numerous discussions with all parties, DLA Land and Maritime-VAC has developed a formatted document that includes class Y devices screening, TCI/QCI requirements and update Appendix B requirements (see attachment) to wrap up the EP study on class Y.

IV. CONCLUSIONS: All received comments on this EP study were reviewed and discussed by the DLA Land and Maritime and JEDEC, G-12 class Y task group. After review and examine all comments DLA Land and Maritime has developed a formatted document that includes class Y devices screening, TCI/QCI requirements and Appendix B requirements which need to be finalized for inclusion to MIL-PRF-38535.

V. RECOMMENDATION: DLA Land and Maritime is requesting military services and industry representatives, the class Y task group and Space users to review class Y requirements (see attachment). Any comments on this final study report shall be submitted to: Muhammad.akbar@dla.mil no later than April 24, 2012. The results of this study will provide a basis of the next MIL-PRF-38535 spec action.

ATTACHMENT

EP study on Class Y (Non-hermetic microcircuits for space application)

The Class Y definition:

Class Y. The class Y device shall be defined as ceramic non-hermetic package, and meet all applicable appendices requirements of this specification including qualification, screening and TCI/QCI requirements, and shall be passed all applicable requirements of Appendix B herein.

Manufacturer Qualification:

Manufacturer shall have QML class Q level certification/qualification prior to supply class Y device.

Recommendation:

1. **Board level testing for BGA/CGA package.**

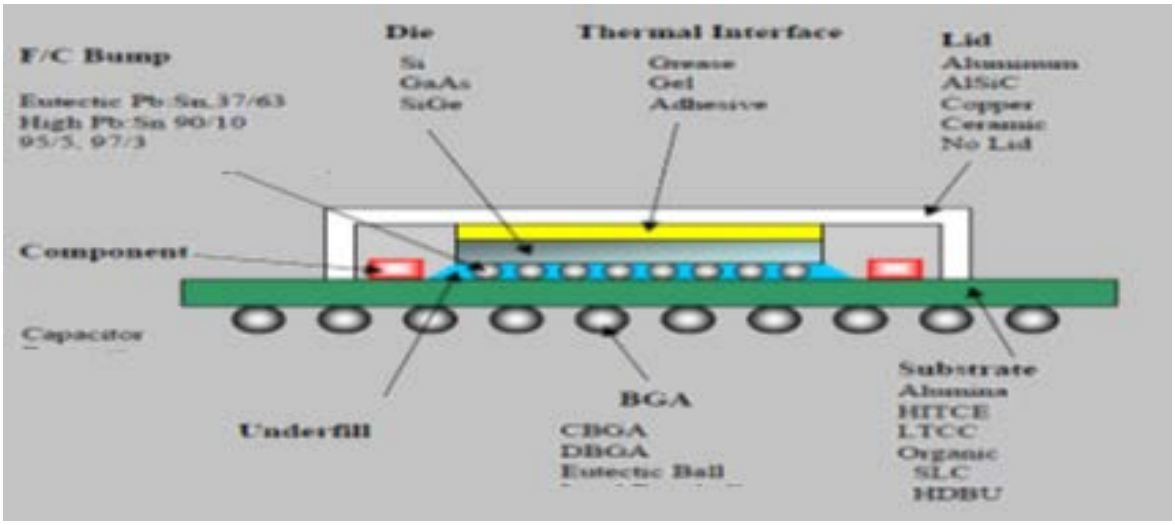
   - Board level testing is totally beyond the scope of MIL-PRF-38535.

2. **Underfill and/or thermal grease/epoxy to expose in atmosphere moistures:**

   - The under fill material and lid attach epoxy shall meet TM5011
   - Must be addressed in the package integration demonstration test plan (PIDTP)
   - HAST test shall be performed for moisture resistance of the under fill and lid attach materials.
   - Both X-ray and CSAM should be performed on underfill as they detect different types of defects.

3. **Electrical tests after column/ball attach at -55/ 25/125°C**

   - Electrical test shall be performed across the full temperatures ranges prior to attach ball/columns on the package to ensure bumps/solder/epoxy integrity.
   - After ball attach (BGA package) electrical test shall be performed across the full military temperatures ranges.
   - After column attach (CGA package) electrical test shall be performed at 25°C as a minimum to verify no electrically/mechanically damage have been introduced due to the attach process.



(For an example of typical flip chip device, please do not use this figure to justify Class Y device.)

ATTACHMENT

TABLE IC. Microcircuit screening procedure for ceramic non-hermetic class Y QML microcircuits.

Screening Test	MIL-STD-883, test method (TM), condition and minimum sample size quantity(accept no)	
1. Wafer lot acceptance test 1/	TRB plan (see H.3.2.1.4) and TM 5007 MIL-STD-883	100%
2. Internal visual inspection (check internal materials, construction and workmanship)	TM 2010 condition A & inspection of Bumps	
3. Temperature cycling /Thermal shock	For TC= TM 1010 test condition C, 50 cycles minimum	
4. Constant acceleration (high stress test) 2/	TM 2001, test condition E (see J.3.4)	
5. Serialization 3/	Laser marking is required (In accordance with device specification)	
6. Interim pre burn-in electrical 4/ 5/	Interim pre burn-in static & dynamic @25°C	
7. Burn-in test: 6/ 7/ a. Static burn-in b. Dynamic burn-in	TM 1015 a. 140 hrs@125°C, condition B b. 240 hrs@125°C, condition D	
8. Interim post burn-in electrical 4/ 5/	Interim post burn-in static & dynamic@25°C	
9. Reverse bias burn-in 9/	TM 1015, Condition A or C; 72 hours at +150°C minimum (100%)	
10 PDA or alternate procedure for lot acceptance test 4/ 8/	5 percent PDA on subgroup I, table III and 3 percent PDA for functional parameters subgroup VII, table III at 25°C	All Lots
11. Final electrical tests 10/ (see table III, for definition of subgroups) a. static test b. dynamic test c. functional test d. switching test	Group A tests at +25°C, maximum rated operating temperature/minimum rated operating temperature (In accordance with device specification) (see J.3.6)	
12. Radiographic (x-ray) 11/	TM 2012, Two views	
13. Column/Ball attach visual inspection	Manufacturer shall submit PIDTP test plan for approval by QA	
14. External visual inspection 12/	TM 2009 13/	
15. Radiation dose rate induced latch-up test 14/	TM 1020	100%

1/ All lots shall be selected for testing in accordance with the requirements of method 5007 of MIL-STD-883.

2/ All microcircuits shall be subjected to constant acceleration. The constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (i.e., to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

3/ Class level S or class V or class Y devices shall be serialized prior to initial electrical parameter measurements.

4/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when a PDA is specified. The PDA shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class Y the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class Y screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA, or 20 percent whichever is greater. This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

5/ Pre burn-in or interim electrical parameters shall be read and recorded only when delta measurements have been specified as part of post burn-in electrical measurements.

6/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request.

7/ Dynamic burn-in only. Test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class level S or class V or class Y burn-in test shall perform in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the validation team, for dealing with lot failures.

8/ When specified in the applicable device specification, 100 percent of the devices shall be tested for those parameters requiring delta calculations.

9/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be of concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted.

10/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of table III, group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification.

11/ The radiographic screening test may be performed in any sequence after serialization.

12/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

13/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

14/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation step after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the specified device specification. The PDA for each inspection lot or class level S or class V or class Y devices sublot, screened, shall be 5 percent or one device, whichever is greater.

TABLE II. Group B tests (Mechanical and environmental test). 1/

Test 1/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
	Class Q (class level B)	Class V (class level S)	**Class Y (class level S)**
Subgroup: 1 a. Physical dimensions 2/ b. Internal water vapor content 2/ 3/		a.TM 2016 2(0) b.TM 1018 3(0) or 5(1) 4/ 5,000 ppm maximum water content at 100°C	a. TM 2016 2(0) b. 5/
Subgroup: 2 a. Resistance to solvents **6**/ b. Internal visual inspection for DPA and mechanical test		a.TM 2015 3(0) b.TM 2013, 2014 2(0) Failure criteria from design and construction requirements of applicable acquisition document	Where applicable a.TM 2015 3(0) b.TM 2013, 2014 2(0)
Subgroup: 3 a. Bond strength 7/ (1) Thermo compression (2) Ultrasonic (3) Flip-chip (4) Beam lead b. Die shear test or substrate attach strength or stud pull test (for passive elements) c. Flip chip pull off test (test perform prior underfill dispense)		a. TM 2011 22(0) (1) condition C or D (2) condition C or D (3) condition F (4) condition H b. TM 2019 or 2027 for the applicable die size 3(0) c. TM 2031 2(0)	Where applicable a.TM 2011 22(0) (3) condition F b. TM 2019 or 2027 for the applicable die size 3(0) c. TM 2031 2(0)
Subgroup: 4 Solderability 8/		TM 2003 22(0) (Based on leads from 3 devices minimum Solder temperature +245°C ±5°C)	Where applicable TM 2003 22(0) (Leads from 3 devices minimum) Solder temperature +245°C ±5°C)
Subgroup: 5 2/ a. Lead integrity b. Seal test (1) Fine (2) Gross c. Lid torque 10/		a. TM 2004 45(0) 9/ Test condition B2, lead fatigue b. TM1014, as applicable c. TM2024, as applicable	Where applicable a. TM 2004 45(0) 9/ Test condition B2, lead fatigue b. 5/ c. TM2024
Subgroup: 6 11/ a. Steady state life test b. End-point electrical parameter 12/		a.TM 1005 45(0) (condition C, D, or E) b. As specified in the applicable device specification	a.TM 1005 45(0) (condition C, D, or E) b. As specified in the applicable device specification

TABLE II. Group B tests (Mechanical and environmental test) -Continued.

Test 1/	**MIL-STD-883 test method and conditions** Minimum sample size quantity (accept no.)		
	Class Q (class level B)	Class V (class level S)	**Class Y (class level S)**
Subgroup: 7 a. Temperature cycling b. Constant acceleration c. Seal (a) Fine (b) Gross d. End-point electrical parameters		a.TM 1010 15(0) (condition C 100 cycles min.) b. TM2001 15(0) (condition E Y orientation only) c.TM1014 d. As specified in the applicable device specification	a.TM 1010 15(0) (Condition C 100 cycles min.) b. TM2001 15(0) (condition E Y orientation only) c. 5/ d. As specified in the applicable device specification
Subgroup: 8 13/ a. Electrostatic discharge (ESD) sensitivity (For initial qualification only)		TM 3015 (see 4.2.3 MIL-PRF-38535)	TM 3015 (see 4.2.3 MIL-PRF-38535)

1/ Electrical reject devices from that same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. . Group B test shall be performed also each qualified package type and lead finish.

2/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot.

3/ This test is required only if it is a glass-frit-sealed package. Unless handling precautions for beryllia packages are available and followed method 1018, procedure 3 shall be used. See subgroup 6 of group D.

4/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e. 3 or 5 devices) fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.

5/ This test is not applicable for class Y device.

6/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.

7/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than three devices be used to provide the number of leads required.

9/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 9/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use method 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need be performed only on packages having leads exiting through a glass seal.

10/ Lid torque test shall apply only to glass-frit-sealed packages.

11/ The alternate removal-of-bias provisions of 3.3.1 of method 1005 shall not apply for test temperature above 125°C.

12/ Read and record group A subgroups 1, 2, and 3.

13/ The requirements for ESD testing are specified in appendix A of MIL-PRF-38535.

TABLE III. Group A (electrical tests). 1/

Subgroup	**Test**	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.) 2/ 3/ 4/ 5/		
		Class Q (class level B)	Class V (class level S)	**Class Y** **(class level S)**
1 2 3	Static tests at +25 □C Static tests at maximum rated operating temperature Static tests at minimum rated operating temperature		116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0) or 100 percent/ 0 sample (see B.4.2.a)
4 5 6	Dynamic tests at +25 □C Dynamic tests at maximum rated operating temperature Dynamic tests at minimum rated operating temperature		116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0) or 100 percent/ 0 sample (see B.4.2.a)
7 8A 8B	Functional tests at +25 □C Functional tests at maximum rated operating temperature Functional tests at minimum rated operating temperature		116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0) or 100 percent/ 0 sample (see B.4.2.a)
9 10 11	Switching tests at +25 □C Switching tests at maximum rated operating temperature Switching tests at minimum rated operating temperature		116(0) or 100 percent/ 0 sample (see B.4.2.a)	116(0) or 100 percent/ 0 sample (see B.4.2.a)

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements. Group A test shall be performed on each inspection lot on actual devices and test can be performed any order.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in footnote 2/ above, and shall be 116/0 sample.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For class level S or class V or class Y: if this testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub) lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

TABLE IV. Group C tests (Die related test). 1/ 2/ 3/ 4/

Subgroup	Test	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	**Class Y** **(class level S)**
1	a. Steady-state life test b. End-point electrical parameters		a. TM 1005 22(0) 2000hrs @125°C (see B.4.2.c) b. As specified in the applicable device procurement specification	a. TM 1005 22(0) 2000hrs @125°C (see B.4.2.c) b. As specified in the applicable device procurement specification

1/ Group C test shall be performed on each SEC/actual device on a periodic basis (at least every 3 months) as a condition for acceptance for delivery.

2/ The quantity (accept no.) for all group C tests shall be 45/0, unless otherwise specified in the acquisition document.

3/ Life test shall be performed on a quantity (accept) criteria of 22(0) for 2000 hours @ 125°C or equivalent per TM 1005 to attain 44,000 device hours. The criteria of 45(0) for 1000 hours is also acceptable. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-month period.

4/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

TABLE V. Group D tests (Package related test).

Subgroup	Test 1/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Sub-group: 1 2/	Physical dimensions		TM 2016 15(0)	TM 2016 15(0)
Subgroup: 2 2/	a. Lead integrity b. Seal 4/ (1) Fine (2) Gross		a.TM 2004 3/ Test condition B2 (lead fatigue) or applicable for the package technology style. b.TM 1014 15(0) Test condition as applicable	Where applicable a.TM 2004 3/ Test condition B2 (lead fatigue) or applicable for the package technology style. b. 5/
Subgroup: 3 6/	a. Thermal shock b. Temperature cycling c. Moisture resistance d. Seal (1) Fine (2) Gross 8/ e. Visual examination f. End-point electrical parameters 9/		a.TM1011 15(0) test condition B , 15 cycles minimum. b TM1010 15(0) test condition C, 100 cycles minimum. c.TM1004 15(0) 7/ d.TM1014 test condition as applicable e. In accordance with visual criteria of TM1010 or TM1011 f. As specified in the applicable device specification	a.TM1011 15(0) (Test condition B , 15 cycles minimum.) b TM1010 15(0) (Test condition C, 100 cycles minimum) c.TM1004 15(0) 7/ d. 5/ e. In accordance with visual criteria of TM1010 or TM1011. f. As specified in the applicable device specification.
Subgroup: 4 6/	a. Mechanical shock b. Vibration, variable frequency c. Constant acceleration d. Seal (1) Fine (2) Gross e. Visual examination f. End-point electrical parameters		a.TM 2002 15(0) condition B min b.TM 2007 15(0) condition A min c.TM 2001 15(0) Test condition E minimum Y1 orientation only d.1014 condition as applicable e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification	a. TM 2002 15(0) condition B min b. TM 2007 15(0) condition A min c. TM 2001 15(0) (Test condition E minimum Y1 orientation only.) d. 5/ e. In accordance with visual criteria of method 2007 f. As specified in the applicable device specification

TABLE V. Group D tests (Package related test). - Continued.

Subgroup	Test 1/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup: 5 2/	a. Salt atmosphere 7/ b. Seal (1) Fine 8/ (2) Gross c. Visual		a.TM 1009 15(0) Test condition A minimum b. TM 1014 condition as applicable c. TM 1009 In accordance with visual criteria of method 1009	Where applicable a.TM 1009 15(0) Test condition A minimum b. 5/ c. TM 1009 In accordance with visual criteria of method 1009
Subgroup: 6 2/	Internal water vapor (cavity packages) 10/		TM 1018 3(0) or 5(1) 5,000 ppm maximum water content at 100°C	5/
Subgroup: 7 2/	Adhesion of lead finish 11/		TM 2025 15(0) 12/ (Leads from 3 devices minimum)	Where applicable TM 2025 15(0) 12/ (Leads from 3 devices minimum)
Subgroup: 8: 2/	Lid torque 13/		TM 2024 5(0) Glass frit seal only	Where applicable TM 2024 5(0) Glass frit seal only
Subgroup: 9:	a. Soldering heat 14/ b. Seal (1) Fine (2) Gross c. External Visual examination d. End-point electrical		a. TM2036 3(0) b. TM1014 condition as applicable c. TM2009 d. As specified in the applicable device specification	Where applicable a. TM2036 3(0) b. 5/ c. TM2009 d. As specified in the applicable device specification

1/ Group D test shall be performed on each SEC/actual device at every 6 months. In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented by the accepted or rejected data.

2/ Electrical reject devices from that same inspection lot may be used for samples.

3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use method 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum.

TABLE V. Group D tests (Package related test) - Continued.

4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/ This test is not applicable for class Y device.

6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical shock".

7/ Lead bend stress initial conditioning is not required for leadless chip carrier packages. For fine pitch packages (25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.

8/ After completion of the required visual examinations and prior to submittal to method 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

9/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

10/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e. 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with 5 additional devices from the same lot. If sample size (accept number) of 5(1) is used to pass the lot, the manufacturer shall evaluate his product to determine the reason for the failure and whether the lot is at risk.

11/ The adhesion of lead finish test shall not apply for leadless chip carrier packages.

12/ Sample size number based on number of leads.

13/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

14/ This test is performed at qualification/re-qualification of design changes, which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from test method 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

Proposed changes in MIL-PRF-38535 (yellow highlighted)

Main body Text :

This specification is approved for use by all Departments and Agencies of the Department of Defense.

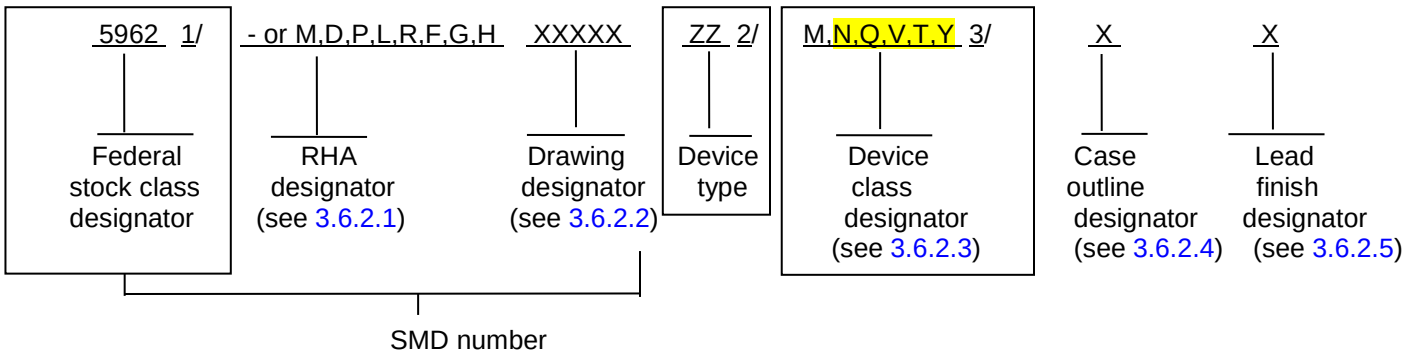
This document is a performance specification. It is intended to provide the device manufacturers an acceptable established baseline in order to support Government microcircuit application and logistic programs. The basic section of this specification has been structured as a performance specification, which is supplemented with detailed appendices. These appendices provide guidance to manufacturers on demonstrated successful approaches to meeting military performance needs. These appendices are included as a benchmark and are intended to impose performance requirements. For QML microcircuits the manufacturer is required to develop a program plan that meets or exceeds the performance detailed in these appendices (see appendices A, G, H, and J). Appendix A is mandatory for manufacturers of device types supplied in compliance with MIL-STD-883 and forms the basis for QML classes Q, V and Y. Appendix B is intended for space application and is required for class level S (class V and class Y) devices. Appendix C is mandatory for devices requiring radiation hardness assurance (RHA). Appendix D is mandatory for statistical sampling, life test, and qualification procedures used with microcircuits.

3.4.2.1 Qualification extension. When a basic plant desires to qualify a device or process flow that includes an offshore site, application for certification and qualification may be extended with QA approval under the following conditions:
a. Control and approval of the design, fab, assembly and test operations by the manufacturer's TRB is required along with periodic self-assessments of the offshore sites. The manufacturer's TRB shall review all screening and TCI tests to determine whether they should be performed exclusively in the offshore site or reserved for the basic plant in order to assure quality and reliability. The manufacturer's TRB assessment shall be made available to the QA for review or approval as appropriate.

b. QA certification of the offshore site is required. For class Q, V and Y products all operations, sites, and plants shall be QA certified however, this certification may be issued through the manufacturer's TRB with QA approval. Validation of these offshore operations is also required. For assembly site(s) an initial site shall be certified and qualified by the QA. Additional assembly sites shall be assessed subsequent to the initial validation.

3.6.2 Part Identification Number (PIN). Each QML microcircuit shall be marked with the complete PIN. The PIN may be marked on more than one line provided the PIN is continuous except where it "breaks" from one line to another. As of revision B of MIL-PRF-38535, several types of documents are acceptable for use when specifying QML microcircuits. They are MIL-M-38510 device specifications and SMD. The PIN marked on those parts under QML shall be the same as when supplied by the manufacturer prior to being listed on the QML-38535. The "Q" or "QML" designator combined with the listing of that PIN on a particular vendors QML listing shall indicate the fact that the manufacturer of the device is QML certified and qualified for the processes used to build that product. The PIN system shall be of one of the following forms, as applicable to the SMD or MIL-M-38510 device specification used for production:

a. SMD PINs shall be as follows:



3.6.8 QML marked product. For QML certified and qualified manufacturers and manufacturers who have been granted transitional certification (see H.3.3), standard product (Joint Army Navy (JAN), class M SMDs, and military temperature range class B data book product), produced on a QML flow may be marked with the "Q" or "QML" certification mark. This allowance applies to contractor prepared drawings covering standard product only if the drawing was released prior to 31 December 1993 or the date the manufacturer becomes QML whichever is the later date, and the part is marked with the standard part number. A list of the manufacturer's military temperature range product to be included under QML shall be submitted to the QA for approval. Contractor prepared drawings written for nonstandard parts may not be marked with a "Q" or "QML". The only exception to this requirement is an altered item drawing required by a device specification or SMD.

Only parts covered by a MIL-M-38510 device specification, an SMD, or generic parts that have been grandfathered (a list of eligible devices shall be submitted to DLA Land and Maritime-VA or DLA Land and Maritime -VQ for review) shall be listed on QML-38535. After 31 December 93, new QML products, which are marked with a "Q" or "QML" certification mark, shall be documented on an SMD (see 3.5). Any device that is not processed in compliance with the provisions of MIL-PRF-38535 shall not be claimed to be compliant. Non-compliant products shall not contain “QML”, “QML Y”, “QML V” or any variant thereof within the vendor part number or within any marking located on the package.

4.3 Technology conformance inspection (TCI). All product shipped shall be capable of passing TCI in accordance with tables II, III, IV, and V; for plastic packages see Table IB herein. With QA approval when TM 5005 of MIL-STD-883 is used as a TCI option, class Q shall be capable of passing the class level B flow and class V shall be capable of passing the class level S flow. Class Y shall be capable of passing the flow tables II, III, IV, and V (or class level S) and as defined in Appendix B. When selecting the TM 5005 TCI option for class V or class Y, the group B end-point electricals shall be the same as the group C end-point electricals, unless otherwise specified in the acquisition document. TCI testing shall be accomplished by the manufacturer on a periodic basis to assure that the manufacturer's quality, reliability, and performance capabilities meet the requirements of the QM plan (see G.3.3). Where appropriate, as an option, in place of the fixed sample size (Acceptance number) the manufacturer may use the sample size series (SSS) plan of Appendix D.

6.4.28 Class N. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic. This product must be assessed by the user to determine if it is appropriate for use in users’ application.

6.4.29 Class Q. Items which are hermetic and have been subjected to and passed all applicable requirements of this specification and applicable appendices including qualification testing, screening testing, and TCI/QCI inspections.

6.4.30 Class V. Items that are hermetic and meet all the class Q requirements, and have been subjected to, and passed all applicable requirements of appendix B herein.

6.4.31 Class Y. The class Y device will be defined as ceramic non-hermetic package, and meet all applicable appendices requirements of this specification including qualification, screening and TCI/QCI requirements, and shall pass all applicable requirements of Appendix B herein.

6.4.32 Class level B. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections and are documented on a MIL-M-38510 specification sheet.

6.4.33 Class level S. Items that meet all the class B requirements, and have been subjected to, and passed, all applicable requirements of appendix B herein and are documented on a MIL-M-38510 specification sheet.

A.3.5 Design and construction. Microcircuit design and construction shall be in accordance with all the requirements specified herein and in the device specification or drawing.

A.3.5.1 Package. All devices supplied under this appendix except for class Y shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. No organic or polymeric materials (lacquers, varnishes, coatings, adhesives, greases, etc.) shall be used inside the microcircuit package unless specifically detailed in the device specification or drawing (e.g., polyimide interlayer dielectric). Alpha Particle protection is permitted if permitted by the device specification or drawing. Desiccants may be used in the microcircuit package (except for class level S devices where they are prohibited) only if each lot is subjected to and passes an internal water vapor test, test method 1018 of MIL-STD-883, with a limit of 1,000 ppm at +100°C for a sample of 3(0) or 5(1). The internal moisture content for class level S devices, after completion of all screening, shall not exceed 5,000 ppm at +100°C. Polymer impregnations (backfill, docking, coating, or other uses of organic or polymeric materials to effect, improve, or repair the seal) of the microcircuit packages shall not be permitted. Polymer coating used to effect or improve marking adhesion shall not be applied over lid seal area.

The class Y device shall be defined as ceramic non-hermetic package, and meet all applicable appendices requirements of this specification, and shall pass all applicable requirements of Appendix B herein.

A.3.5.1.1 Polymeric die attach materials. All polymeric materials of the microcircuits shall meet the requirements TM 5011 of MIL-STD-883. Polymeric die attach materials shall be allowed under the following conditions. Polymeric materials shall be approved by the acquiring or preparing activity.

A.3.5.6.2 Lead or terminal material. Lead or terminal material shall conform to one of the following compositions:

a. Type A: Iron-nickel-cobalt alloy: SAE-AMS-I-23011, class I, ASTM F15.

b. Type B: Iron-nickel alloy (41 percent nickel): SAE-AMS-I-23011, class 5, ASTM F30.

c. Type C: Co-fired metallization such as nominally pure tungsten. The composition and application processing of these materials shall be subject to QA approval and submitted with application to test

d. Type D: Copper-core, iron-nickel ASTM F30 alloy (50.5 percent nickel). The core material shall and the consist of copper (oxygen-free), ASTM B170, grade 2.

e. Type E: Copper-core ASTM F15 alloy. The core material shall consist of copper (oxygen-free) ASTM B170, grade 2.

f. Type F: Copper (oxygen-free) ASTM B170, grade 2. This material shall not be used as an element of any glass-to-metal seal structure.

g. Type G: Iron-nickel alloy (50.5 percent nickel): SAE-AMS-I-23011, class 2, ASTM F30.

h. Type H: Tin-lead alloy solder balls, bumps or columns.

i. Type J: Tin-lead alloy with copper spiral columns.

Appendix B

SPACE APPLICATION

B.1 SCOPE

B.1.1 Scope. This appendix presents the requirements that are to be used to supplement this specification and the other applicable appendices for space level microcircuits. The manufacturer's process may include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved by the qualifying activity after coordination with the government space community (e.g. DTRA, NASA, NRO, and AFSMC). The approach outlined in this appendix is a proven baseline that contains details of the screening and technology conformance inspection (TCI) procedures. Manufacturers are to be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix. This appendix is intended for product to be used in space applications. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2 APPLICABLE DOCUMENTS.

B.2.1 General. The documents listed in this section are specified in sections B.3 or B.4 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections B.3 and B.4 of this appendix, whether or not they are listed.

B.2.2 Government documents.

B.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-M-38510 - Microcircuits, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

B.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

(Copies of this document are available online at http://www.jedec.org/ or from JEDEC Office, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

B.3 REQUIREMENTS

B.3.1 General. Microcircuits supplied to this appendix shall be manufactured and tested in accordance with approved baselines and the requirements herein as applicable. Only class “V” and class “Y” level product marked with an RHA designator is required to meet table B-1 herein. Upon approval from the Technology Review Board (TRB) and the qualifying activity (QA), screening and TCI may be modified for qualified manufacturer listing (QML) class V and class Y level product, provided substantiating data is submitted to demonstrate that the manufacturer has a defined capability on the manufacturing line which is controllable, and in control. These changes cannot affect any thermal, mechanical or electrical parameters, which affect form, fit, function or radiation hardness assurance level (when applicable) of the device, defined within the device specification or standard microcircuit drawing (SMD). The space community (e.g. DTRA, NASA, NRO, and AFSMC) and the customer shall be notified of major changes to the manufacturer's quality management (QM) plan. Any optimization proposed by the manufacturer must be presented to the qualifying activity and coordinated with the space community with accompanying supporting data to validate the proposed change. The optimization must be approved by the QA in writing prior to implementation.

B.3.1.1 Acquiring activity. When specified by the acquisition document (purchase order), the acquiring activity may:

a. Require prior notification of major changes to the baselined processes, procedures, or testing.

b. Require independent verification of wafers (unprobed) or packaged devices (technology characterization vehicle (TCV), standard evaluation circuit (SEC), or actual devices) by original equipment manufacturer’s (OEM's) or Government agencies.

c. Request screening and TCI summary data is delivered with the devices.

B.3.2 Conflicting requirements. In the event of conflict between the requirements of this appendix and other referenced documents, the order of precedence shall be as follows:

a. The acquisition document (order).
b. Applicable device specification.
c. This appendix.
d. MIL-PRF-38535.
e. Specifications, standards, and other documents referenced in 2.1 of MIL-PRF-38535.

NOTE: The acquisition document may specify additional requirements, but shall not reduce or waive any requirements herein.

B.3.3 Validation (certification. Validation of a manufacturing line for production of integrated circuits for use in space systems shall be accomplished by a team headed by DLA Land and Maritime with members from the space community (e.g. NASA, NRO, DTRA, and AFSMC), other interested services, and the customer as necessary.

B.3.4 Manufacturing verification. When specified, the manufacturing verification procedure for new technology shall include characterization of actual devices at -55 □C and 12 specification) with DC, AC and full functional electrical parameters (where applicable). Life testing of new technologies shall be determined by the manufacturer based on characterization with full temperature testing and read and record measurements every 1000 hours. Characterization shall also include a complete evaluation of potential failure mechanisms and mitigations strategies, calculation/evaluation of activation energy and acceleration factors for voltage, temperature, frequency, etc, and establishment of long term reliability failure rates. The life test may be modified based on the determination of failure mechanisms and activation energy (see TM 1016 for guidance with a goal of 15 year operating life at +65 □C 95□C. The manufacturer shall determine worst case for their devices). Additional requirements for characterization are included in appendices G and H (see H.3.1.9 c (v)), and are a requirement for class V and class Y (class level S) devices.

B.3.5 Design verification. When specified, a fully functional VHSIC Hardware Description Language (VHDL) model shall be available.

B.3.6 Part or identifying number (PIN). Each class V level QML microcircuit shall be marked with the device class designator "V" in place of the "Q" designator in the PIN format, see 3.6.2a herein. Devices procured to MIL-M-38510 PINs shall be marked in the format in 3.6.2b herein with the device class designator "S".

B.3.7 Serialization. Prior to the first recorded electrical measurement in screening, each class V microcircuit shall be marked with a unique serial number assigned within the level of the individual microcircuit within that inspection lot.

B.3.8 Traceability. For class V, inspection lot records shall be maintained to provide traceability from the device serial number to the specific wafer lot or to the specific wafer when testing to any group E subgroup (see table B-I), is performed on a wafer by wafer basis.

B.3.9 New technology requirement. For class level S product, this is a product family, material, or process that has never been previously characterized and qualified by the manufacturer for space applications, and is detailed in the manufacturer's new technology insertion program (see 3.4.1.1 and 6.4.42). Existing devices that meet the major change criteria of table A-I are to be evaluated in conjunction with the qualifying activity to determine if the change should be classified as a new technology, as defined in 3.4.1.1 prior to finalized qualification plan implementation.

B.3.10 Use of passive elements: Passive elements should be used only devices that need enhance performance of Die. Chip capacitors used for class Y devices must follow requirement specified in paragraph 3.15 and 3.15.1 for space applications products.

B.3.11 Solder Terminated microcircuits. The solder terminations (e.g. Ball Grid Array – BGA or Column Grid Array-CGA) microcircuits shall meet all applicable appendices and Appendix B herein and must be addressed in the packaging integration demonstration test plan (PIDTP).

B.3.11.1 Assembly Material: For flip chip BGA and CGA packages material contents for solder balls, bumps and solder columns shall be specified on device SMDs and QM plan .

B.3.11.2 Shelf Life Caution: The solder ball/columns oxidize when exposed to atmosphere. It is estimated that sealed dry pack may prevent solder ball/column from oxidizing for about 2 years. Sealed dry packs and/or storage in dry nitrogen environment shall be required for BGA/CGA package devices. Flip chip non-hermetic nature of class Y devices under-fill and/or thermal grease/epoxy would expose to atmosphere moisture, and it is required by the manufacturer to attached moisture sensitivity level (MSL) sticker on the dry packs.

B.3.11.3 Process and materials. For flip chip technology specific materials and process shall be addressed at the start of the flip package design cycle. The following materials and process must be controlled and reviewed by TRB, and shall be documented in the QM plan to produce reliable flip chip package devices which are guided by statistical process control.

a. Substrate materials: Selection of substrate materials is very important since different materials (i.e. ceramic, silicon, organic) have unique behaviors over temperature and effects on solder and underfill materials. Manufacturer shall document all substrate materials in the QP plan.

b. Bump design. The solder bump measurement (bump diameter, bump height and bump pitch) shall be documented in the devices specification and QM plan.

c. Solder deposition process and materials. The solder deposition process (i.e. plated, evaporation, screen print, jetting) and solder deposition materials lead bearing (i.e. eutectic lead (Pb 37) /tin (Sn 63) and high lead (Pb 90) /tin (Sn10)) shall be documented in the devices specification and QM plan.

d. Underfill materials and process. Selection of underfill materials is very important aspect for reliability performance of ICs. Underfill materials bond the two surfaces together to absorb stresses, when different materials thermal coefficient expansion (TCE) are mismatch that lead to drive failure of underfill delamination, solder joint crack, die crack etc. For Hi thermal coefficient expansion (HiTCE) underfill materials must be reviewed by TRB and documented to device specification and QM plan. All underfill material and lid attach epoxy shall meet TM5011 of MIL-STD-883 and must be addressed in the packaging integration demonstration test plan (PIDTP).

B.4 VERIFICATION

B.4.1 Screening for class V. In addition to the screening tests specified in the main body of this specification, the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

a. Nondestructive bond pull (NDBP) in accordance with TM 2023 of MIL-STD-883, or approved alternate verified during validation, on each interconnect bond. An alternate method, if necessary, shall consider a 100 percent visual inspection of the elements to be bonded (i.e., bond pads and posts) prior to the bonding operation, as one part of an overall alternate method.

b. Internal visual inspection in accordance with TM 2010 of MIL-STD-883, condition A, or approved alternate verified during validation on each microcircuit. An alternate method, if necessary, shall address all the inspection topics of
TM 2010 of MIL-STD-883.

c. Particle impact noise detection (PIND) in accordance with TM 2020, condition A of MIL-STD-883 on each device.

d. Reverse bias burn-in in accordance with TM 1015 of MIL-STD-883 on each device as specified in the applicable device specification.

e. Radiograph inspection in accordance with TM 2012 of MIL-STD-883 on each device. Only one view is required for flat packages and leadless chip carriers having lead terminal metal on four sides.

f. Burn-in test in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. Other burn-in conditions may be considered by a class V validation team. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the validation team, for dealing with lot failures. PDA shall be in accordance with TM 5005 of MIL-STD-883 for class S.

g. Wafer lot acceptance testing in accordance with TM 5007 of MIL-STD-883 or an alternative which meets the minimum requirements of TM 5007 on each wafer lot producing class V or S devices (see H.3.2.1.4).

B.4.2 Screening for class Y. In addition to the screening tests specified in the main body of this specification (see table IC) for class Y non-hermetic microcircuits for space applications, the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

a. Confocal scanning acoustic microscopy (CSAM) may be substituted for radiographic inspection on approval by QA.

a.1. CSAM tests on the flip chip underfill of each device shall be performed per method TM2030 of MIL-STD-883.

a.2. When heat sink and/or lid is attached to the class Y device, CSAM as above shall also be used when epoxy or thermal grease are used to attach the heat sink and/or lid directly to the back side of the flip chip die.

For solder terminated microcircuits shall be required screening steps (including electrical test and burn-in) and screening must be performed prior to attachment of solder balls or columns upon approval by the QA. Electrical test shall be performed across the full military temperatures ranges prior to attach of ball/columns on the package to ensure bumps/solder/epoxy integrity. After ball attach (BGA package) electrical test shall be performed across the full military temperatures ranges. After column attach (CGA package) electrical test shall be performed at 25°C as a minimum to verify no electrically/mechanically damage have been introduced due to the attach process, and visual inspection shall perform according to TM 2009 of MIL-STD-883.

B.4.3 **Technology Conformance Inspection (TCI) for class V and Y**. In addition to the TCI tests specified in the main body of this specification (see table II, III, IV, V), unless otherwise noted herein, the TCI requirements listed below apply on each lot of deliverable devices. The group and table references correspond to those contained herein. These requirements do not replace the normal TCI testing requirements of this specification. The following additions or exceptions apply to the TCI tests specified in the main body of this specification.

a. **Table III, group A** electrical test shall be performed on each deliverable lot using actual devices. For those lots having a quantity of less than 116 devices, the tests shall be imposed on a 100 percent basis and the lot accepted on zero test rejects. If a microcircuit fails a group A test parameter as a result of faulty test equipment or operator error, the cause shall be determined and documented, and corrective action shall be implemented and documented.
The affected lot may then be accepted by being resubmitted to the failed test parameters using a 116/0 or 100 percent/0 sample. If a microcircuit fails a group A test due to a previously unscreened parameter, the affected lot may be accepted by screening the lot 100 percent for the failed parameters, and resubmitting a group A sample to the failed subgroup using a 116/0 or 100 percent/0 sample. Any failures resulting from the second screen shall count toward the lot total percent defective. PDA shall be in accordance with footnote 5/ of the Table III group A electrical test or TM 5005 of MIL-STD-883 for class level S.

Group A electrical tests are not required to be performed when the following conditions are met:

(1) The final electrical tests of the 100 percent screening test (see table I) includes all required group A tests (see table III).
(2) The test setup and test conditions are verified by a certified monitor other than the test operator.
(3) Analysis of failures does not indicate a generic or lot related reliability problem.

In no event shall the absence of separate group A testing result in a failure to satisfy the data requirements of section B.3.1.1c.

b. **Table II, group B**, shall be performed on actual devices except as noted herein. Empty device packages or electrical rejects may be used for subgroups B-1 and B-3, and electrical rejects that have been subjected to the 100 percent screening tests may be used for subgroup B-2. The electrical rejects and empty packages shall have been produced under equivalent conditions as the production lot. The TRB shall determine that the intent of the tests is not violated. The sample size of table II is acceptable provided the 22(0) bond strength and solderability criteria has been applied to at least two separate devices (i.e., 11 leads per device), and the die shear test is applied with a 3(0) criteria.

For class Y exceptions and additional requirements are as follows:

1. Subgroup 2. Resistance to solvents is not required for laser marking device.
2. For class Y device package with lid/heat sink attached on the back side of the flip chip die shall require the lid shear or lid torque test. Manufacturers shall submit test procedures for approval by QA for lid shear test. Lid Torque test shall meet TM2024.
3. Subgroup 4. Solderability test is not required for flip chip BGA and CGA packages. Solderability test shall be verified during solder ball and solder column attachment processes. Each BGA ball attachment lot shall be performed ball shear test (ref: JESD22-B117) or ball pull test (Ref: JESD22-B115). Each CGA column attachment lot shall be performed column pull or shear test.
4. For Flip chip BGA/CGA package bump shear test shall be performed in accordance to ASTM 1269 to determine the shear strength of a series of bumps bonds made by either thermal compression or thermosonic techniques)
5. Dye penetration test for inspection of delamination for plastic/organic materials encapsulated packages to withstand moisture ingress and to detect flaws in packaging materials shall perform in accordance with
TM 1034 with sample size 3(0) criteria.
6. Highly accelerated stress testing (HAST) test shall perform in accordance with JESD 020 for 100 hours, +130°C, 85% relative humidity with 15(0) criteria.
7. Autoclave test shall perform in accordance with JESD22- A102-B for laser marked package for the evaluation of moisture resistance of non-hermetic packaged solid state devices.

c. **Table IV, group C** or group B, Subgroup 5 life test requirements shall be met using one of the procedures below.

(1) Life test shall be performed on a quantity (accept) criteria of 22(0) for 2000 hours @ 125°C or equivalent per TM 1005 to attain 44,000 device hours. The criteria of 45(0) for 1000 hours is also acceptable. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-month period.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

(2) Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

d. **Table V, group D** test requirements for package technology style characterization testing (see table H-IIX), and group D testing on the initial production lot utilizing the package family of interest, shall be in accordance with MIL-PRF-38535 and the manufacturer's approved QM plan. A package family consists of a set of package types with the same package configuration (e.g., BGA, CGA), material type (e.g., alumina, beryllium oxide (BeO)), package construction techniques (e.g., single layer, multilayer), ball (bumps) and column spacing with identical package assembly techniques (e.g., material and type of seal, ball attach, underfill, solder bumps or wire bond method and wire size, die attach method and material). All new alternate sources of package elements shall be qualified to the applicable group D tests.

For class Y exceptions and additional requirements are as follows:

a. Manufacturers are responsible for ensuring the package meets all appropriate group D tests as defined in table V of MIL-PRF-38535 or method TM5005 of MIL-STD-883. For class Y, a Packaging Integration Demonstration Test Plan (PIDTP) shall be submitted to QA for approval. This plan must address issues unique to non-hermetic construction and materials, such as potential materials degradation (i.e. out gassing materials shall meet method TM 5011 of MIL-STD-883), moisture absorption, resistance of active devices, passive devices, interconnect substrates selection, solder bump type and underfill materials, environmental effects (e.g. moisture, hydrogen or other contaminants), resistance to processing stresses and unique to solder terminations, such as ball/column integrity, attachment integrity, damage due to test, protection for shipment and shelf life. The PIDTP plan shall be approved by QA after consultation with the space community. Moisture sensitivity level characterization for exposed flip chip underfill and/or thermal grease/epoxy shall use JEDEC J-STD-020D.

e. **Group E inspection** shall be performed in accordance with table B-I. Metal oxide semiconductor (MOS) microcircuits, when specified, shall be tested for time dependent effects post total dose irradiation. When 100 percent latch-up screen is specified, the PDA shall be 5 percent or one device, whichever is greater. The devices used for group E testing shall pass the specified group A electrical tests. An alternate procedure to table B-I may be used upon approval of the qualifying activity.

Appendix B

TABLE B-I. Group E (RHA) TCI test for class V and class Y.

Subgroup	**Test** 1/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	**Class Y (class level S)**
Subgroup: 1 2/ 3/	Neutron irradiation test (Displacement Damage test) a. Qualification b. QCI c Endpoint electrical parameters		a.TM 1017 @25°C 2(0) devices/wafer or 11(0) devices/wafer lot 5/ b. TM 1017 2(0) devices/wafer or 11(0) devices/wafer lot c. As specified in accordance with device specification	a.TM 1017 @25°C 2(0) devices/wafer or 11(0) devices/wafer lot 5/ b. TM 1017 2(0) devices/wafer or 11(0) devices/wafer lot c. As specified in accordance with device specification
Subgroup: 2 3/ 6/ 8	a Total ionization dose(TID) a. Qualification b. QCI c. Endpoint electrical parameters		a.TM 1019 @ 25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot 22(0) devices/ inspection lot 7/ or 1(0)devices/wafer + 4(0) SEC/wafer or 5(0)devices/wafer lot+ 4(0) SEC/wafer 9/ b.TM 1019 @25°C 2(0) devices/wafer or 22(0) devices/wafer lot c. As specified in accordance with device specification	a.TM 1019 @ 25°C at maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/ inspection lot 7/ or 1(0)devices/wafer + 4(0) SEC/wafer or 5(0)devices/wafer lot+ 4(0) EC/wafer 9/ b.TM 1019 @25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/ inspection lot 7/ or 1(0)devices/wafer + 4(0) SEC/wafer or 5(0)devices/wafer lot+ 4(0) EC/wafer 9/ c. As specified in accordance with device specification
Subgroup: 3 10/	a. Dose rate upset test (Transient irradiation test b. End point electrical parameters.		a. For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer 11(0) devices/wafer lot 5/ b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 at 25°C 2(0) devices/wafer 11(0) devices/wafer lot 5/ b. As specified in accordance with device specification

TABLE B-I. Group E (RHA) TCI test for class V and class Y. –continued.

Subgroup	**Test** 1/	**MIL-STD-883 test method and conditions** Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	**Class Y (class level S)**
Subgroup: 4 11/	Radiation dose rate induced latch-up test		TM 1020 As specified in the device specification	TM 1020 As specified in the device specification
Subgroup: 5 12/	Single event effects (SEE) test		ASTM F-1192 or JESD57 4(0) devices As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices As specified in the device specification

1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.

2/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

3/ The radiation hardness assurance capability level (RHACL)/ radiation assurance in the SPEC level is the ratio of the capability level to the specification level of fluence. Subgroups shall be invoked when radiation hardness assurance capability level (RHACL) specification requirements listed in table C-I are not met. For an example if RHACL/SPEC ratio is > 10 then this test may not be required but, if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then this test is required.

4/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 27(1).

5/ In accordance with wafer lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 27(1).

6/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

7/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

8/ Traceability to the specific wafer is required.

9/ In accordance with wafer for device types with greater than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.

10/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when specified in purchase order or contract.

11/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test shall be in accordance with the specified device specification. The PDA for each inspection lot or class level S or class V devices sublot, screened, shall be 5 percent or one device, whichever is greater.

12/ When single event effects (SEE) testing is specified in the purchase order or contract the SEE test shall be performed during initial qualification and after any design or process change that may affect SEE response.

H.3.1.1. Characterization requirements. Testing performed with the intent to understand the technology part, materials, and processes used to determine an item's capability. The manufacturer should evaluate of their process to determine the long term reliability of the product. For class level S (class V and class Y) product, a detailed characterization plan identifying critical parameters, test conditions, durations, required measurements, sample size, and temperatures shall be documented, including a detailed physics-of-failure analysis considering mechanical, thermal, electrical, and chemical properties that could contribute to failures. A failure modes effects analysis approach must be followed to ensure to the maximum extent possible that all significant failure mechanisms have been defined and appropriate mitigation techniques have been identified.

H.3.1.6 New technology requirements. For class level B product, this is a product family, material, or process, that has never been previously characterized and qualified by the manufacturer, and is detailed in the manufacturer's new technology insertion program (see 3.4.1.1.1 and 6.4.42).

For class level S (class V and class Y) product, this is a product family, material, or process, that has never been previously characterized and qualified by the manufacturer for space applications, and is detailed in the manufacturer's new technology insertion program (see 3.4.1.1.1, 6.4.42 and B.3.9).

H.3.1.9 Overview of QML Approval Process. The process for achieving QML approval is outlined below in six basic stages and is further described in detail in the subsequent sections. The stages are listed in the normal sequence to be accomplished; however, several stages may occur concurrently.

v) For class level S (class V and class Y) products, long term life test shall meet the requirements of paragraph B.3.4, appendix B, or shall meet long term life test on a minimum of 1 wafer lot for 4,000 hours minimum at 125°C ambient, or equivalent.

H.3.2.1.1.2 Design checklist for Class level S (class V and class Y) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

H.3.2.1.2.1 Wafer fabrication checklist for class level S (class V and class Y). The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

H.3.4 Qualification.

H.3.4.1 Technology Qualification. The process for qualification is outlined below and is further described in detail in the subsequent sections.

(5) For class level S (class V and class Y). products, long term life test shall meet the requirements of paragraph B.3.4, appendix B, or shall meet long term life test on a minimum of 1 wafer lot for 4,000 hours minimum at 125°C ambient, or equivalent.

For initial technology qualification, a sufficient number of SEC devices is required, from wafers passing the wafer screen requirements and randomly chosen and evenly distributed from one wafer lots for life testing and from 3 wafer lots for total ionizing dose requirements (RHA products only). The testing shall be in accordance with MIL-PRF-38535 Groups A, B, C, D, and E (if applicable) or to the agreed to alternatives and test optimizations defined in the QM plan. The number of SEC device failures shall serve as a qualification benchmark for the technology. Failure analysis (FA) should be done on failed SEC's to determine each failure category and action taken to correct any problems found. The SEC reliability data, including FA results, should be available for review by the QA. For RHA environments, irradiate SEC to demonstrate radiation hardness assurance capabilities limit (RHACL).

H.3.4.4.1 Flip chip package assembly/packaging technology validation. For flip chip technology specific materials and process shall be addressed at the start of the flip package design cycle, and shall submit a packaging integration demonstration test plan (PIDTP) for QA approval. The following materials and process must be controlled and reviewed by TRB, and shall be documented in the QM plan to produce reliable flip chip package devices which are guided by statistical process control.

a. Substrate materials: Selection of substrate materials is very important since different materials (i.e. ceramic, silicon, organic) have unique behaviors over temperature and effects on solder and underfill materials. Manufacturer shall document all substrate materials in the QP plan.

b. Bump design. The solder bump measurement (bump diameter, bump height and bump pitch) shall be documented in the devices specification and QM plan.

c. Solder deposition process and materials. The solder deposition process (i.e. plated, evaporation, screen print, jetting) and solder deposition materials lead bearing (i.e. eutectic lead (Pb 37) /tin (Sn 63) and high lead (Pb 90) /tin (Sn 10)) shall be documented in the devices specification and QM plan.

d. Underfill materials and process. Selection of underfill materials is very important aspect for reliability performance of ICs. Underfill materials bond the two surfaces together to absorb stresses, when different materials thermal coefficient expansion (TCE) are mismatch that lead to drive failure of underfill delamination, solder joint crack, die crack etc. For Hi thermal coefficient expansion (HiTCE) underfill materials must be reviewed by TRB and documented to device specification and QM plan. All underfill material and lid attach epoxy shall meet TM5011 of MIL-STD-883 and must be addressed in the package integration demonstration test plan (PIDTP).

TABLE H-IC. Assembly process technology testing for class Y Non hermetic microcircuits. 1/

Group number	Process	Test	MIL-STD-883 test method and condition or JEDEC test method
1	Die-attach and interconnect	Where applicable a. Thermal shock (100 cycles) b. End-point electricals c. X-ray or ultrasonic d. Visual inspection e. Bond strength f. Die shear or stud pull g. Underfill/epoxy	a. TM 1011, condition C b. In accordance with device specification c. TM 2012 or TM 2030 d. TM 2010 (die-mount and wire bond) plus die cracks e. TM 2011 f. TM 2019 or TM2027 g. TM5011
2	Die-attach, interconnect and seal	Where applicable a.Mechanical shock b. Variable frequency vibration c. Constant acceleration d. Fine and gross leak e. Visual inspection f. End-point electricals	a. TM 2002, condition B b. TM 2007, condition A c. TM 2001 d. 2/ e. TM2009 and magnification criteria 20X of TM2007. f. In accordance with device specification
3	Lid seal	Internal water vapor (5,000 ppm maximum at +100°C)	2/
4	Lid seal	Where applicable Lid torque	TM 2024 (glass seal)
5	Code marking	Where applicable Resistance to solvents	TM 2015
6	Final package testing	High temperature storage	TM 1008 1,000 hours at +150°C
7	Post burn-in lead finish	Where applicable Solderability	TM 2003 (+245°C ± 5°C)

1/ The test methods are listed herein to give the manufacturer an available method to use. Alternate procedures or test methods may be used.
2/ This test is not applicable for non-hermetic class Y device.

TABLE H-IIC. Technology characterization testing for class Y Non hermetic microcircuits

Group number	Process	MIL-STD-883 test method or industry standard
1	Dimensions	Physical dimension TM 2016 1/
2	Resistance to moisture	Where applicable a. Thermal shock TM 1011 condition C b. Temperature cycling (100 cycles) TM1010 condition C. c. Moisture resistance TM1004 / Biased HAST (500 hours, +130°C , 85% RH)In accordance with device specification. JESD22-A110 3/ d. Visual inspection per TM1010 e. End-point electrical - In accordance with device specification
3	Susceptibility to corrosion	Where applicable Salt atmosphere TM 1009
4	Susceptibility to leakage and corrosion	Where applicable Autoclave (no bias) (pressure pot) 2 atm., +121°C - JESD22-A102 (data to be provided for 96 hours and 168 hours)
5	Leads	Where applicable Lead integrity a.TM2004 condition A, B2 or D b. TM2028 for pin grid array
6	Safety	Flammability UL 94, ASTM D2863
7	Fungus resistance	ASTM G21 Required only if fungus is a concern
8	Susceptibility to electrostatic discharge (ESD) sensitivity	ESD TM 3015 or JESD22-A114 4/
9	Susceptibility to latch-up	Radiation induced latch-up test- TM1020
10	Thermal resistance	Thermal characteristics TM 1012
11	Underfill/epoxy materials	TM5011
12	BGA/CGA Ball/column attachment	Per approved PIDTP.

1/ Performed as either characterization or as part of qualification.

2/ The manufacturer shall define a "preconditioning" procedure that simulates board assembly of plastic surface mount devices. This procedure should include moisture intake and reflow simulation. Exposure to soldering fluxes (possible source of corrosiveness) and to board cleaning agents is also recommended for preconditioning the devices.

3/ Five hundred hours of highly accelerated stress testing (HAST) is preferred but the qualifying activity shall consider the manufacturers overall processing and testing to evaluate this requirement. The actual HAST hours or alternate testing shall be included in the QM plan.

4/ ESD classification level is as defined within test method 3015.