DEFENSE LOGISTICS AGENCY
LAND AND MARITIME
P.O. BOX 3990
COLUMBUS, OHIO 43218-3990

May 23, 2016

DLA LAND AND MARITIME-VAC

MEMORANDUM FOR MILITARY AND INDUSTRY COORDINATION

SUBJECT: Engineering Practice (EP) Study for Re-write Radiation Hardness Assurance (RHA) requirements to Appendix C of MIL-PRF-38535. Project Number 5962-2016-006

The initial draft for this subject document, dated 23 May 2016 is attached, and is also available for viewing and downloading from the DLA Land and Maritime-VA Web Site:

http://www.landandmaritime.dla.mil/programs/milspec/ListDocs.aspx?BasicDoc=5962EPStudies

The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, package assembly houses and user communities concerning Re-write Radiation Hardness Assurance (RHA) requirements to Appendix C of MIL-PRF-38535 documents.

Concurrence or comments are required at this Center within 45 days from the date of this letter. Late comments will be held for the next coordination of the document. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with supporting data. Military review activities should forward comments to their custodians of this office, as applicable, in sufficient time to allow for consolidating the department reply. Since Navy-EC is a custodian for this document, all Navy Review activities should forward their comments directly to this center.

The point of contact for this document is Mr. Muhammad Akbar, DLA Land and Maritime-VAC, Post Office Box 3990, Columbus, OH 43218-3990. Mr. Akbar can also be reached at 614-692-8108 or DSN: 850-8108, or by facsimile 614-692-6939, or by e-mail to: Muhammad.akbar@dla.mil.

-/Signed/-
THOMAS M. HESS
Chief
Active Devices Team

cc:
VQ
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ENGINEERING PRACTICE STUDY

TITLE: Re-write Radiation Hardness Assurance (RHA) requirements to Appendix C of MIL-PRF-38535.

May 23, 2016

EP Study Project Number: 5962-2016-006

PRELIMINARY

Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Device Branch (VAC)

Prepared by:

Muhammad Akbar
DLA Land and Maritime -VAC

EP study on

Re-write Radiation Hardness Assurance (RHA) requirements to Appendix C of MIL-PRF-38535

I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, and Space user communities concerning re-write Radiation Hardness Assurance (RHA) requirements to Appendix C of MIL-PRF-38535.

II. BACKGROUND: This appendix C of MIL-PRF-38535 presents the mandatory requirements part of the specification for device manufacturers supplying radiation hardness assurance (RHA) microcircuits. RHA qualified manufacturer listing (QML) manufacturers shall meet all of the requirements of MIL-PRF-38535 and shall take into consideration of all applicable radiation environment and effects that devices basic parametric limit may degrades or fails or damages due to radiation effects. The following factors shall be considered as a minimum requirements for supplying RHA devices:

(i) Radiation hardness assurance capability level (RHACL) process demonstration which required addressing electrical performance based on radiation environment and all applicable tests.

(ii) For characterization of RHA devices of total ionizing dose (TID) level, manufacturers shall perform total ionizing dose (TID) test in accordance with test method 1019 of MIL-STD-883.

(iii) Bipolar or BiCMOS linear or mixed-signal technology devices have susceptibility to enhanced low dose rate sensitivity (ELDRS) effects in space low dose rate environment. For characterization of bipolar or BiCMOS linear or mixed-signal technology device, enhanced low dose rate sensitivity (ELDRS) effects test is required.

(iv) For MOS microcircuits technology, accelerated annealing test shall be performed at initial qualification for measuring time dependent effects (TDE) of devices are requiring TID level greater than 5K Rad (Si).

(v) The Space environment (e.g. Galactic cosmic rays (GCR), Solar enhanced particles, and energetic neutron and protons) has an effects on microcircuits and caused devices displacement damage. For characterization of devices to be used in space environment, manufacturers are required to consider heavy ion single event effects (SEE) test including single event latchup (SEL), single event upset (SEU), single event burnout (SEB), single event transient (SET), single event gate rupture (SEGR).

The goal of this EP study is to re-write updated requirements for radiation Hardness Assurance (RHA) devices to Appendix C of MIL-PRF-38535 based on current radiation/space energetic particles effects to the microcircuits devices. Proposed re-write updated requirements are **Attachment-1** with yellow highlighted.

III. RESULTS: All comments on this study shall be submitted to: Muhammad.Akbar@dla.mil and resulting coordinated changes will provide a basis for preliminary draft of appendix C of MIL-PRF-38535. Comments to this study are to be provided to DLA Land and Maritime within 45 days i.e. no later than July 06, 2016.

IV. CONCLUSIONS: All received comments will be discussed and coordinated, final EP study will be published and may result as changes of appendix C of MIL-PRF-38535.

Attachment-1

RE-WRITE RADIATION HARDNESS ASSURANCE (RHA) REQUIREMENTS FOR MICROCIRCUITS.

C.1 SCOPE

C.1.1 Scope. This appendix presents the requirements which are to be used to supplement MIL-PRF-38535 for device manufacturers supplying radiation hardness assurance (RHA) microcircuits. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

C.2 APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, or C.5 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections C.3, C.4, and C.5 of this appendix, whether or not they are listed.

C.2.2 Government documents.

C.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices.
MIL-HDBK-815 - Dose-Rate Hardness Assurance Guidelines.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

C.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

ASTM F1892 - Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

(Copies of these documents are available online at http://www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

C.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3 REQUIREMENTS

C.3.1 General. Microcircuits supplied to this document shall be manufactured and tested in accordance with approved baseline manufacturing flow and the requirements herein. RHA qualified manufacturer listing (QML) manufacturers shall meet all of the requirements of MIL-PRF-38535 and shall take into consideration all applicable radiation environments and effects that may degrade the devices basic parametric limit or causes failure or damages due to radiation effects. ~~the additional requirements specified herein.~~ The Technology Review Board (TRB) shall not make major changes to the baselined design rules, processes, procedures, or testing without notifying the qualifying activity prior to implementation of the change.

C.3.2 TRB duties. The TRB duties shall be as outlined in G.3.2.2.

C.3.2.1 TRB/RSS. In the case of a Radiation Source of Supply (RSS) (see 6.4.23), the RSS shall establish a TRB and representatives from the device manufacturer, assembly facility, and test facility shall be part of the TRB. The RSS TRB shall be responsible for all aspects of the device manufacturing process. Details of how all aspects of the device manufacturing processes are controlled shall be documented in the RSS quality management (QM) plan. These include conversion of customer requirements, design, wafer fabrication, assembly, test, RHA testing and verification, and characterization for device specification.

C.3.3 RHA QM plan. A RHA QM plan shall be developed to document the major elements of the manufacturer's QML process (G.3.3). This plan establishes the procedures to be followed to ensure that the devices meet the Radiation Hardness Assured Capability Level (RHACL). The RHA QM plan shall be kept current and up-to-date and reflect all major changes to the RHACL. The RHA QM plan shall be included following requirements as a minimum:

(i) Radiation hardness assurance capability level (RHACL) process demonstration which require addressing electrical performance based on radiation environment and all applicable tests.

(ii) Qualification testing to RHA level in accordance to total ionizing dose (TID);

(iii) Wafer fabrication technology details including devices technology characterization and statistical process control (SPC) monitoring program for critical process steps.

(iv) Wafer acceptance plan based on devices post irradiation parametric limit (PIPL) measurement in accordance with RHA group E test table.

C.3.3.1 Qualification testing to RHA levels Qualification to a RHA level shall consist of characterization to the highest offered RHA level of total ionizing dose (TID). The conditions for radiation testing shall consist of exposing the devices in a step-stress manner to the highest dose level offered and as a minimum the two next consecutive lower RHA levels. The levels are identified as follows: 3K Rad(Si), 10K Rad(Si), 30K Rad(Si), 50K Rad(Si), 100 K Rad(Si), 300K Rad(Si), 500K Rad(Si), 1M Rad(Si). The radiation testing plan (QM Plan) and qualification to the appropriate quality and reliability assurance level for device classes B, Q, S, V, Y or T shall be submitted for QA approval. The RHA level designators are defined below:

RHA designation levels:

RHA level designator (see 3.6.2.1)	Total ionizing dose (TID) level in Rad(Si)
/ or -	No RHA
M	3K Rad
D	10K Rad
P	30K Rad
L	50K Rad
R	100K Rad
F	300K Rad [3]
G	500 K Rad
H	1M Rad

C.3.3.1.1 Total Ionizing Dose (TID) test requirements: For characterization of radiation hardness assurance (RHA) devices of total ionizing dose level, manufacturers shall perform total ionizing dose (TID) test in accordance with test method 1019 of MIL-STD-883. Radiation features and test condition shall be included in the device specification “standard microcircuits drawing (SMD)” and M38510 slash sheet. The following test conditions are the minimum requirements for performing total ionizing dose (TID) test.

(a) For pure CMOS technology devices, manufacturers shall perform total ionizing dose (TID) test for irradiation dose rate between 50 to 300 Rads(Si)/s (e.g. high dose rate (HDR) condition A) of test method 1019 of MIL-STD-883.

(b) For bipolar or BiCMOS linear or mixed-signal devices only, manufacturers shall perform total ionizing dose (TID) test for irradiation dose rate $\leq$10m Rad(Si)/s (e.g. low dose rate (LDR) condition D) and dose rate between 50 to 300 Rads(Si)/s (e.g. high dose rate (HDR) condition A) of test method 1019 of MIL-STD-883. Characterization of enhanced low dose rate sensitivity (ELDRS) test is required in accordance with paragraph 3.13.1 of method 1019 of MIL-STD-883.

C.3.3.1.2 Accelerated annealing test requirements: For MOS microcircuits technology, accelerated annealing test shall be performed for measuring time dependent effects (TDE) of devices are requiring TID level greater than 5K Rad (Si). Annealing test shall be performed at initial qualification and after any design or process changes which may affect the TDE/RHA response of the device (see 3.12 of TM 1019).

C.3.3.1.3 Enhanced low dose rate sensitivity (ELDRS) effects test requirements: Bipolar or BiCMOS linear or mixed-signal technology devices have susceptibility to enhanced low dose rate sensitivity (ELDRS) effects in space low dose rate environment. For characterization of bipolar or BiCMOS linear or mixed-signal technology device, enhanced low dose rate sensitivity (ELDRS) effects test is required. Manufacturers shall perform ELDRS characterization test in accordance with paragraph 3.13 of test method 1019 of MIL-STD-883. If ELDRS characterization test has not been performed, the statement must be included in the procurement document (e.g. SMD) to alert the procuring activity to the potential risk that the device may occurs functional failure in space low dose rate environment.

C.3.3.1.3.1 ELDRS characterization test to determine if a part exhibits ELDRS. Select a minimum random sample of 21 devices from a population representative of recent production runs and have undergone burn-in .
Divide the samples into four groups of 5 each and use the remaining part for a control which means 10 samples are HDR (50- 300 rads(Si)/s) at 5 bias and 5 unbias and 10 samples are LDR ($\leq$ 10 mrads(Si)/s) at 5 bias and 5 unbias conditions.

Post irradiation electrical measurements shall be performed (per paragraph 3.10 TM1019) at HDR condition A and Condition D (bias and unbias). Calculate the radiation induced change in each electrical parameter (Δpara) for each sample at each radiation level. Calculate the ratio of the median Δpara at low dose rate to the median Δpara at high dose rate for each irradiation bias and unbias group at each total dose level. If this ratio exceeds 1.5 for any of the most sensitive parameters then the part is considered to be ELDRS susceptible.

C.3.3.1.3.1.2 ELDRS parts to determine the irradiation conditions for production or lot acceptance testing. Upon characterization and determination of the parts that exhibit ELDRS, Manufacturer shall be marking parts with device type series 61, 61, 63 and so forth to the caution of the customer that devices are ELDRS susceptible.

(i) If the part type is known to exhibit ELDRS or has been shown to exhibit ELDRS by the characterization tests in paragraphs 3.13.1.1 then the parts production or radiation lot acceptance testing (RLAT) may be performed using the default low dose rate test at $\leq$ 10 mrads(Si)/s (Condition D) or an accelerated test (Condition E).

(ii) For the accelerated test a detailed characterization shall be performed to establish the test parameters for the test. The accelerated test approach may include one of the following methods:

(1) A room temperature low dose rate irradiation at a dose rate $\leq$ 10 mrads(Si)/s,

(2) An elevated temperature irradiation,

3) Combinations of high dose rate tests and elevated temperature anneals,

4) Switched dose rates, or some other form of accelerated testing (for guidance on characterization of ELDRS parts see ASTM F1892 Appendix X2).

The characterization testing of the ELDRS parts must demonstrate that the irradiation test procedure for production or lot acceptance testing will bound the low dose rate response for all critical electrical parameters at a dose rate of $\leq$ 10 mrads(Si)/s using a combination of overtest and/or parameter delta design margins. Hence the characterization testing shall include irradiation at $\leq$ 10 mrads(Si)/s, to the specification dose, as a baseline for comparison.

C.3.3.2 Single event phenomena (SEP) or single event effects(SEE). When specified in the purchase order or contract, SEP or SEE testing e.g. single event latchup (SEL), single event upset (SEU), single event burnout (SEB), single event transient (SET), single event gate rupture (SEGR) etc. shall be performed on all RHA designator devices (see 1.5 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle or actual devices as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. ASTM standard F1192 or JEDEC standard JESD57 may be used as a guideline when performing SEP testing. When performing SEP test, manufacturers shall consider following conditions as a minimum for performing SEP test:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0º $\leq$ angle $\leq$ 60º). No shadowing of the ion beam due to fixturing or package related effects are allowed.

b. .The fluence shall be $\geq$ 100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip. Range of the ion which shall be sufficiently penetrate well beyond the deepest part of the sensitive volume of the devices to detect latch-up.

e. The test temperature shall be +25ºC ±10ºC for single event upset (SEU) testing and at the maximum rated operating temperature $\pm$10ºC for SEL/SEB/SEGR testing.

f. Bias conditions shall be defined by the manufacturer for latchup (SEL) measurements.

C.3.4 RHA/QML certification requirements. The manufacturer shall meet the requirements in 3.4.1 herein. In addition to standard flow certification the manufacturer's RHA certification testing shall be performed by a laboratory that has received suitability from the qualifying activity (QA).

C.3.4.1 Process capability demonstration. The manufacturer shall meet the requirements in 3.4.1.1 and shall also meet the following for an RHA device. A RHACL shall be established for the environments selected by the TRB and consistently demonstrated for a technology at the specified level of electrical performance. Changes in the RHACL may require reevaluation of these capabilities by the TRB. Listed below are the radiation environments that shall be addressed:

a. Natural or Space environment:

Devices technology	Total ionizing dose (TID) test (TM 1019 of MIL-STD-883)				Displacement damage test 1/		Heavy ion SEE test 2/
	High dose rate(HDR)	Low dose rate(LDR)	HDR and LDR for ELDRS characterization	TDE	Neutron (TM1017)	Proton SEE test (JSED234)	SEL, SEB, SERG, SEU, SET and SEFI (JESD57 or ASTM F1192)
Digital CMOS	Required	Optional	Not required	Required	Not Required	Required	Required
Linear Bipolar	Optional	Required	Required 3/	Required	Optional	Required	Required
BiCMOS or mixed signal devices	Required	Required	Required 3/	Required	Optional	Required	Required

1/ The neutron or proton is caused microcircuits devices displacement damage. The displacement damage test is to be conducted only initial characterization of device. However, production test can be performed when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

2/ The Space environment (e.g. Galactic cosmic rays (GCR), Solar enhanced particles, and energetic neutron and protons) has an effects on microcircuits. Manufacturers are required to consider space environment for characterization of devices to be used in space environment. However, the heavy ion single event effects (SEE) test shall be performed in production test when specified in the purchase order or contract.

~~(1) Total ionizing dose and time dependent effects for ionizing radiation (MIL-HDBK-814, ASTM F1892 and TM 1019 of MIL-STD-883).~~

~~(2) Single-Event-Effects (SEE): Including upset, latch-up, burnout, gate rupture caused by Galactic Cosmic Rays (GCR), Solar Enhanced Particles, and energetic neutron and protons (ASTM F1192 or JESD57).~~

~~(3) Displacement damage: Caused by energetic neutrons and protons.~~

b. Weapon or Nuclear environment:

Devices technology	Total ionizing dose (TID) test (TM 1019 of MIL-STD-883)				Displacement damage test 1/	High dose rate latch up 2/	High dose rate upset 2/	Dose rate survivability 2/
	High dose rate(HDR)	Low dose rate(LDR)	HDR and LDR for ELDRS	TDE	Neutron (TM 1017)	(TM 1017)	(TM 1021)	TM1023
Digital CMOS	Required	Not required	Not required	Required	Not Required	Required	Required	Required
Linear Bipolar	May required	Not required	Not required	Required	Required	Required	Required	Required
BiCMOS or mixed signal devices	Required	Not required	Not required	Required	Required	Required	Required	Required

1/ The neutron is caused microcircuits devices displacement damage. The displacement damage test is to be conducted onlyfor initial characterization of the device. However, production testing shall be performed when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

2/ The weapons or nuclear environment high dose rate irradiation has an effect on microcircuits. However, the high dose rate upset, latch up, and survivability test shall be performed in production testing when specified in the purchase order or contract.

~~(1) Dose rate: Upset, latch-up, burnout (MIL-HDBK-815, TM 1020, TM 1021, and TM 1023 of MIL-STD-883).~~

~~(2) Neutron irradiation (MIL-HDBK-814 and TM 1017 of MIL-STD-883).~~

~~(3) Total ionizing dose (MIL-HDBK-814 and TM 1019 of MIL-STD-883).~~

C.3.4.1.1 Design. The manufacturer shall address the design methodology for the following areas of design:

(NOTE: These are also applicable to third party design centers.)

a. Model verification. Model verification shall provide evidence that models defining device response in radiation environments accurately predict the nominal and worst-case circuit response over operating voltage limits and over the temperature range selected for the technology at the RHACL.

b. Design rule verification. The vendor shall document his design rules for radiation hardening his technology and demonstrate his procedures for verifying rule compliance in the context of Design Rules Check (DRC), Electrical Rules Check (ERC) and reliability checking procedures (see G.3.1.b, G.3.4.1.c, H.3.2.1.1.1 b). These rules cover, as a minimum:

   (1) DRC: Geometric and physical.

   (2) ERC: Shorts and open, connectivity.

   (3) Reliability verification: Electromigration (current density), latch-up, electrostatic discharge (ESD), and fuse/anti-fuse reliability.

   (4) RHA rules: The vendor shall document their design rules for radiation hardening in their technology and the procedures for verifying rule compliance.

c. Performance verification. The vendor shall demonstrate his ability to predict the response of the post-irradiation performance at the RHACL including the effects of the specified limits for temperature and voltage variations and the influence of process variations (see H.3.2.1.1.1.c). Any deviation from these requirements shall receive qualification activity approval.

C.3.4.1.2 Wafer fabrication. As part of certification, the manufacturer shall identify a specific technology or technologies for the wafer fabrication (see H.3.2.1.2).

a. Statistical process control (SPC) and in-process monitoring program for RHA. SPC is especially critical for maintaining a technology's RHACL. This occurs since relatively minor changes in a process flow can drastically effect device radiation performance. The manufacturer shall identify and document all critical process nodes associated with RHA. See H.3.2.1.3 for a general list of critical process steps, any deviation from this list shall receive qualifying activity approval.

b. Technology characterization vehicle (TCV) program. The TCV program is an integral part of a technology's RHA and shall be carefully configured to ensure the accurate characterization of a technologies radiation capability. The TCV program shall be designed to support RHA activities, parametric extraction, model development and validation, SPC and failure mode analysis. (see H.3.2.2.2.1) The TCV structures shall be used to determine a technology's RHACL and in addition determine failure modes and mechanisms by irradiation to 2x RHACL or failure, whichever comes first. Failure can be either functional or parametric.

c. TCV certification. When radiation hardness is a requirement of the technology, special structures shall be incorporated into the TCV program to characterize the technology's capability for producing devices with assured radiation hardness to the RHACL. To determine that the RHACL is appropriate for the technology, the vendor shall irradiate the TCV to 2x the RHACL or until failure to determine failure mode and mechanism(s). Also, the bounds of the radiation response shall be determined by testing the appropriate TCV test structures for worst case bias conditions, annealing conditions, and temperature.

d. Standard evaluation circuit (SEC). The SEC shall utilize all relevant radiation hardness assurance design rules and shall be used to demonstrate the specified level of performance at the RHACL. When radiation hardness assurance is a requirement of the technology, the SEC shall be used to certify and monitor the RHACL of a specific fabrication technology in a specific fabrication facility. The SEC shall be designed so it can be used to assess and monitor the radiation hardness of the fabrication process and design rules (see H.3.4.3). The SEC reliability data, including failure analysis results, shall be available for review by the qualifying activity. For RHA environments, the manufacturer shall irradiate SEC to 2x the requested RHACL or to failure (whichever occurs first) under worst case bias, annealing and temperature conditions as a demonstration of the technology's capability to meet the RHACL. A different SEC may be required whenever the design rules, the materials, the basic processes, or the basic functionality of the technology differ.

e. Process monitor (PM). The process monitor is an integral part of a technology's RHA SPC program for in-line process monitoring. The structures shall be carefully designed and configured to ensure the accurate characterization of a technology's radiation performance and capability. The PM shall support wafer acceptance testing and TCI (see H.3.2.1.3.2). Any deviation from this guidance shall be justified to the qualifying activity.

When RHA is a requirement of the QML line, as a minimum, process monitors for RHA qualified technologies shall include test structures to support the following:

(1) Metal oxide semiconductor (MOS) RHA parameters:

(a) Gate oxide thickness; Structures shall be included to ensure gate oxide thickness since this is a critical parameter affecting radiation performance.

(b) The following parameters shall be measured as a function of total ionizing dose:

(i) Threshold voltage (V_T); The linear V_T for each transistor in a cell.

(ii) Linear transconductance (g_m); The linear g_m for a set of transistors.

(iii) I_{on}/I_{off} (leakage current).

(iv) Propagation delay time (t_{PD}); A test structure in the form of a functional circuit such as an inverter or register chain shall be available to support this measurement.

(v) Field transistor leakage; Field transistor leakage for the minimum design/layout rules.

(2) Bipolar parameters. The bipolar parameters should be those found in H.3.2.1.3.2 c and shall be measured as a function of total ionizing dose and neutron fluence (as appropriate).

(3) Gallium arsenide (GaAs) parameters. The following parameters should be measured as a function of total ionizing dose and neutron/proton fluence (as appropriate).

(a) Sheet resistance.

(b) Isolation; An ohmic transmission line structure should be included to measure contact resistance and transfer length.

(c) FAT FET; A long length gate FET suitable for the measurement of Schottky barrier height, ideality factor, carrier concentration, and channel depth should be available.

(d) GaAs FET parameters; see H.3.2.1.3.2 d.

(4) Radiation hardness assurance. When RHA is a requirement of the technology, the PM shall include test structures to monitor the following phenomena, as applicable:

(a) Dose-rate latch-up.

(b) Dose-rate upset.

(c) Single-event effects (SEE).

(d) Total ionizing dose.

(e) Displacement damage from neutron or proton irradiation.

(5) Other RHA considerations. In addition, test structures to monitor and characterize radiation response mechanisms and for linear circuit applications shall be included (as appropriate). These structures would include but not be limited to:

(a) Matched transistor pairs for offset current and voltage characterization.

(b) Annular and dual or multi-edged transistor sets for sub threshold I-V characterization.

(c) Four contact devices for charge pumping measurements.

C.3.4.1.3 Wafer acceptance plan. The TRB shall develop and demonstrate a wafer acceptance plan based on electrical and radiation measurement of parametric monitors (PMs). PMs shall be used to determine wafer and wafer lot uniformity and latch-up immunity (when specified). Further testing of the actual device to table C-I may be required. As an option to actual device testing, after initial establishment of device specification and device post-irradiation parameter limits (PIPL), the following procedures are presented as examples for the specified radiation environments:

a. Latch-up: The PM should utilize worst case latch-up structures to determine latch-up holding voltage at maximum temperature. The holding voltage shall be greater than the maximum rated voltage.

b. SEE: The PM should utilize SEE structures such as cross-coupling resistors to memory cells to assure critical parameters agree with worst case acceptance criteria.

c. Dose rate: The PM should utilize structures to ensure rail span collapse does not cause upset or burnout or both and that the metallization resistivity, contact resistance, via resistance, epitaxial layer (EPI), substrate resistivity, and minority carrier lifetime specifications are met.

d. Total ionizing dose: The PM should utilize structures such as capacitors and transistors to ensure that critical parameters agree with worst case PIPL values.

C.3.5 On-site validation. In addition to the requirements in 3.4.1.3 the on-site validation shall include RHA test procedures and RHA data reduction.

C.3.5.1 Technology validation. The general requirements for a technology validation are defined in 3.4.1.4. For RHA technology the following items shall be added:

a. Radiation test procedures.

b. RHA data reduction (e.g., interface state and oxide trapped charge separation).

C.3.6 RHA packages. Packages used for RHA microcircuits shall be characterized for effects that may influence the hardness of packaged product. Characterization shall include impedance of the power and ground distribution network, impedance contributions of bond wires and die attach, and the impedance associated with any passive elements included as integral parts of the package. Qualification of the same die in different packages shall require demonstration either by test or similarity analysis.

C.3.7 Demonstration vehicles. The demonstration vehicles shall be as described in H.3.4.1.3. Each demonstration vehicle shall operate and perform in compliance with the device specification and to the RHACL for a radiation hardened process (which shall be submitted to the qualifying activity) and shall be manufactured in packages which have been tested to C.3.6 herein prior to use for qualification. For a technology that has die as its primary product, the demonstration vehicle shall be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

C.3.7.1 Qualification test plan. See H.3.4.2. Note that for RHA, the die traceability shall be to the individual wafer.

C.3.7.2 Qualification test report. For RHA testing, the pre and post irradiation, electrical parameters and the transient and SEE test conditions shall be retained by the manufacturer.

C.4 VERIFICATION

C.4.1 Traceability. Traceability to the wafer lot level (for GaAs to wafer level) shall be provided for all delivered microcircuits. Traceability shall document, as a minimum, the completion of each step required in design (when applicable), fabrication, assembly, test and any applicable qualified rework procedure.

C.4.2 Design requirements. The manufacturer shall show evidence that all QML/RHA product has been through the qualified RHA technology flow. For RHA devices, sample testing of each design to verify PIPL shall be conducted to determine total dose and neutron hardness level, dose rate upset threshold, latch-up immunity (when specified) at maximum temperature and voltage, and linear energy transfer threshold (LET_{TH}) for upset and latch-up as well as the cross section for SEE. If simulation models can be verified by test to address these concerns, they would be acceptable. It is anticipated that several designs of each ASIC family shall be tested.

C.4.3 Radiation response characterization. When specified in the acquisition document, radiation response characterization data shall be provided for QML microcircuits in those environments specified in the device specification. The characterization shall be obtained in increments of irradiation levels to failure or to a radiation level at or beyond the specification level as determined by the TRB. The characterization data shall be accompanied by the mean and standard deviation of the critical parameters. The results obtained from table C-I testing herein shall be added to the characterization data (at fluence level, dose rate, and parameter levels defined in the device procurement specification test conditions) periodically.

C.4.4 End-of-line technology conformance inspection (TCI) testing (option 1). Group E inspection shall include radiation hardness assurance (RHA) tests on each wafer lot. The PIPL, transient and single event phenomenon (SEP) response (as applicable), and test conditions shall be as specified in the device specification. End-of-line TCI testing shall be performed as recommended in table J-I herein. Requirements as detailed in TM 5005 of MIL-STD-883 may be used, with qualifying activity approval, in place of the TCI requirements herein. All group E testing shall be performed on microcircuits to be delivered as RHA QML microcircuits.

Group E inspection is required only for parts intended to be marked as RHA. RHA quality conformance inspection sample tests shall be performed at the level(s) specified and in accordance with table C-I herein. The applicable subgroups of group E shall be performed when specified in the acquisition document. The actual devices used for group E testing shall be assembled in a qualified package and, as a minimum, shall pass table I, group A, subgroups 1, 7, and 9 at +25 □C prior to irradiation. manufacturer elects to eliminate a quality conformance inspection step by substituting an in-process control or statistical process control procedure, the manufacturer is only relieved of the responsibility of performing the TCI operation associated with that step. The manufacturer is still responsible for providing a product which meets all of the performance, quality, and reliability requirements herein and in the device specification. Documentation supporting substitution for TCI shall be retained by the manufacturer and available to the qualifying activity upon request. For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within post-irradiation specified electrical limits) on the total dose radiation response, one of the following shall be done:

a. The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing.

b. The manufacturer shall develop a correction factor (which is acceptable to the parties to the test) taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

C.4.4.1 End-point tests for group E. End-point measurements and other specified post-test measurements shall be made for each sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the detailed specifications. Any additional end-point electrical measurements may be performed at the discretion of the manufacturer.

C.4.5 In-line TCI testing (option 2). In-line control testing shall be performed through the use of the approved SEC or QML microcircuit. The following shall be addressed for RHA devices; group E testing shall be performed on the SEC or product meeting SEC complexity at intervals set by the TRB in the QM plan. Burn-in shall be addressed as per C.4.4 a or C.4.4 b above.

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class Y.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 1 3/ 4/	Neutron irradiation test (Displacement Damage test) a. Qualification test	a.TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot 5/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	b. QCI/TCI test	b. TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot 5/	b. TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/	b. TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	c. Endpoint electrical parameters test	c. As specified in accordance with device specification	c. As specified in accordance with device specification	c. As specified in accordance with device specification

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class Y. –continued.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 2 3/ 7/ 9/ 10/	Total ionization dose (TID) a. Qualification test	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or ~~22(0) devices/wafer lot~~ 5(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or ~~22(0) devices/wafer lot or~~ 5(0) devices/wafer lot 1(0) devices/wafer + 4(0) SEC or test structures/ wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer
	b. QCI/TCI test	b. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/	b.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/wafer	b.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 1(0) devices/wafer + 4(0) SEC or test structures/ wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer
	c. Endpoint electrical parameters test	c. As specified in accordance with device specification	c. As specified in accordance with device specification	c. As specified in accordance with device specification

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class Y. –continued.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)		
		Class Q (class level B)	Class V (class level S)	Class Y (class level S)
Subgroup 3 11/	a. Dose rate upset test (Transient irradiation test b. End point electrical parameters test	a. For Digital TM 1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0)devices/inspection lot 5/ b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/ b. As specified in accordance with device specification	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/ b. As specified in accordance with device specification
Subgroup 4 12/	Radiation dose rate induced latch-up test	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification
Subgroup 5 13/	Single event effects (SEE) test		ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.

2/ For devices with solder terminations, group E subgroups test may be performed without balls and columns.

3/ The radiation hardness assurance capability level (RHACL)/radiation assurance in the SPEC level is the ratio of the capability level to the specification level of devices fluence. Subgroups shall be invoked when the radiation hardness assurance capability level (RHACL) specification requirements of > 10 are not met. For an example, if RHACL/SPEC ratio is > 10 then this test may not be required, but if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then the subgroup test is required.

4/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V and class Y. –continued.

5/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

6/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed, 18(1).

7/ Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

8/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed, 38(1).

9/ Traceability to the specific wafer is required.

10/ In accordance with wafer for device types with greater than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.

11/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when
specified in purchase order or contract.

12/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test in accordance with the specified device specification. The PDA for each inspection lot for class V or class Y (class level S) devices sublot, screened, shall be 5 percent or one device, whichever is greater.

13/ When single event effects (SEE) testing is specified in the purchase order or contract, the SEE test shall be performed during initial qualification and after any design or process change that may affect SEE response. Destructive SEE (SEB and SEGR) testing shall be performed accordance with JEDEC standard JESD57.

C.5 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

C.5.1 Additional reference documents. The documents in this section may be used as guidelines for the development of a hardness assurance program and are not mandatory for this specification.

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.
MIL-HDBK-816 - Guidelines for Developing Radiation Hardness Assurance Device Specifications.
MIL-HDBK-817 - System Development Radiation Hardness Assurance.
MIL-HDBK-1547 - Electronic Parts, Materials, and Processes for Space and Launch Vehicles.
SD-18 - Defense Standardization Guide for Part Requirements and Applications.

(Copies of these documents are available online at http://quicksearch.dla.mil/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

ASTM INTERNATIONAL (ASTM)

ASTM E666 - Standard Practice for Calculating Absorbed Dose from Gamma or X Radiation.
ASTM E668 - Standard Practice for Application of Thermo Luminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.
ASTM F744 - Standard Test Method for Measuring Dose Rate Threshold for Upset of Digital Integrated Circuits.
ASTM F773 - Measuring Dose Rate Response of Linear Integrated Circuits (Metric).

(Copies of these documents are available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

For information purpose only
Some failure analysis figure based on devices technology and dose rate test conditions:

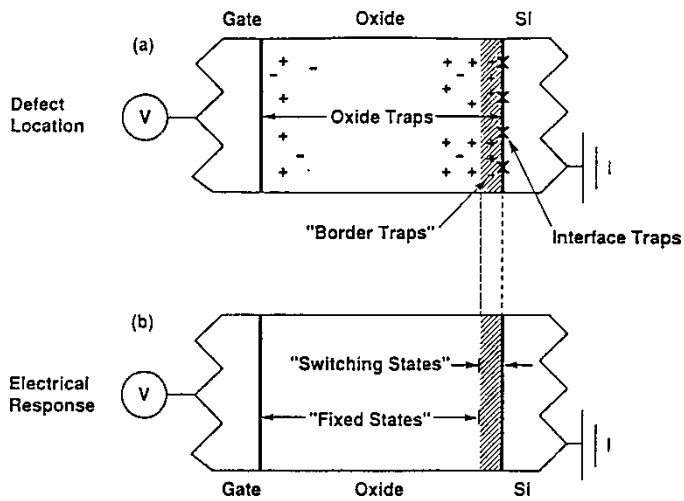

FIG. x Physical Location (*a*) and Electrical Response (b) Associated With Defects in MOS Gate Oxides

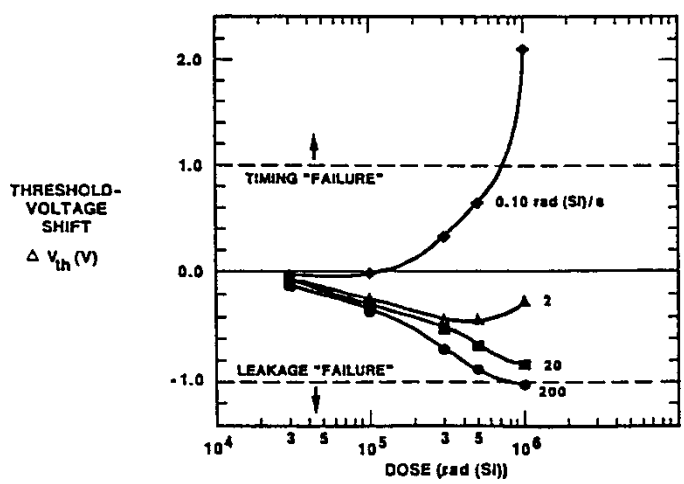

FIG. xxx Threshold Voltage Shifts Versus Dose and Dose Rate for ^{60}Co (2 – 200 rd(SiO_2)/s) and ^{137}Cs (0.1 rd(SiO_2)/s) Irradiations of MOS Transistors With 45-nm Thick Gate Oxides

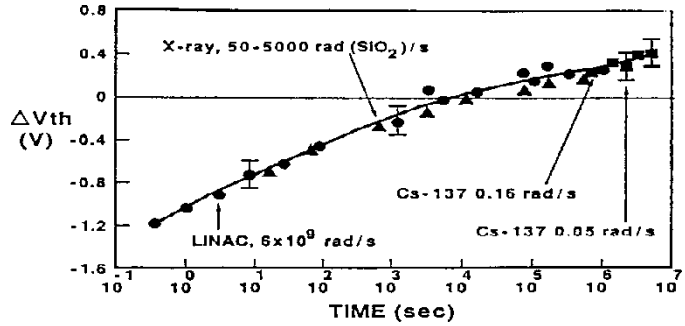

FIG. xx Threshold Voltage Shifts for nMOS Transistors With 60-nm Gate Oxides Versus Post-irradiation

Anneal Time For Varying Dose Rate Exposures to a Dose of 100 krd(SiO_2)

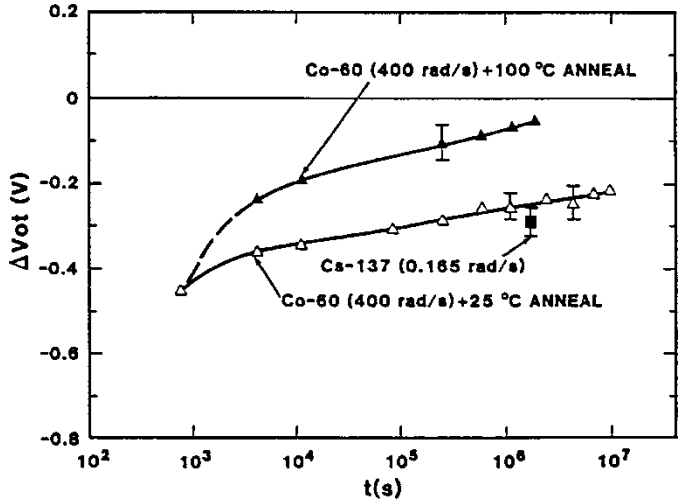

FIG. xxx Threshold Voltage Shift Due to Oxide-Trap Charge for nMOS Transistors With 32-nm Oxides, Irradiated to 300 krd(SiO_2) With ^{60}Co or ^{137}Cs Gamma Rays

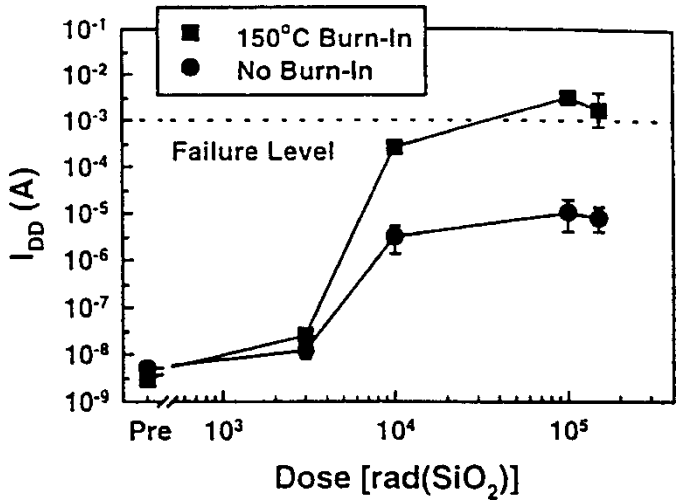

FIG. xx Static Power Supply Leakage Current as a Function of Dose for Commercial Octal Buffer/Line Drivers With or Without a Pre-Irradiation 150°C Burn-In, Irradiated With ^{60}Co Gamma Rays at 90 rd(SiO_2)/s

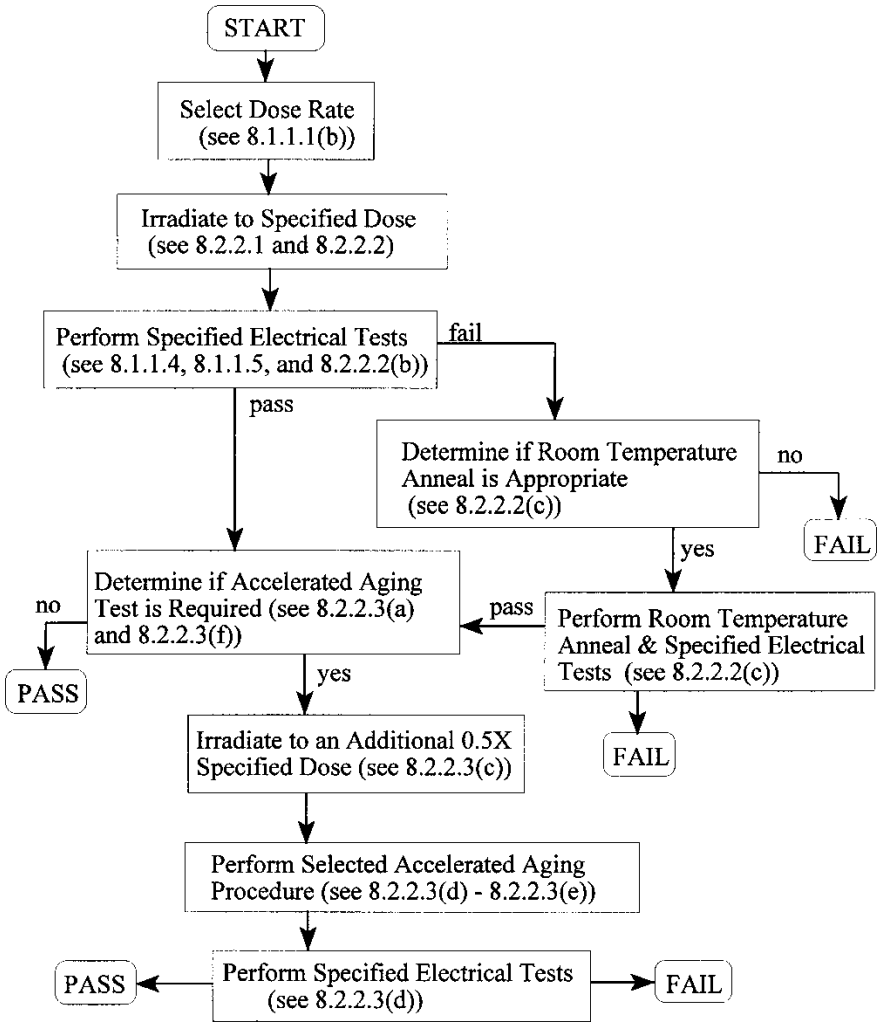

FIG.xxx Flow Chart for Ionizing Radiation Testing of MOS Devices

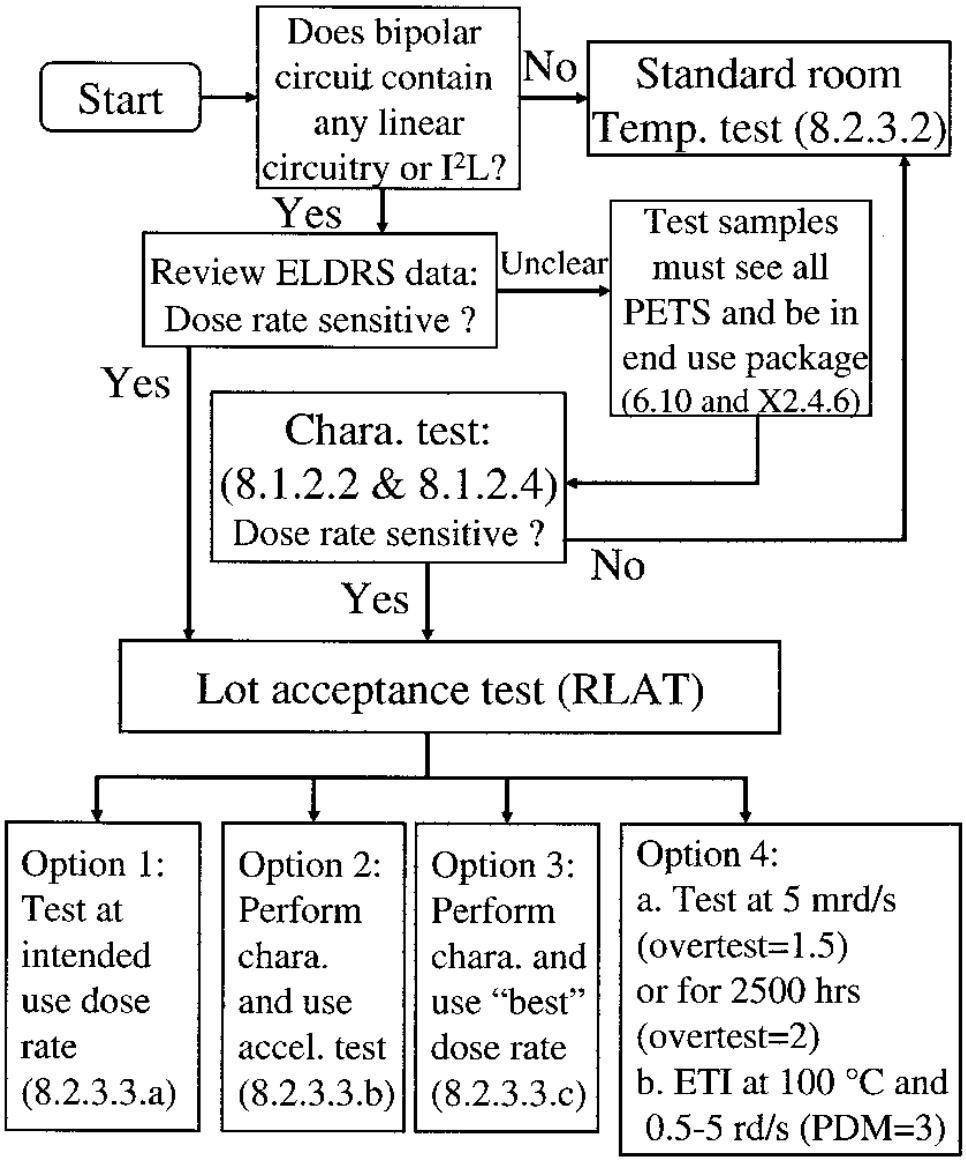

FIG. xx Flow Chart for Lot Acceptance Testing for Bipolar Devices