ENGINEERING PRACTICE STUDY

TITLE: Flip Chip Underfill and Thermal Interface Materials (TIM) Requirements to Propose Test Method TM 5011 of MIL-STD-883 and MIL-PRF-38535.

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Final Report

Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Devices Branch (VAC)

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I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, package assembly houses and user communities concerning to Flip chip underfill test requirements to be added to propose test method TM 5011 of MIL-STD-883 and MIL-PRF-38535 documents.

II. BACKGROUND: Design requirements of modern electronics systems are growing faster and moving forward with an advance in complex package technologies like flip chip. Flip-chip design have been developed with Controlled Collapse Chip Connection (C4) compared with conventional packaging using wire-bonding technology, flip-chip offers many advantages such as high I–O density, short interconnects, self-alignment, better heat dissipation through the back of the die, smaller footprint, lower profile, high throughput, etc. The outstanding merits of flip-chip have made one of the most attractive techniques in modern electronic packaging.

But a major concern of flip-chip technology is the thermal mechanical fatigue life of the C4 solder joints. This thermal mechanical issue mainly arises from the coefficient of thermal expansion (CTE) mismatch between the silicon chip (~ 2.5 ppm/ C) and the substrate (4-10 ppm/ C for ceramics and 18–24 ppm/ C for organic FR4 board). To overcome thermal mechanical fatigue life issue an underfill materials has been invented which lead flip chip devices popular to the modern electronics systems.

The invention of underfill was one of the most innovative developments to enable the use of low-cost organic substrate in flip-chip packages. Underfill is a liquid encapsulate, usually epoxy resins heavily filled with SiO_2, that is applied between the chip and the substrate after flip-chip interconnection. Upon curing, the hardened underfill exhibits high modulus, low CTE matching that of the solder joint, low moisture absorption, and good adhesion towards the chip and the substrate. Thermal stresses on the solder joints are redistributed among the chip, underfill, substrate, and all the solder joints, instead of concentrating on the peripheral joints. It has been demonstrated that the application of underfill can reduce the all-important solder strain level to 0.10–0.25 of the strain in joints. Therefore, underfill can increase the solder joint fatigue life by 10 to 100 times. In addition, it provides an environmental protection to the solder joint. Underfill becomes the practical solution to extending the application of flip-chip technology from ceramics to organic substrates and from high-end to cost sensitive products.

The goal of this EP study is to develop a consensus test requirement for underfill and thermal interface materials(TIM) to the test method 5011 of MIL-STD-883 and MIL-PRF-38535.

III. RESULTS: The EP Study project was opened and initial draft posted on the DLA web and distributed to military services, microcircuit manufacturers, original equipment manufacturers, and user communities on July 13, 2015 for review and comments. All received comments were compiled and discussed at the Columbus JEDEC joint JC-13.2/G-12 meeting in September 2015 and agreed JEDEC, DLA and Space communities to be issued an interim solution for underfill and thermal interface materials (TIM) evaluation and acceptance criteria by the DLA and simultaneously to keep open EP study for further reviewing of underfill and TIM requirements by the JC-13.2 task group. Accordingly, Underfill and TIM requirements interim solution was issued to the JEDEC community including flip chip manufacturers, flip chip assembly houses and space user's communities on September 30, 2015.

After numerous discussions and meetings for underfill and TIM requirements at JEDEC JC-13.2, G-12 and task group and teleconference among flip chip manufacturers, underfill manufacturers, flip chip assembly houses and space user's communities, the following agreement/decision and action were taken by DLA-VAC:

a. Underfill and thermal interface materials (TIM) requirements should be included into MIL-PRF-38535 appendix H to package integrity demonstration test plan (PIDTP) paragraph.

b. DLA discussed updated proposal provided by Aerospace corporation and NASA/JPL for underfill and TIM evaluation and acceptance criteria in New Orleans JEDEC JC-13.2 meeting on June 10, 2016 and decision was reached that underfill and TIM evaluation and acceptance criteria should be simplified and that need to be sent JC-13.2 flip chip underfill task group chair for further review with flip chip manufacturers and space users communities.

c. Accordingly, DLA-VAC prepared a simplified underfill and TIM evaluation and acceptance criteria (see attachment #1) which will be incorporated into MIL-PRF-38535 package integrity demonstration test plan (PIDTP) paragraph.

IV. CONCLUSIONS: DLA-VAC will continue work with JEDEC JC-13.2 flip chip underfill task group and final recommendation for underfill and TIM evaluation and acceptance criteria as outlined in attachment 1 will be incorporated into MIL-PRF-38535 package integrity demonstration test plan (PIDTP) paragraphs.

ATTACHMENT #1

Underfill and Thermal interface materials (TIM) requirements to be added into MIL-PRF-38535

6.4.xx Underfill: Underfill is a liquid encapsulate, usually epoxy resins heavily filled with SiO_2, that is applied between the chip and the substrate after flip-chip interconnection. Upon curing, the hardened underfill exhibits high modulus, low CTE matching that of the solder joint, low moisture absorption, and good adhesion towards the chip and the substrate.

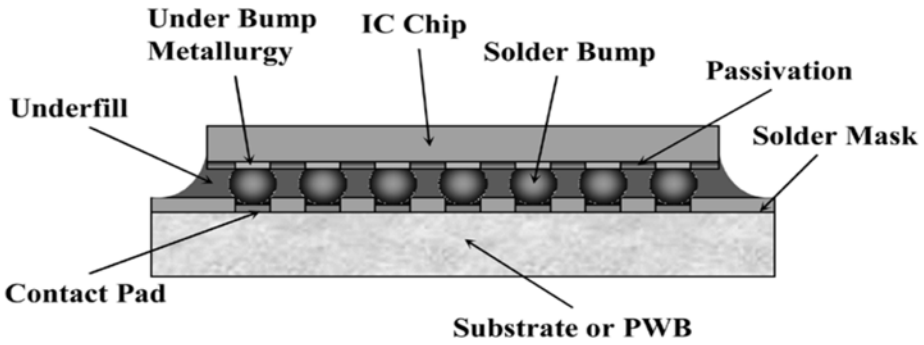

Figure x: Typical flip chip layout with underfill

6.4.xx Thermal interface materials(TIM): Thermal interface materials is the similar materials of adhesive. TIM also used in flip chip devices as a lid attached martials but main reasons to heat spray over the lid. The TIM materials shall have high viscosity, non-corrosive, very high thermal conductivity and good adhesion.

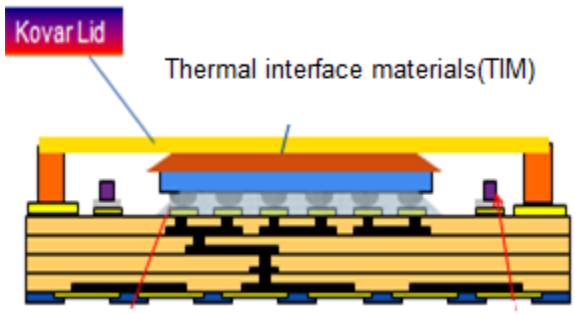

Figure x: Typical flip chip layout with TIM

Propose changes to MIL-PRF-38535:

H.3.4.4.1.2 **Flip-chip assembly.** For space microcircuits employing flip-chip assembly technologies either class V or class Y (class level S), the PIDTP must address the materials and processes unique to solder bump interconnect attach, underfill and lid-to-die attach. The plan shall demonstrate as a minimum, how the following are evaluated and monitored including a corresponding package level reliability demonstration:

1) **Substrate materials**. The substrate materials shall be documented in the PIDTP, and shall include landing pad composition.

2) **Bump geometry.** The solder bump geometry shall be documented in the PIDTP, and shall include bump height, bump diameter and bump pitch, as well as a description of the under bump metallurgy (UBM) shape, size and thickness.

3) **Solder bump deposition process and materials.** The solder bump deposition process shall be documented in the PIDTP (e.g., plated, evaporation, solder paste), along with the solder alloy. In addition, the UBM deposition process (e.g., plated, evaporation, sputtered) and composition shall be documented in the PIDTP.

4) **Flux materials**. The flux type (e.g., no-clean, water soluble) and materials employed for solder bump interconnect reflow shall be documented in the PIDTP.

5) **Underfill materials**. Underfill materials shall be documented in the package integrity demonstration test pan (PIDTP). The PIDTP shall address the relevant properties of the underfill and how they are characterized. The properties below shall be included:

   i) **Coefficient of thermal expansion (CTE**)

   ii) **Glass transition temperature (Tg)**

   iii) **Viscosity**

   iv) **Pot life**

   v) **The shelf life**

   vi) **Underfill particle size/Filler contents**

   vii) **Underfill cure time and temperatures**

   viii) **Bond strength**

   ix) Ionic impurities

   x) **Underfill Outgassing test**: Outgassing shall be tested in accordance with ASTM E595. Underfill outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.

   xi) **Temperature cycling test**: Cured underfill with solder bump shall be performed temperature cycling test for 1,000 cycles in accordance with TM1010 condition C (-65 to 150°C) and subsequently C-SAM test shall be performed to verify underfill void and delamination. The sample size 10(0) shall be considered as minimum.

6) **Thermal interface materials (TIM).** Devices with lid or heat spreader attached to the back side of a microcircuit die, the lid attach/adhesive thermal interface materials shall be documented in the PIDTP. All lid attach/adhesive thermal interface materials shall meet the requirements of TM 5011, MIL-STD-883, and outgassing requirements shall meet the test method ASTM E595. The following test parametric results may be considered with C of C or initial certification test performed by TIM suppliers/users; and approved by QA:

a) Viscosity.

b) Density

c) Volume resistivity

d) Lap shear adhesion

e) Expiration Date

f) Pot life

g) Glass transition temperature (Tg)

h) Outgassing test

i) Dissipation factor

j) Ionic impurities

k) Coefficient of thermal expansion (CTE)

l) Thermal conductivity