DEFENSE LOGISTICS AGENCY
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September 07, 2016

DLA LAND AND MARITIME-VAC

MEMORANDUM FOR MILITARY AND INDUSTRY COORDINATION

SUBJECT: Engineering Practice (EP) Study on proposed changes for electrostatic discharge (ESD) requirements to MIL-PRF-38535. Project Number 5962-2016-008

The initial draft for this subject document, dated 07 September, 2016 is attached, and is also available for viewing and downloading from the DLA Land and Maritime-VA Web Site:

https://landandmaritimeapps.dla.mil/programs/milspec/ListDocs.aspx?BasicDoc=5962EPStudies

The purpose of this Engineering Practice (EP) Study is to obtain input from the military services, microcircuit manufacturers, and user community concerning updating the electrostatic discharge (ESD) requirements in MIL-PRF-38535. Microcircuits are damaged by ESD due to deficiencies in proper ESD protection, controls, handling, and training programs. Additionally, the ESD test methods being used need to be updated for high count pin devices and advanced packaging for new technology devices, which will lead to changes in MIL-PRF-38535 requirements.

Concurrence or comments are required at this Center within 45 days from the date of this letter. Late comments will be held for the next coordination of the document. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with provided supporting data. Military review activities should forward comments to their custodians, as applicable, in sufficient time to allow for consolidating the department reply. Since Navy-EC is a custodian for this document, all Navy Review activities should forward their comments directly to this center to the point of contact.

The point of contact for this document is Mr. Muhammad Akbar, DLA Land and Maritime-VAC, Post Office Box 3990, Columbus, OH 43218-3990. Mr. Akbar can also be reached at 614-692-8108 or DSN: 850-8108, or by facsimile 614-692-6939, or by e-mail to: Muhammad.akbar@dla.mil.

-/Signed/-
Charles F. Saffle
Chief
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cc:
VQ
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ENGINEERING PRACTICE STUDY

TITLE: Propose changes for Electrostatic Discharge (ESD) requirements to MIL-PRF-38535

September 7, 2016

STUDY PROJECT 5962-2016-008

PRELIMINARY

Study Conducted by DLA Land and Maritime

Prepared by:

Muhammad Akbar
DLA Land and Maritime -VAC

I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study is to obtain input from the military services, microcircuit manufacturers, and user community's concerning update ESD requirements to MIL-PRF-38535 documents. Microcircuits damaged by electrostatic discharge (ESD) due to deficiency of proper ESD protection, controlling, handling and training program in place during manufacturing process, also ESD test method need to update for high count pin devices or advanced packages for new technology devices which will lead to change MIL-PRF-38535 documents.

II. BACKGROUND: Advanced microcircuits packaging system deemed small footprint and higher pin count which lead issues of appropriate design of ESD protection circuits, testing method for ESD classification and handling microcircuits are very important. Microcircuits damage from ESD can cost of time, money and mission risk. Currently MIL-PRF-38535 stated ESD classification shall be identified to the devices based on human body model (HBM) and referring test method 3015 of MIL-STD-883 and/or JESD22-A114.

Microcircuit part production, handling, and shipping has changed rapidly wherein Automatic Handling Equipment (AHE) is being added for safely processing the devices. Proper grounding and material requirements of ESD controls in AHEs are very important for prevention of charged device model (CDM) and machine model (MM) type damage to ESD sensitive devices.

MIL-PRF-38535 paragraph A.4.4.2.8, Electrostatic Discharge Sensitivity, states that, "ESD classification shall be done in accordance with TM 3015 of MIL-STD-883 (the testing procedure defined within JESD22-A114 may be used as an alternate with acceptable correlation data)". However, the two documents have differences in their test methods.

- TM3015 states that each device shall be tested using three positive and three negative pulses using each of the pin combinations as shown in the table II in the document. A minimum of 1 second delay shall separate the pulses.
- Whereas, JESD22-A114 states that each sample shall be stressed using one positive and one negative pulse with a minimum of 300 milliseconds between pulses per pin for all pin combinations specified in table 2 of the document.

Recently, manufactures are raised an issue for using TM3015 for high count pin devices wherein products can cause severe problems because of testing times increase dramatically which caused repeatedly stressing the same path and the increasing influence of tester parasitic losses and parasitic charge can lead to false-positive failures.

Considering above issues DLA Land and Maritime –VAC has launched an EP study is to develop an appropriate ESD requirements to MIL-PRF-38535 and update test method 3015 of MIL-STD-883. Propose ESD requirements/survey questionnaire (see attachment # 1) is attached for comments.

III. RESULTS: All comments on this study shall be submitted to: Muhammad.Akbar@dla.mil and resulting coordinated changes will provide a basis for next revision of MIL-PRF-38535. Comments to this study are to be provided to DLA Land and Maritime within 45 days from the date of this letter.

IV. CONCLUSIONS: The final comments on this study will be published as changes in next revision of MIL-PRF-38535 after all submitted comments have been resolved.

Attachment # 1

Questionnaire for propose change of
Electrostatic Discharge (ESD) requirements to MIL-PRF-38535

Electrostatic Discharge (ESD): The transfer of electrostatic charge between bodies or surfaces that are at different electrostatics potentials. The ESD has an impact in electronics industry especially in microcircuits damaged from ESD can cost of time, money and mission risk. In electronics industry three most common ESD Models (1) Human body model(HBM), (2) Charge device model (CDM) and (3) Machine model (MM) are used for classification of ESD and protection of failure analysis.

Human Body Model (HBM): A source of ESD damage is the charged human body, as modeled by HBM standards. The human body model is the oldest and well known ESD model using for characterization of ESD classification in semiconductor industries since 1960s. MIL-PRF 38535 has referred HBM model for classification of ESD classes in paragraph A.3.4.1.4 for initial qualification or marking ESD class level in microcircuits devices in accordance with test method 3015 of MIL-STD-883. Currently MII-PRF-38535 microcircuit devices ESD classification stated below:

HBM ESD class designator	Electrostatic voltage
0	< 250 V
1A	250 V-499 V
1B	500 V-999 V
1C	1000 V-1999 V

Charged Device Model (CDM): A source of damage for the CDM is the rapid discharge of energy from a charged device. CDM is increasingly important reliability issue in the semiconductor industry due to automation in IC's process flow. CDM is now the dominant form of component level ESD failures and assume the IC package is charged either directly via triboelectric effects or indirectly due to external electrical field. The IC industry has been using ESD test standard/method S5.3 for CDM classification and classification are below (see MIL-STD1686 table I):

CDM ESD class designator	Electrostatic voltage
Class C1	0-124 V
Class C2	125-249V
Class C3	250-499 V
Class C4	500-999 V
Class C5	1000-1499 V
Class C6	1500-2,999 V
Class C7	≥ 3,000 V

Machine model (MM): A source of damage for the MM is a rapid transfer of energy from a charged conductor/machine to the conductive leads of the device. MM represents a rapid discharge from items such as charged board assembly, charged cables or the conduction arm of an automatic tester. The IC industry has been using ESD test standard/method S5.2 for MM classification and classification are below (see MIL-STD1686 table I):

MM ESD class designator	Electrostatic voltage
Class M1	0-100 V
Class M2	101-200 V
Class M3	201-400 V
Class M4	401-800 V
Class M5	> 800 V

Considering above three HBM/CDM/MM model, the following questionnaire responses or feedback is required for update MIL-PRF-38535 ESD requirements:

1) What is your comment to update ESD requirements to MIL-PRF-38535 paragraphs?

2) What ESD models are using in your IC manufacturing process including design, wafer fabrication process, assembly, testing and packaging process to classify ESD sensitivity? Please explain details.

3) Currently, MIL-PRF-38535 is required for classification of ESD based on HBM (see MIL-PRF-38535 paragraph A.3.4.1.4). What is your comment regarding incorporate other ESD model Charge device model (CDM) and Machine model (MM) requirement for ESD classification to MIL-PRF-38535?

4) Currently ESD marking and classification on microcircuits devise are based on HBM model, If CDM and MM are incorporated how these 2 models will be implemented? it should be just information purposes in the devices specification?

5) Should the MIL standards be expanded to include charge device model (CDM) and Machine model (MM) testing method?

Recently, manufactures are raised an issue for using TM3015 for high count pin devices wherein products can cause severe problems because of testing times increase dramatically which caused repeatedly stressing the same path and the increasing influence of tester parasitic losses and parasitic charge can lead to false-positive failures. MIL-PRF-38535 paragraph A.4.4.2.8, Electrostatic Discharge Sensitivity, states that, "ESD classification shall be done in accordance with TM 3015 of MIL-STD-883 (the testing procedure defined within JESD22-A114 may be used as an alternate with acceptable correlation data)". However, the two documents have differences in their test methods.

- TM3015 states that each device shall be tested using **three positive and three negative pulses** minimum of 1 second delay shall separate the pulses.

- Whereas, JESD22-A114 states that each sample shall be stressed using **one positive and one negative** pulse with a minimum of 300 milliseconds.

6) What is your comment to use TM3015 and/or JESD22-A114 for microcircuits devices with high count pin for ESD sensitivity characterization/classification?

7) Should DLA need to update MIL-PRF-38535 paragraph A.4.4.2.8 for use JESD22-A114 as an alternate with **acceptable correlation data** requirements?

8) Do we want a standard or test method for reducing the number of pin combinations required for testing?

9) Would statistical pin testing be a good approach?

10) How do the new 2.5D and 3D configurations affect ESD testing?

ESD protection, control, handling and training programs are very important key points to mitigate ESD damage at the design, wafer fab, AHEs, packaging and handing level. Recent audits and NASA/JPL EEE parts bulletin (January–July, 2016 • Volume 8, Issue 1) revealed that microcircuits product manufacturers need to establish well management ESD control program at the component level. i.e. die design, wafer fabrication, wafer bumping, package design, assembly, column attached process, testing and screening, radiation testing, transport by franchise distributor, board level test and verification, and final box level assembly. MIL-PRF-38535 paragraph 3.12 ESD control: require "QML microcircuits shall be handled in accordance with JESD625 or other industry standard practices, to safeguard against discharge damage."

11) JESD625 is a requirements documents for handling ESD sensitivity devices and has an extensive ESD protection and control requirements other than ANSI ESD20.20. Should MIL-PRF-38535 be updated as required documents JESD625 for ESD handling and control program?

12) JESD625 section 11 stated "Recommended ESD audit checklist" which is comprising 33 check points. What is your comment to implement these 33 pints' checklist ESD program for each component level of ICs manufacturing steps?

ESD failures analysis exposed below images during scanning electron microscopy (SEM) inspections

Figure 1. an example of subtle damage that may be caused by ESD. An investigation into excessive current draw on an electronic component successfully isolated a short location using a relatively new infrared imaging technique called pulse sample thermography (PST). Deprocessing and subsequent layer-by-layer scanning electron microscopy (SEM) inspections identified a likely ESD silicon melt site at the active layer on a unique horizontal structure. Follow-up review with the manufacture noted this device to be very sensitive to ESD. The issue was attributed to mishandling, and a follow-up activity was initiated to review the ESD control rigor. (Figure courtesy of JPL Analysis and Test Laboratory.)

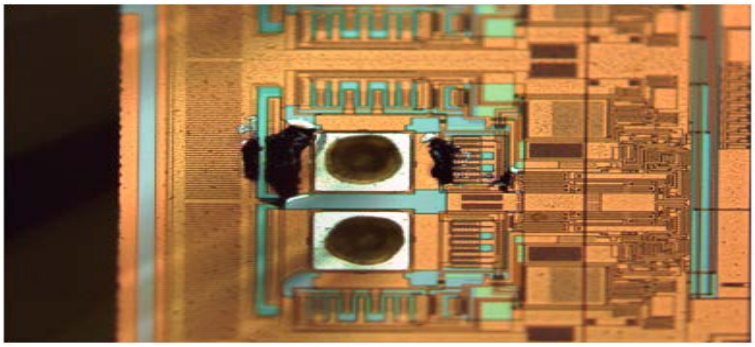

Figure 2: ESD failure devices found in supply chain

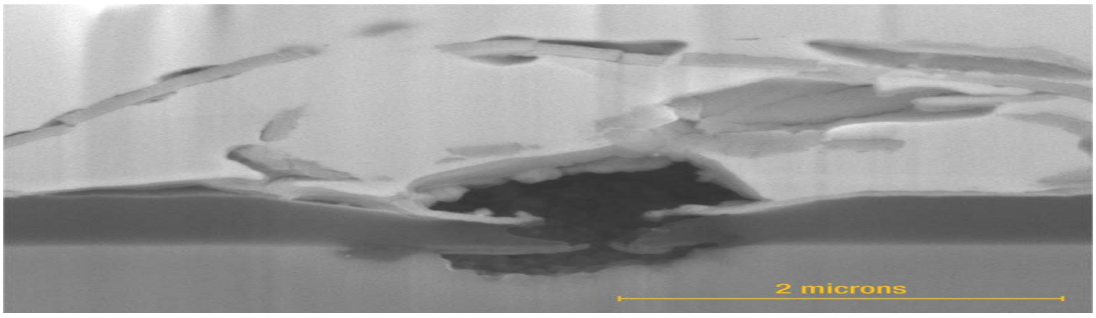

Figure 3: This scanning electron microscope (SEM) cross-section image shows the damage done by a worker forgetting to wear a grounding wrist strap while performing a reverse-bias test on a tunnel diode. The part was observed to drop out of specification, and JPL helped with the failure analysis. Apparently, –600 V of electrostatic discharge (ESD) burned a hole into the part. Furthermore, the surface of the roughened area surrounding the hole experienced an unknown degree of melting and reforming of the alloy. (Figure courtesy NASA/JPL EEE parts bulletin January/May 2014 • Volume 6 • Issue 1)