DEFENSE LOGISTICS AGENCY
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July 13, 2015

DLA LAND AND MARITIME-VAC

MEMORANDUM FOR MILITARY AND INDUSTRY COORDINATION

SUBJECT: Engineering Practice (EP) Study for Flip Chip Underfill Test Requirements to TM 5011 and MIL-PRF-38535. Project Number 5962-2015-004

The initial draft for this subject document, dated **13 July 2015** is attached, and is also available for viewing and downloading from the DLA Land and Maritime-VA Web Site:

http://www.landandmaritime.dla.mil/programs/milspec/ListDocs.aspx?BasicDoc=5962EPStudies

The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, package assembly houses and user communities concerning to Flip chip underfill test requirements to be added to test method TM 5011 of MIL-STD-883 and MIL-PRF-38535 documents.

Concurrence or comments are required at this Center within 30 days from the date of this letter. Late comments will be held for the next coordination of the document. Comments from military departments must be identified as either "Essential" or "Suggested". Essential comments must be justified with supporting data. Military review activities should forward comments to their custodians of this office, as applicable, in sufficient time to allow for consolidating the department reply. Since Navy-EC is a custodian for this document, all Navy Review activities should forward their comments directly to this center.

The point of contact for this document is Mr. Muhammad Akbar, DLA Land and Maritime-VAC, Post Office Box 3990, Columbus, OH 43218-3990. Mr. Akbar can also be reached at 614-692-8108 or DSN: 850-8108, or by facsimile 614-692-6939, or by e-mail to: Muhammad.akbar@dla.mil.

-/Signed/-
THOMAS M. HESS
Chief
Active Devices Team

cc:
VSS
VQ
FMTA

ENGINEERING PRACTICE STUDY

TITLE: Flip chip underfill test requirements to propose test method TM 5011 of MIL-STD-883 and MIL-PRF-38535.

July 13, 2015

EP Study Project Number: 5962-2015-004

PRELIMINARY

Study Conducted by DLA Land and Maritime
Document Standardization Division (VA)
Active Device Branch (VAC)

Prepared by:

Muhammad Akbar
DLA Land and Maritime -VAC

EP study on
Flip chip underfill test requirements to propose test method TM 5011 and MIL-PRF-38535

I. OBJECTIVE: The purpose of this Engineering Practice (EP) Study is to obtain input/feedback from the military services, microcircuit manufacturers, package assembly houses and user communities concerning to Flip chip underfill test requirements to be added to test method TM 5011 of MIL-STD-883 and MIL-PRF-38535 documents.

II. BACKGROUND: Design requirements of modern electronics systems are growing faster and moving forward with an advance in complex package technologies like flip chip. Flip-chip design have been developed with Controlled Collapse Chip Connection (C4) compared with conventional packaging using wire-bonding technology, flip-chip offers many advantages such as high I–O density, short interconnects, self-alignment, better heat dissipation through the back of the die, smaller footprint, lower profile, high throughput, etc. The outstanding merits of flip-chip have made it one of the most attractive techniques in modern electronic packaging.

But a major concern of flip-chip technology is the thermal mechanical fatigue life of the C4 solder joints. This thermal mechanical issue mainly arises from the coefficient of thermal expansion (CTE) mismatch between the silicon chip (~ 2.5 ppm/ C) and the substrate (4-10 ppm/ C for ceramics and 18–24 ppm/ C for organic FR4 board). To overcome thermal mechanical fatigue life issue an underfill materials has been invented which lead flip chip devices popular to the modern electronics systems.

The invention of underfill was one of the most innovative developments to enable the use of low-cost organic substrate in flip-chip packages. Underfill is a liquid encapsulate, usually epoxy resins heavily filled with SiO, that is applied between the chip and the substrate after flip-chip interconnection. Upon curing, the hardened underfill exhibits high modulus, low CTE matching that of the solder joint, low moisture absorption, and good adhesion towards the chip and the substrate. Thermal stresses on the solder joints are redistributed among the chip, underfill, substrate, and all the solder joints, instead of concentrating on the peripheral joints. It has been demonstrated that the application of underfill can reduce the all-important solder strain level to 0.10–0.25 of the strain in joints. Therefore, underfill can increase the solder joint fatigue life by 10 to 100 times. In addition, it provides an environmental protection to the solder joint. Underfill becomes the practical solution to extending the application of flip-chip technology from ceramics to organic substrates and from high-end to cost sensitive products. It is the main reason why flip-chip is so popular today.

The goal of this EP study is to develop a consensus test requirements for underfill to the test method 5011 of MIL-STD-883 and MIL-PRF-38535. Proposed underfill test requirements survey questionnaire Attachment-1 is a unique steps how to evaluate underfill and use in flip chip devices.

III. RESULTS: All comments on this study shall be submitted to: Muhammad.Akbar@dla.mil and resulting coordinated changes will provide a basis for preliminary draft of test method 5011 of MIL-STD-883 and MIL-PRF-38535. Comments to this study are to be provided to DLA Land and Maritime within 30 days i.e. no later than August 13, 2015.

IV. CONCLUSIONS: All received comments will be discussed and coordinated, final EP study will be published and may result as changes test method 5011 of MIL-STD-883 and MIL-PRF-38535.

ATTACHMENT # 1 (Survey questionnaire)

EP study on Flip chip underfill test requirements to be added to propose test method TM 5011 and MIL-PRF-38535

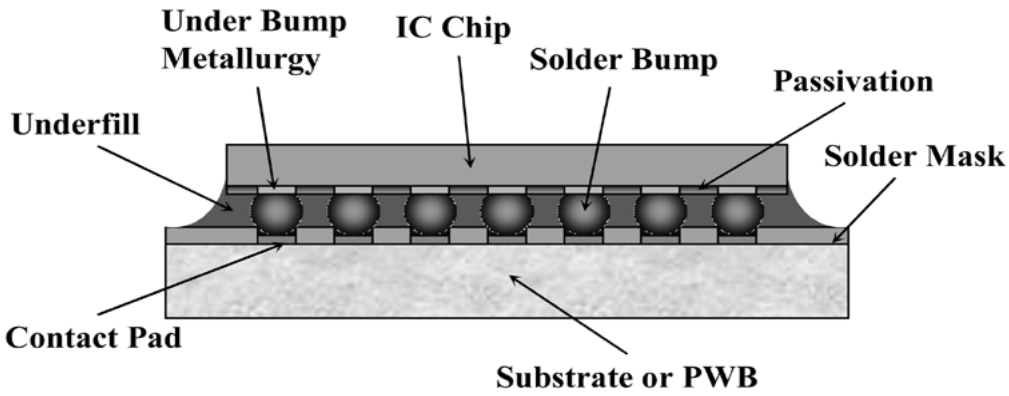


Figure 1: Typical flip chip layout

What is underfill materials ?

Underfill is a liquid encapsulate, usually epoxy resins heavily filled with SiO , that is applied between the chip and the substrate after flip-chip interconnection. Upon curing, the hardened underfill exhibits high modulus, low CTE matching that of the solder joint, low moisture absorption, and good adhesion towards the chip and the substrate.

Why underfill is used in Flip chip ?

Underfill can improve the reliability life of flip-chip device as much as ten folds which provided environmental protection to the device, and to distribute the stress imposed by coefficient thermal expansion (CTE) mismatch between silicon chip and substrate. By using an underfill material, the stress on the solder bumps during temperature cycling has been dispersed over the area of device. Thus, the stress on the device can be reduced and the reliability of the device can be enhanced.

TM 5011 (Evaluation and acceptance procedures for polymeric materials) of MIL-STD-883: TM 5011 does not have provision for underfill materials evaluation/test column in table I. However, JEDEC JC-13.2 task group has made draft requirements for underfill (see attachment # 2) but some users/manufacturers raised some concerns for underfill long term stability with compliance of TM 5011 test requirements as a result this EP study will find more technical information from the underfill suppliers as well as user's community to make acceptable underfill test requirements of table I to TM 5011 and/or to MIL-PRF-38535.

Concerns and issues with underfill: General speaking, underfill materials evaluation and acceptance procedure involved two parties (1) Underfill suppliers (i.e. underfill manufactures) and (2) Users (i.e. flip chip assembly houses/manufacturers). Therefore, it is a dual responsibility, how underfill suppliers performed following tests and acquired certification of performance, on the other hand user communities (i.e. assembly houses) how verify all engineering properties to select the underfill materials for their flip chip devices.

Questionnaire:

1) Since polymeric materials of TM 5011 and flip chip underfill material has different engineering properties and applications process. Therefore, should we update TM 5011 with adding underfill test requirements to table I below? or Add paragraphs in PIDTP of MIL-PRF-38535 with requirements of "selection criteria of underfill materials for flip chip" which must be documented in QM plan. Please provide your feedback and comments.

2) If we prefer to update/add underfill test requirements to TM 5011 then following table I need to review for evaluation and acceptance test for both underfill suppliers and devices assembly houses including devices manufacturers? Provide your comments.

3) Please also discuss/comments how underfill suppliers to comply TM 5011?

Table I: Underfill evaluation and acceptance test

Tests	Underfill suppliers testing responsibilities		Underfill users testing responsibilities	
	Acceptance test (A)	Certification test (C)	Acceptance test (A)	Certification test (C)
Materials test				
Viscosity test				
Pot life test				
Shelf life.				
Underfill cure profile				
Outgassed evaluation				
Ionic impurities.				
Coefficient of linear thermal expansion (CTE)				
Volume resistivity				
Dielectric constant				
Dissipation factor.				
Flux				
Glass transition temperature (Tg)				
Underfill dispense procedure				
Adhesion test				
Moisture absorption				

Selection criteria of underfill materials for flip chip devices PIDTP paragraph of MIL-PRF-38535

Questionnaire:

4) If we prefer to add underfill test requirements to MIL-PRF-38535 to Package integrity demonstration test plan (PIDTP) then following test shall be performed by the underfill suppliers or underfill users, and all underfill profile must be documented to QM plan for QA review and approval. Is this acceptable?

Underfill materials. For selection of underfill materials following materials characteristics shall be tested/examined and verified by the underfill suppliers or underfill users:

Underfill materials evaluation process:

i) **Coefficient of thermal expansion (CTE**): The coefficient of thermal expansion (CTE) of the underfill is the most critical properties for flip chip devices, and underfill CTE should match of the solder bump materials which connecting the die to the substrate.

ii) **Glass transition temperature (Tg)**: The underfill glass transition temperature (Tg) should be chosen 115°C~150°C or higher to maintain underfill CTE match with the solder bumps throughout the reliability tests.

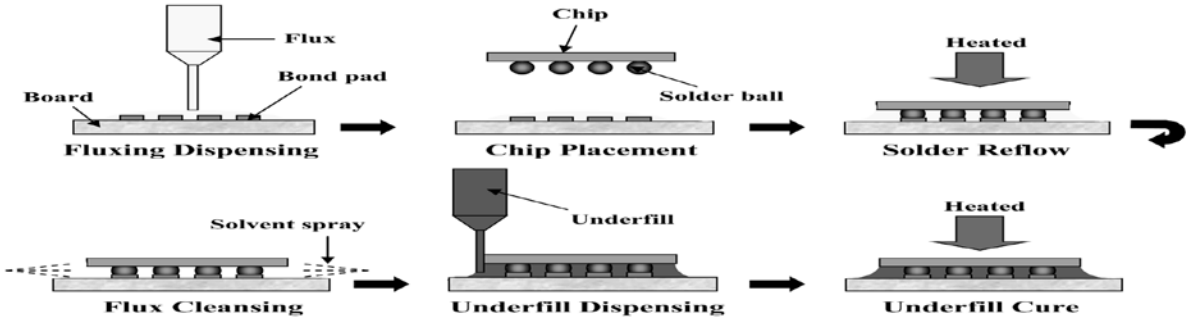
iii) **Viscosity**: The viscosity varied over time (i.e. some cases viscosity increases 30 percent over a 30hr period) and also has an effects underfill dispense flow rate which lead to achieving stable process and a good quality underfill layers. The viscosity of the underfill has to be a room temperature pot life that extends to more than one shift at the IC assembly line. It should also have a long enough shelf life.

iv) **Pot life**: The underfill pot life must be labeled and mentioned on the underfill container. Typical values for the pot life range from 8 to 24 hrs depending on the ability of the dispensing system to handle variation in viscosity over time. The underfill material shall be used within the pot life period after removal from the container, after mixing, or after thawing to room temperature.

v) **The shelf life**: Shelf life of underfill materials is defined as the time that the underfill material continues to meet the requirements of this specification. This shelf life shall be a minimum of 12 months at room temperature (32°C maximum) unless the supplier certifies for some other period of time.

vi) **Flux**: The flux materials shall be compatible with underfill materials.

Underfill application process:



vii) **Underfill dispense flow**: The underfill dispense flow rate measurement can be assessed utilizing tests that have been developed by underfill suppliers/users to get optimum results. Flow properties as the underfill is dispensed from the syringe/needle at the edge of chip to substrate gap area and as the underfill flows under the chip are both important from the users perspective.

viii) **Underfill particle size**: The particles size within the filler and their size distribution determine the speed of underfill dispense flow rate. The largest particle size should be smaller than quarter of the bump height. Typical underfill particles sizes are 10 to 50 micron diameter.

Underfill cure profile:

ix) **Underfill cure time:** Underfill should be cured soon after dispensing and flow out. The curing step should occur within 8 hours after dispensing, unless the assembly is maintained in a controlled (low humidity) environment. A typical underfill cures in 10 minutes at 165°C but cure time can e reduced by employing higher temperatures.

x) **Heating Rate:** This heating rate may influence the quality and reliability of the assembly. Acceptable heating rate is influenced by the mechanical and physical properties of the substrate, topography of the die, and the underfill material. In general, slower heating rates may result in filler settling, but less warpage/stress on the assembly. A fast heating rate (high ramp) for some underfill materials can cause one or more of the reactive monomers to volatilize. Users need to be cognizant of the curing schedule utilized and work closely with the underfill supplier to ensure the desired cured properties are attained.

xi) **Young's Modulas (E) value**: The cured hard underfill young modulus values should be considered as low enough to relive the stress between the die and the substrate during reliability testing. It also needs to be stiff enough to maintain the shape and co-planarity of the package, and help relieve the stress from the solder bump. Select an underfill material that has a modulus value within the 7GPa to 10GPa range.

Underfill materials reliability test:

xii) **Underfill Outgassing test**: Outgassing of the cured material shall be determined in accordance with outgassed moisture and shall be less than or equal to 5,000 ppmv (0.5 percent V/V) for 3 packages (0 failures) or 5 packages (1 failure). Other gaseous species present in quantities greater than or equal to 100 ppmv (0.01 percent V/V) shall be reported in ppmv or percent V/V. The vapor content of the package with getter shall not exceed 2000 ppmv after 24 hours at 150°C and 3000 ppmv after 1000 hours at 150°C.
For non-hermetic applications, outgassing shall be tested in accordance with ASTM E595. Underfill outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.

xiii) **Adhesion test:** The adhesion test of the underfill to the die, solder bumps and substrate determine its ability to prevent delamination, especially under stress. Flip chip packages undergo stresses during post mold cure, solder reflow and reliability tests. Once underfill cured, the die can be tested using die shear, lap shear or stud pull test method. For comparative estimations for the shear/adhesion strength of different materials, a suggested test method is ASTM D1002.

xiv) **Moisture absorption test:** Moisture absorption of underfill encapsulants can be an issue, since absorbed moisture in micro voids/craze sites in critical locations may exacerbate corrosion of aluminum circuitry at the IC. In addition, the Tg, modulus, adhesion, and other properties may be reduced thereby reducing high temperature exposure tolerance and loose adhesion. Pressure cooker test (PCT) shall be performed with applying conditions of 121°C at 2 atm pressure and 100% relative humidity for 96 hours. After moisture absorption C-SAM and stud pull test shall be performed to verify void/delamination of underfill and chip interface.

xv) **Thermal cycling test**: Cured underfill with solder bump shall be performed thermal cycling test for 3,000 cycles and subsequently C-SAM test shall be preformed to verify underfill void and delamination.

5) **Responsibility for testing**: The underfill manufacturer and user are responsible for the performance of all tests as mentioned above. Please provide your comments.

6) **Certification testing.** Certification testing shall be performed on the initial lot of material and for any major changes to the material thereafter and consist of all tests to determine conformance with all requirements specified herein. To insure that both the polymeric material and the processes employing the material are controlled, both the supplier and the user of the material shall be responsible for performance of the tests. Please provide your comments.

7) **Sample size**. The number of samples to be subjected to each testing procedure shall be as specified in the individual test methods. Provide your comments.

8) **Retention of data.** The data generated for certification shall be retained for a period of 5 years or until a recertification is performed, whichever is greater. Provide your comments.

9) **Acceptance testing**. Acceptance tests shall be performed on each lot and shall consist of tests as specified in table I. Provide your comments.

10) **Test lot**. A test lot shall consist of all underfill material manufactured under the same batch number, i.e., a batch number identifies those materials whose constituents can be traced to a single lot of raw materials. Provide your comments.

Attachment #2

TG2010-04
PROPOSED MODIFICATION TO TM5011 FOR UNDERFILLS

Add columns to Table I for Underfills as illustrated (addition highlighted in yellow):

Test or Condition	Test Method Paragraph	Encapsulating Compounds				Underfills			
		Supplier		User		Supplier		User	
		A	C	A	C	A	C	A	C
Materials (3.4.1)	3.8.1	X	X	X	X	x	x	x	x
Viscosity (3.4.2)	3.8.2		X				x		
Pot Life (3.4.3)	3.8.3								
Shelf Life (3.4.4)	3.8.4		X				x		
Thermogravimetric analysis (3.5.2)	3.8.5		X				x		
Outgassed materials (3.5.3)	3.8.6						x		
Ionic impurities(3.5.4)	3.8.7	X	X				x		
Bond strength (3.5.5)	3.8.8	X	X						
Coefficient of linear thermal expansion (3.5.6)	3.8.9		X				x		
Thermal conductivity (3.5.7)	3.8.10		X				x		
Volume resistivity (3.5.8)	3.8.11		X				x		
Type 1 materials							NA		
Type 2 materials			X				x		
Dielectric constant (3.5.9)	3.8.12		X				x		
Dissipation factor (3.5.10)	3.8.13		X				x		
Sequential test environment (3.5.11)	3.8.14								
Density (3.5.12)	3.8.15								
Mechanical integrity (3.5.13)	3.8.16								
Operating life test (3.5.14)	3.8.17				X				

A= Performed at acceptance testing.
C= Performed at certification testing.

Paragraph 3.5.2.1: Add, “Not applicable to Underfills”

Paragraph 3.5.3: Add, “For non-hermetic applications, outgassing shall be tested in accordance with ASTM E595. Spec limits shall be <1% for total mass loss and <0.1% for CVCM”