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IN REPLY REFER TO DSCC-VAT (K Bernier/DSN 850-0563/(614)692-0563) 10 March 2008

MEMORANDUM FOR VSS

SUBJECT: Dated Engineering Practices Study of MIL-PRF-55365 Voltage de-rating for inrush current to capacitors during use.
Project number 5910-2008-001

The subject engineering practices study is dated 10 March 2008. If you have any questions please contact the project officer Ken Bernier, by email at Kenneth.bernier@dla.mil or by phone at 614-692-0563.

Michael A. Radecki
Chief
Electronic Components Team

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ENGINEERING PRACTICE STUDY

TITLE: DERATING OF APPLIED VOLTAGE TO TANTALUM CAPACITORS

PROJECT NUMBER 5910-2008-001

10 March 2008
(approval date)

STUDY PROJECT (SEE ENCLOSED)

FINAL REPORT

Study conducted by Ken Bernier

Prepared by:

Ken Bernier
DSCC-VAT

Approved by:

Michael A. Radecki
Chief
Electronic Component Team

EP STUDY: DERATING OF APPLIED VOLTAGE TO TANTALUM CAPACITORS
PROJECT NUMBER 5910-2008-001

OBJECTIVE: Gather information on de-rating practices in Space and Military applications for Tantalum capacitors.

PROBLEM BACKGROUND:
An end user is questioning the limitation to 40% of rated voltage applied to circuit capacitors. The 40% of rated voltage is in the Aerospace Technical Operating Reports (TOR) document (TOR-5236A). The initial draft is out for comment and contains the 40% of rated voltage reference cited by Lockheed Martin.

REASON FOR LIMITING CURRENT INRUSH

A high current in-rush application is defined as one where over one ampere of charging current is available to the capacitor. With the advent of surface mount technology and the associated closer interconnection distances, the actual series resistance available in applications has reduced, making transients an even more important consideration. When tantalum capacitors are used in such low series impedance applications they are subject to large current in-rushes, especially if the source supply is of low impedance. During initial testing of assemblies, this environment can produce a low, but measurable PPM (Parts Per Million) fallout of early life failures under certain circuit conditions.

During the surge current testing of capacitors tested by the manufacturers, the applied voltage is controlled during its application by using a regulated power supply. The power source is required to have an energy storage bank capacity of 50,000uF across the output terminals.

A look at the capacitor charging equation shows how easily the 1 amp can be exceeded:

$$I = \frac{E}{R}\left(1 - e^{\frac{-t}{RC}}\right)$$

Where I = current amps
E = voltage in volts
R = resistance in ohms
C = capacitance if farads
T = time in seconds

It can be calculated that if the voltage, resistance, time, and capacitance remain constant then the amount of inrush current is proportional to the applied voltage. As the voltage increases so does the inrush current.

REASONS FOR TEST REQUIREMENTS:

In a conversation with The Aerospace Corp. application engineers concerning inrush current, they stated that the current inrush to a capacitor can cause early life failures. To prevent these failures they require that there be a method for controlling the amount of current charging the capacitors. This problem can be easily controlled by limiting the applied voltage.

SUPPORTING INFORMATION:

Study concerning the 0.1 ohm/volt series resistance. When the surge current is tested during the capacitor manufacturing process both the input resistance and the voltage are tightly controlled. There are no stray voltages and the input current is tightly controlled. When the part is used in a design the user may not have tight control over the voltage application, transients, current. There may be an inrush of current that is detrimental to the capacitor.

The following information will help to explain the reasoning used to limit the voltage applied to capacitors without sufficient current flow resistance.

INCREASING RELIABILITY OF SMD TANTALUM CAPACITORS IN LOW IMPEDANCE APPLICATIONS
by David Mattingly Applications Engineer Myrtle Beach, SC

A high current in-rush application is defined as one where over one ampere of charging current is available to the capacitor. With the advent of surface mount technology and the associated closer interconnection distances, the actual series resistance available in applications has reduced, making transients an even more important consideration. When tantalum capacitors are used in such low series impedance applications they are subject to large current in-rushes, especially if the source supply is of low impedance. During initial testing of assemblies, this environment can produce a low, but measurable PPM (Parts Per Million) fallout of early life failures under certain circuit conditions.

Today, AVX references one hundred milliohms per working volt for standard steady state reliability on all of its tantalum product lines. These changes are a direct result of advances in manufacturing processes and increases in the purity of capacitor grade tantalum powders. However, these recommendations are for steady state conditions within circuits and do not directly address dynamic conditions (i.e. voltage and current transients).

See article from AVX at this web site: http://www.avxcorp.com/docs/techinfo/tantimp.pdf

VOLTAGE DERATING RULES FOR SOLID TANTALUM AND NIOBIUM CAPACITORS
T. Zednicek, J. Gill

For many years, whenever people have asked tantalum capacitor manufacturers for general recommendations on using their product, the consensus was “a minimum of 50% voltage de-rating should be applied”. This rule of thumb has since become the most prevalent design guideline for tantalum technology. This paper revisits this statement and explains, given an understanding of the application, why this is not necessarily the case.

See article from AVX at this web site: http://www.avxcorp.com/docs/techinfo/voltaged.pdf

MIL-PRF-55365G Surge current test during manufacture of capacitors.

4.7.18 Surge current (optional) (see 3.21). This test, when specified (see 1.2.1.7), shall be performed on a 100 percent basis either before or after Weibull/voltage aging as indicated in 4.7.18a. Capacitors shall be subjected to ten cycles at each temperature:

a. Temperature: Option A: (+25°C ±5°C; after Weibull grading or voltage aging) or
Option B: (-55°C +5°C, -0°C and +85°C ±5°C; after Weibull grading or voltage aging) or
Option C: (-55°C +5°C, -0°C and +85°C ±5°C; before Weibull grading or voltage aging).
Option Z or no option: No test required.

b. Applied voltage: Rated dc voltage ±2 percent from a power source having an energy storage bank of 50,000 µF (minimum) across the output terminals.

c. Charge cycle: 4 seconds ±1 second.

d. Discharge cycle: 4 seconds ±1 second to a voltage below 1 percent of rated voltage.

e. The total dc resistance (excluding the capacitor) including the wiring, fixturing, and output impedance of the regulated power supply to each test position during the charging cycle shall be a maximum of 1.2 ohm.

After the final cycle, the dc leakage, capacitance, and dissipation factor shall be measured as specified in 4.7.6, 4.7.7, and 4.7.8, respectively.

CONCLUSION:

For many years, whenever people have asked tantalum capacitor manufacturers for general recommendations on using their product, the consensus was “a minimum of 50% voltage de-rating should be applied”. This rule of thumb has since become the most prevalent design guideline for tantalum technology.

RECOMMENDATIONS:
For Aerospace to require that the voltage be limited to 40% of the maximum applied voltage is not unreasonable, given the applications they have.