ENGINEERING PRACTICES STUDY

TITLE: Soldering Heat Testing For Semiconductors

October 27, 2004

STUDY PROJECT 5961-2911

FINAL REPORT

Study Conducted by Alan Barone

Prepared by

Alan Barone

I. OBJECTIVE: The objective of this project was to create guidance on how to invoke solder heat testing for each semiconductor package technology. In addition our objective was to study and determine sample size, frequency of test and failure criteria.

II. BACKGROUND: See preliminary EP Study, dated 20 February 2004 (See attachment 1).

III. RESULTS: Microsemi submitted an alternate method from the MIL-STD-202 proposal. This proposal was sent out as part of a JC 13 ballot which DSCC rejected. At the September 2004 JEDEC meeting (see attendees list, attachment 2) in Columbus Ohio a task group meeting (TG 0304) was held to discuss the soldering heat study. The individual package testing has yet to be specified in MIL-PRF-19500. This will require additional effort by the industry during the MIL-PRF-19500 document coordination phase.

IV. CONCLUSION: DSCC has committed to incorporating the contents of TM 210 from MIL-STD-202 into TM 2031 of MIL-STD-750 Revision “E” in total. The package technology groupings will be incorporated in MIL-STD-750E to invoke the applicable test procedures. MIL-PRF-19500 Revision “N” will contain the specific requirements for semiconductor devices. A sample size of 3 devices per test will be required by the manufacturers to prove device capability. This qualification test will be specified in Group E of MIL-PRF-19500N for all devices. DSCC will not allow any reduction of test or alternate testing without supporting data to justify alternate methods of testing for soldering heat.

V. RECOMMENDATIONS: Recommend that military and industry representative review the latest drafts of MIL-PRF-19500N and MIL-STD-750E for incorporation of soldering heat test. See test method 2031 in attachment 3. See proposed technology groupings in attachment 4.

Attachment 1

ENGINEERING PRACTICES STUDY

TITLE: Standardization On Soldering Heat Testing For Semiconductors

February 20, 2004

STUDY PROJECT 5961-2911

REPORT

Study Conducted by Alan Barone

Prepared by

Alan Barone

I. <u>OBJECTIVE</u>: The objective of this project is to address the need for a resistance to soldering heat test to simulate the users soldering process. This will include the following:

a. Determine which test conditions apply to each package.
b. Determine failure criteria.
c. Determine package groupings for acceptance.
d. Determine sample size for each test condition.
e. Determine implementation and frequency of the soldering heat test.

II. <u>BACKGROUND</u>:

a. NASA has reported some problems and failures while performing hand soldering.
b. Army's essential comment for 5961 is as follows:

"*For surface mount glass, ceramic, or plastic devices it is recommended that MIL-STD-202G, method 210F, dated 8 Feb 2002, test conditions I, J, K (as applicable) be proposed to the industry for use until a MIL-STD-750 method can be developed. Method 202 G conditions A (soldering), C (wave top side), and D (bottom side) may also need to be considered based on construction (eg TO-254 AA-package) and expected applications. It is also requested that this test be incorporated into Group C as a periodic test to address process and material variations. It is not unreasonable to impose this test on a periodic sample of devices from a family of devices (as allowed by Group C)."*

Soldering heat test method 2031 has become a global issue. DSCC first added method 2031 of MIL-STD 750 to all glass diode specifications after reports of cracked glass and cracked die occurred. Specifically, after the 1N4148-1 NASA alert was written. Army submitted an essential comment for periodic testing due to variation in process and materials. Army requested all surface mount devices be tested to 2031.

Industry is now objecting to this test. The following issues have been brought to my attention:

1. This test has references to diodes and not to transistors. (see attachment 1).
2. Frequency of test.
3. Package and design sensitivity (see attachment 1), particularly surface mount packages.
4. Sample size.
5. Redundancy with solderability.
6. Number of cycles & temperature extreme.
7. Cost driver with no benefit.

Industry has commented that certain packages and designs like glass diodes have a direct thermal path to the die and are sensitive to this test. Many package do not have this feature and are thought not to be sensitive to this test. RHA MOSFETS in power packages are very expensive and the supplier's claim TM 2031 is an unacceptable cost driver. While DSCC recognizes the importance of cost, our primary concern is that of quality and reliability for our customers.

DSCC has requested this subject be put on the JC-22, JC-25, and JC-13.1 agenda's for further discussion. We have formed a soldering heat task group at JC-13.1 and at JC-13.5. The 2031 test method needs to be re-written using MIL-STD-202 METHOD 210 as a baseline. DSCC is looking for data to justify the Army request to expand the scope of this test to group C (periodic), while the manufacturers object to the group E (qualification) implementation of TM 2031 for devices not susceptible to soldering heat. Any information or insight the Army and device manufacturers can provide in this issue to support their position would be greatly appreciated.

The users at JEDEC G-12 (January 04) meeting commented that there are many soldering profiles including hand soldering. The suppliers are asking for the users and government to identify their soldering process and profiles, while at the same time users want the devices characterized in terms of their design capability. Suppliers are calling for users to understand the procedures, which govern hand soldering to boards. Suppliers are accusing users of violating device ratings and safe soldering practices. A soldering expert will be speaking on this issue at the next JEDEC meeting.

Suppliers have made the following comments:

"Here's what I believe you should do with this request. Remove the requirement from all existing slash sheets. This requirement (if needed) should reside in the general spec 19500 and I propose that you perform an EP study to determine relevance."

Martin Enright

"It is a little difficult to derive the costs for implementing this proposed test method in Group C, as the specific devices/package-types and test conditions are not fully defined. The requester suggests conditions I, J, K, A, C and D may (all?) be appropriate, which implies a range of necessary equipment from a simple soldering iron to vapor phase reflow chambers. If applied to all ceramic surface mount packages with these proposed test conditions, the implementation cost could range from modest to quite significant.

More importantly, the benefits are far too vaguely defined to justify even modest implementation costs. From a Semicoa perspective, if the request continues to apply to a broad set of package types, it is appropriate to address in 19500 (as suggested by Martin Enright at IR). A slash-sheet approach seems appropriate (and manage-able) only if the request can be narrowed in scope to particular constructions with historical soldering-heat issues."

Regards,
Dave Dickens

Engineering Manager, Semicoa

III. <u>DISCUSSIONS</u>: After reviewing the various inputs from the military departments, NASA, semiconductor manufacturers and equipment manufacturers, DSCC offers the following:

a. The current method 2031 in MIL-STD-202 does not address the various methods used for soldering semiconductors. The method only simulates a solder-dip process for diodes. Today there is no wave solder, infrared or vapor phase simulations and the method is inadequate in that respect. MIL-STD-202 method 210 offers a bench mark for passive components that could be incorporated into method 2031 to address these deficiencies and tailor requirements to the semiconductor industry.

b. After trying to resolve the military essential comments on soldering heat by including the existing method 2031 into MIL-PRF-19500 spec sheets, DSCC has concluded that this approach is not workable. As noted previously, the existing method 2031 is not adequate. Furthermore, trying to resolve this issue at the specification sheet is a piecemeal approach at best that will take years to incorporate into the hundreds of MIL-PRF-19500 spec sheets. DSCC is of the opinion that this approach is not in the interest of the government or industry.

c. This soldering heat issue should be addressed at the general specification level in MIL-PRF-19500. When the government and industry have agreed on the technical approach a single change can be made to MIL-PRF-19500 and the change is invoked across all spec sheets. No spec sheets would have to be modified. To this end, we have requested the military agencies that have submitted essential comments to date on this issue, wait and allow these comments to be addressed via this EP Study and the subsequent action on the general specification MIL-PRF-19500.

IV. PROPOSAL: DSCC proposes the following steps to achieve this plan:

1. To address the current deficiencies in method 2031, the following attached revised test method is being distributed for your review and comments. (Note: This is a derivative of the MIL-STD-202 method 210).
2. To facilitate invoking the soldering heat requirements in the general spec versus changing every spec sheet DSCC has prepared a grouping of semiconductor packages. The applicable soldering heat test conditions shall be performed on each package family to prove design capability. See attachment 2 for package family grouping and applicable test conditions. DSCC solicits input from the military/industry on the test conditions proposed.
3. To address the issue of where to perform the new soldering heat method, soldering heat would be performed in Group E and invoked on all applicable detail specifications by 19500.
4. Periodical testing shall be performed as applicable on a case-by-case basis on sensitive packages only. Suppliers shall submit a list of their sensitive packages as applicable.
5. Each supplier shall submit their proposed package family from their qualified parts for review.
6. A sample size of 3 devices with zero failures would be required for each applicable test condition.
7. Group A, subgroup 2, electrical endpoints and hermetic seal would be performed after the resistance to soldering heat for failure criteria.

V. CONCLUSION: DSCC believes we cannot solve our soldering heat issues at the specification sheet level. We must address a global plan with MIL-PRF-19500 that will invoke soldering heat on all applicable products with the specific conditions and requirements that are applicable for our different technologies and packages.

VI. RECOMMENDATIONS: DSCC will address Army's essential comments with this EP study and with the help of the JEDEC committees and task groups.

DSCC will incorporate the results of this study into MIL-STD-750 and MIL-PRF-19500.

METHOD 2031.1

RESISTANCE TO SOLDERING HEAT

1. PURPOSE. This test is performed to determine whether wire and other component parts can withstand the effects of the heat to which they will be subjected during the soldering process (solder iron, solder dip, solder wave, or solder reflow). The heat can be either conducted heat through the termination into the component part, or radiant heat from the solder bath when in close proximity to the body of the component part, or both. The solder dip method is used as a reasonably close simulation of the conditions encountered in wave soldering, in regard to radiated and conducted heat. This test also is intended to evaluate the impact of reflow techniques to which components may be exposed. The heat of soldering can cause solder reflow which may affect the electrical characteristics of the component part and may cause mechanical damage to the materials making up the part, such as loosening of terminations or windings, softening of insulation, opening of solder seals, and weakening of mechanical joints.

2. APPARATUS.

2.1 Solder pot. A static solder pot, of sufficient size to accommodate the mounting board (see 2.4) and to Immerse the terminations to the depth specified for the solder dip (without touching the bottom of the pot), shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified. The solder bath temperature shall be measured in the center of the pot at a depth of at least .500 inch (12.7 mm), but no deeper than 1 inch (25.4 mm) below the surface of the solder.

2.2 Heat sinks or shielding. The use of heat sinks or shielding is prohibited except when it is a part of the component. When applicable, heat sinks or shielding shall be specified in the individual specification, including all of the details, such as materials, dimensions, method of attachment, and location of the necessary protection.

2.3 Fixtures. Fixtures, when required, shall be made of a non-solderable material designed so that they will make minimum contact (i.e., minimum heat sink) with the component. Further, they shall not place undue stress on the component when fixtured.

2.4 Mounting board. A mounting board, in accordance with NEMA grade FR-4 of IPC-4101, 9 square inches (i.e., 3 x 3, 1 x 9, etc.), minimum area, .062 inch ±.0075 inch (1.57 mm ±.191 mm) thick, shall be used, unless otherwise specified. Component lead holes shall be drilled such that the diametrical clearance between the hole and component terminals shall not exceed .015 inch (0.38 mm). Metal eyelets or feed-throughs shall not be used. Surface mount boards, when specified in the individual specification, shall have pads of sufficient size and number to accommodate the component being tested.

2.5 Solder iron. A solder iron, capable of maintaining a temperature of 350°C ±10°C, shall be used.

2.6 Reflow chambers. The reflow chambers or equivalent (Vapor Phase Reflow (VPR) chamber, Infrared Reflow (IRR) oven, air circulating oven, etc.) shall be of sufficient size to accommodate the mounting board and components to be tested. The chamber shall be capable of generating the specified heating rate, temperatures, and environments.

2.7 Temperature measurement. Low mass thermocouples that do not affect the heating rate of the sample shall be used. A temperature recording device is recommended. The equipment shall be capable of maintaining an accuracy of ±1°C at the temperature range of interest.

3. MATERIALS.

3.1 Solder. The solder or solder paste shall be tin-lead alloy with a nominal tin content of 50 percent to 70 percent in accordance with ANSI/J-STD-006, “Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications” or ANSI/J-STD-005, “Requirements for Soldering Pastes”. When specified in the individual specification, other solders can be used provided they are molten at the specified temperature.

3.2 Flux. When flux is used, it shall conform to type A of ANSI/J-STD-004, "Requirements for Soldering Fluxes", or as specified in the individual specification.

3.3 VPR fluid. A perfluorocarbon fluid that has a boiling point of 215°C shall be used.

4. PROCEDURE.

4.1 Special preparation of specimens. Any special preparation of specimens prior to testing shall be as specified in the individual specification. This could include specific instructions such as bending or any other relocation of terminations, cleaning, application of flux, pretinning, or attachment of heat sinks or protective shielding (see 2.2), prior to the solder immersion.

4.2 Preparation of solder bath. The molten solder shall be agitated to assure that the temperature is uniform. The surface of the solder shall be kept clean and bright.

4.3 Application of flux. When flux is used, the terminations to be tested shall be immersed in the flux (see 3.2), which is at room ambient temperature, to the depth specified for the solder dip. The duration of the immersion shall be from 5 seconds to 10 seconds.

4.4 Test conditions. Unless otherwise specified in the individual specification, the test shall be performed on all solder terminations attached to the component part. There are six types of soldering techniques covered by these test conditions. The test conditions are outlined below and in table I.

Test condition A:	Solder iron - Hand soldering of solder cups, through hole components, tab and post terminations, solder eyelet terminations.
Test condition B:	Solder dip - Simulates hot solder dipping (tinning) of leaded components.
Test condition C:	Wave solder - Simulates wave solder of topside board mount product.
Test condition D:	Wave solder - Simulates wave solder of bottom side board mount product.
Test condition H:	VPR - VPR environment without preheat.
Test conditions I, J, K:	Infrared/Convection reflow - Simulates IRR, natural convection, and forced air convection reflow environments.

4.4.1 Test condition A: Solder iron.

a. When testing a solder cup, tab and post termination, or solder eyelet termination, the applicable wire size, properly prepared for the solder termination, shall be attached in the appropriate manner.

When testing a board mount component, the component shall be placed on a mounting board (see 2.4).

b. When specified, the components shall be fluxed (see 4.3).

c. Unless otherwise specified, a solder iron in accordance with 2.5 shall be used.

d. The solder iron shall be heated to 350°C ±10°C and applied to the termination for a duration of 4 seconds to 5 seconds as specified in table I. The solder and iron shall be applied to the area of the assembly closest to the component body that the product is likely to experience. For surface mount components, the iron shall be placed on the pad only.

e. Remove the iron and allow the component to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

f. The component shall be visually examined under 10X magnification.

4.4.2 Test condition B: Solder dip.

a. Place the component in an appropriate fixture (see 2.3).

b. When specified, the leads shall be fluxed (see 4.3).

c. The specific combination of temperature, immersion and emersion rate, immersion duration, and number of heats shall be as specified in table I. Unless otherwise specified, terminations shall be immersed to within .050 inch (1.27 mm) of the component body. Terminations shall be immersed simultaneously, if the geometry of the component permits.

d. After the solder dip, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

e. The component shall be visually examined under 10X magnification.

4.4.3 Test condition C: Wave solder - topside board mount component.

a. The component under test shall be mounted on a mounting board (see 2.4).

   Wire leads: Wire leads shall be brought through the board holes and bent at least 30 degrees from a line perpendicular to the board. Leads shall extend from .050 inch to .100 inch (1.27 mm to 2.54 mm) from the bottom of the board. Axial leads shall be bent at a 90° angle at a point between .06 inch and .08 inch (1.5 mm and 2.1 mm) from the body, eyelet fillet or weld unless otherwise specified (see figure 210-1).

   Pin leads: Where the component is designed with rigid pin leads, the full length of the termination shall be retained. Pin leads shall not be cut or bent (see figure 210-1).

b. When specified, the leads shall be fluxed (see 4.3).

c. The specific combination of temperature, duration, and number of heats shall be as specified in table I.

d. The components, mounted on the board, shall be immersed in the solder pot so that the bottom of the board floats on the molten solder.

e. After the float, the components shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the components shall be cleaned using an appropriate cleaning solution.

f. The components shall be visually examined under 10X magnification.

4.4.4 Test condition D: Wave solder – bottom side board mount product.

a. Place the component in an appropriate fixture (see 2.3).

b. When specified, the terminations shall be fluxed (see 4.3).

c. The specific combination of temperature, preheat conditions, immersion and emersion rates, immersion duration, and number of heats shall be as specified in table I.

d. The component shall be preheated and fully immersed in the solder bath in accordance with 4.4.4c.

e. After the immersion, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

f. The component shall be visually examined under 10X magnification.

4.4.5 Test condition H: Vapor phase reflow soldering.

a. Components shall be mounted on a mounting board (see 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber (see 2.6) shall be used which is large enough to suspend the mounting board without touching the sides or the solution. The VPR fluid shall be placed in the test chamber and shall be heated until it is boiling. The solution shall be allowed to boil for 5 minutes prior to suspending the mounting board.

c. The specific combination of temperature, duration of exposure, and number of heats shall be as specified in table I.

d. After chamber equalization, the mounting board shall be suspended into the vapor in a horizontal plane. The mounting board shall not touch the solution.

e. After the heat, the components shall be allowed to cool and stabilize at room ambient conditions. If a solder paste was used, the component shall be cleaned using an appropriate solution.

f. The components shall be visually examined under 10X magnification.

4.4.6 Test conditions I, J, K: Infared/convection reflow soldering.

a. Components shall be mounted on a mounting board (see 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber as specified in 2.6 shall be used.

c. A low mass thermocouple shall be attached tightly to the component at an appropriate position away from the edges.

d. The specific combination of temperature, preheat, duration, and number of heats shall be as specified by test condition I, J, or K in table I and the individual procurement document.

e. The board shall be placed into the test chamber and the temperature of the component ramped at a rate of 1°C/s to 4°C/s as measured by the thermocouple. The assembly shall be above 183°C for 90 seconds to 120 seconds and held at the final temperature and time designated by the test condition. The assembly shall then be allowed to cool to room ambient temperature. This constitutes one heat cycle. The assembly shall be exposed to three heat cycles.

f. The components shall be visually examined under 10X magnification.

5. EXAMINATIONS AND MEASUREMENTS. Examinations and measurements to be made before and after the test, as applicable, shall be as specified in the individual specification. After the procedure, the specimens shall be allowed to cool and stabilize at room ambient conditions, for the time specified in the individual specification.

5.1 Internal examination. When specified, internal examination of the part shall be made after the test to check for solder reflow or heat damage.

6. SUMMARY. The following details are to be specified in the individual specification:

a. The use of heat sinks or shielding is prohibited except when they are part of the component (see 2.2).

b. Mounting board, if different from that specified (see 2.4).

c. Solder, if different from that specified (see 3.1).

d. Flux, if applicable and if different from that specified (see 3.2, 4.1, and 4.3).

e. Solder terminations that are not to be tested, if applicable (see 4.4).

f. Special preparation of specimens if applicable (see 4.1).

g. Depth of immersion in the molten solder, if different from that specified (see 4.4.2).

h. Test condition letter (see 4.4).

i. Cooling time prior to final examinations and measurements (see 4.4 and 5).

j. Examinations and measurements before and after test, as applicable (see 5).

k. Method of internal inspection, if required (see 5.1).

TABLE I. Test conditions.

Solder technique simulation	Test condition	Temperature (°C)	Time (s)	Temperature ramp/ immersion and emersion rate	Number of heat cycles
Solder iron	A	350 ±10 (solder iron temp)	4 - 5		1
Dip	B	260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s	1
Wave: Topside board-mount product	C	260 ±5 (solder temp)	20 ±1		1
Wave: Bottomside board-mount product	D	260 ±5 (solder temp)	10 ±1	Preheat 1°C/s-4°C/s to within 100°C of solder temp. 25 mm/s ± 6 mm/s	1
	E	CANCELLED			
	F	CANCELLED			
	G	CANCELLED			
Vapor phase reflow	H	215 ±5 (vapor temp)	60 ±5		1
IR/convection reflow	I	215 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3
	J	235 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3
	K	250 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3

Test condition E is cancelled; use test condition C.
Test condition F is cancelled; use test condition B.
Test condition G is cancelled.

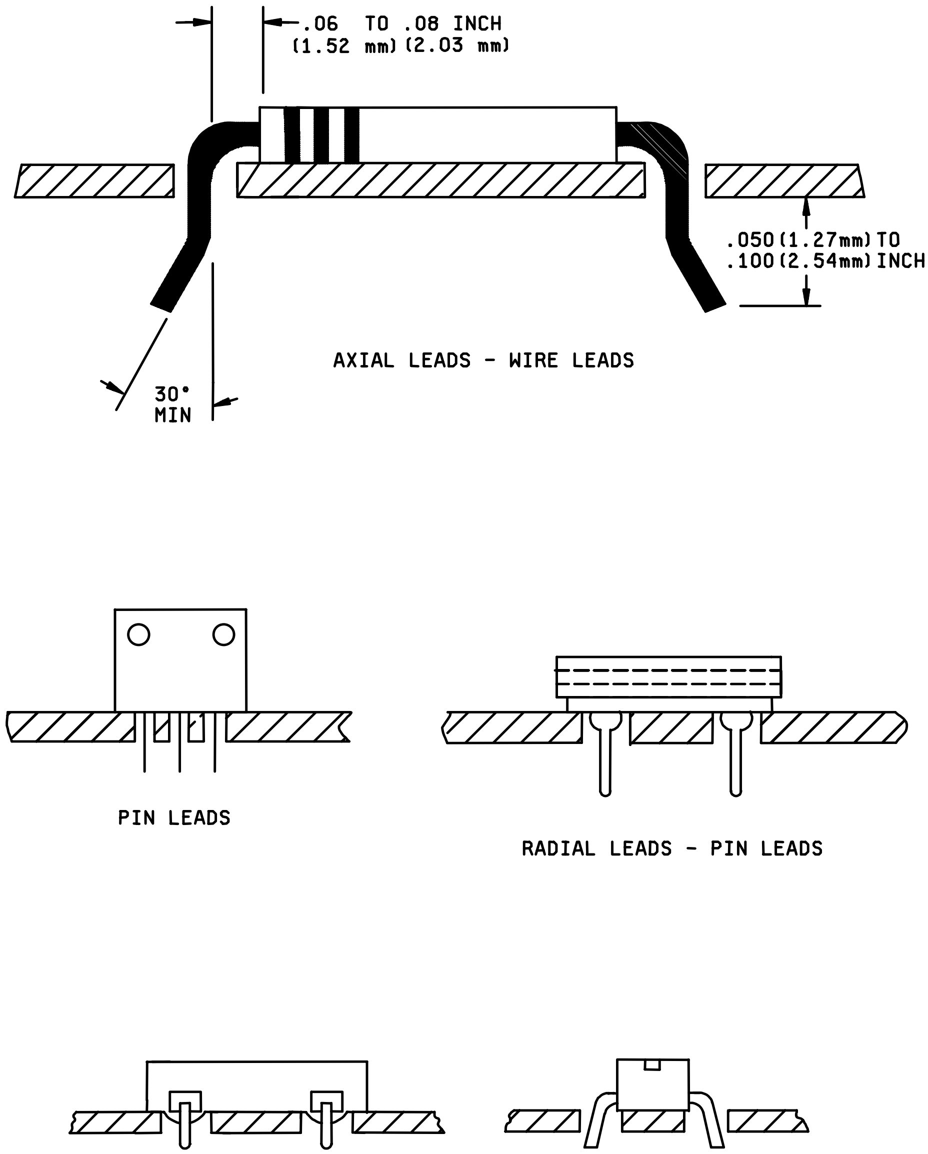

FIGURE 1. Component lead and mounting examples.

International
IR Rectifier
HI-REL PRODUCTS

205 Crawford Street
Leominster MA 01453

Date: 10/8/03

Defense Supply Center Columbus
3990 East Broad Street
Columbus OH 43216
ATT'N Mr. Alan Barone (DSCC-VAC)

Dear Mr. Barone

Internal Rectifier does not agree (in fact we strongly disagree) with the decision to add solder heat to group E tests for MOSFETS detail performance specifications. We have not seen or discussed any rationale for applying this test to our products.

During the die attach process our product is exposed to peak temperatures up to approximately 360 degrees centigrade for two to three minutes depending on the materials involved. This temperature and dwell time is far in excess of the requirements of the solder heat test currently under consideration for inclusion in the slash sheets. Furthermore, the test method 2031 currently specified, was specifically written for glass body diodes and does not apply to our products.

Before any new specification requirements are added to the slash sheets, the sponsor/proponent of the requested action needs to justify (with data) the need for change. In addition, this topic should be discussed at JEDEC/G12 where we can all get some appreciation of the magnitude of the problem prior to implementation.

To better serve our customers, International Rectifier constantly strive to eliminate non value added cost drivers from our product base and even though this requirement is only performed in device qualification, we see it as a meaningless (non value added)cost driver.

Please respond at your earliest convenience as we are holding up issuing kits to manufacturing until this is resolved.

Should you have any questions, please feel free to call me at any time

Sincerely,

Martin Enright

Director of Quality Assurance

Package Family Grouping Proposal

1. Case mounted cans	condition A & C
2. Lead mounted cans	condition A & C
3. Axial leaded Glass (tungsten) class I bond	condition A & C
4. Glass surface mount (tungsten) class I bond	condition A, C & H
5. Glass surface mount (dumet) class II & III bond	condition A, C, H, & I
6. Axial leaded Glass (dumet) class II & III bond	condition A & C
7. Case mounted packages with ceramic seals	condition A & C
8. Dual In line packages	condition A & C
9. Flat packs	condition A & C
10. UA and UB	condition A, C, H & I
11. U1 thru U4 Also known as SMD1, 2, .5 and .22	conditions A, C, H & I

12. Studs are exempt from any soldering heat testing

A- Soldering iron
C- Topside wave solder
H- Vapor phase
I- Infrared

Attachment 2

COMMITTEE TASK GROUP SIGN-IN SHEET

DATE(S):	COMMITTEE/ SUBCOMMITTEE	NAME OF MEETING SITE	LOCATION
9/21/04	DSCC TG 0304 – Alan Barone Resistance to Soldering Practices	The Columbus	Columbus, Ohio

THIS SIGN-IN SHEET IS **ONLY** FOR PERSONS ATTENDING THIS TASK GROUP MEETING.

NAME (PLEASE PRINT LEGIBLY)	STATUS: MEMB. (M) ALTER. (A) GUEST (G)	COMPANY	TELEPHONE	E-MAIL	✓ If your contact info has changed
Alan Barone	G	DSCC			
John Nirschl	G-12	Rockwell Collins	319 295 3111	jwnirsch@rockwellcollins.com	
Wes Hubbell	G-12	Raytheon	727-302-3198	whha@raytheon.com	
Roy Brown	G-12	Honeywell	816-997-3983	rbrown@kcp.com	
Joe Zaccari	G-12	Curfin Industries	503 293 7212	JZACCARI@CURFIN.com	
Mike Cooper	G-12	GD C4S	508-880-4059	mike.cooper@gdc4s.com	
Beth Parker	A	Microsemi Lawrence	978 620 2636	bparker@microsemi.com	
Ray DiBugnara	M	Microsemi	978 620 2614	rdibugnara@microsemi.com	
Jeffrey Carver	G	US Army CECOM	732-370-3494		
Dave Moore	G	DSCC	(614) 692-0675	David.E.Moore@dla.mil	
Tom Hess	G	DSCC-VAC	(614) 692-0547	thomas.hess@dla.mil	
Martin Enright	G.	I.R.	(978) 534-5776	MENRIGHT@IRF.Com	
Alan Johnson	M	Semicoa, Costa Mesa CA	714-242-3014	ajohnson@semicoa.com	
David Diguangco	G	USAF	801-777-1412	Dave.Diguangco@hill.af.mil	
Masao Nakamura	G	Nippon Avionics	+81-45-304-8245	nakamura-masao@avio.co.jp	
Takahiro Sazaki	G	Nippon Avionics	+81-45-304-8245	sazaki-takar@avio.co.jp	

TO ALL PARTICIPANTS: Subjects improper for consideration under the JEDEC "Legal Guidelines" shall not be discussed at this meeting or elsewhere. See Part I, General Guides, reverse side. See Special Guides in Parts II and II for engineering standardization and marketing data programs, respectively. Consult the JEDEC General Counsel about any doubtful questions.

Rev. 09/03

JEDEC

COMMITTEE TASK GROUP SIGN-IN SHEET

DATE(S):	COMMITTEE/ SUBCOMMITTEE	NAME OF MEETING SITE	LOCATION
9/21/04	DSCC TG 0304 – Alan Barone Resistance to Soldering Practices	The Columbus	Columbus, Ohio

NAME (PLEASE PRINT LEGIBLY)	STATUS: MEMB. (M) ALTER. (A) GUEST (G)	COMPANY	TELEPHONE	E-MAIL	✓ If your contact info has changed
THIS SIGN-IN SHEET IS **ONLY** FOR PERSONS ATTENDING THIS TASK GROUP MEETING.					
Kazuhiro Toda	G	Advanced Engineering Services	+81-29-868-2222	toda.kazuhiro@jaxa.jp	
ROGER FRESCH	M	Raytheon	310-647-3573	RAFRESCH@Raytheon.com	
Kyle Carpenter	G	DSCC-VQE	(614) 692-7078	Kyle.Carpenter@dla.mil	
Jason Hochstetler	G	DSCC-VAC	614 692-7106	Jason.hochstetler@dla.mil	
RONAN DILLON	G	MICROSEMI IRELAND	+353 65686 9129	rdillon@microsemi.com	
CARL MOWRY	A	MICROSEMI	561-746-9778	cmowry@microsemi.com	
HUY CAO	A	I.R.	(310) 726-8764	Rcao1@irf.com	
MAX ZAFRANI	G	I.R	978-621-1147	MZAFRANI@IRF.com	
KELLY PRICE	M	I.R	978-514-6457	KPRICE@IRF.com	

TO ALL PARTICIPANTS: **Subjects improper for consideration under the JEDEC "Legal Guidelines" shall not be discussed at this meeting or elsewhere. See Part I, General Guides, reverse side. See Special Guides in Parts II and II for engineering standardization and marketing data programs, respectively. Consult the JEDEC General Counsel about any doubtful questions.**

Attachment 3

MIL-STD-750
METHOD 2031.1

RESISTANCE TO SOLDERING HEAT

1. PURPOSE. This test is performed to determine whether wire and other component parts can withstand the effects of the heat to which they will be subjected during the soldering process (solder iron, solder dip, solder wave, or solder reflow). The heat can be either conducted heat through the termination into the component part, or radiant heat from the solder bath when in close proximity to the body of the component part, or both. The solder dip method is used as a reasonably close simulation of the conditions encountered in wave soldering, in regard to radiated and conducted heat. This test also is intended to evaluate the impact of reflow techniques to which components may be exposed. The heat of soldering can cause solder reflow which may affect the electrical characteristics of the component part and may cause mechanical damage to the materials making up the part, such as loosening of terminations or windings, softening of insulation, opening of solder seals, and weakening of mechanical joints.

2. APPARATUS.

2.1 Solder pot. A static solder pot, of sufficient size to accommodate the mounting board (see 2.4) and to Immerse the terminations to the depth specified for the solder dip (without touching the bottom of the pot), shall be used. This apparatus shall be capable of maintaining the solder at the temperature specified. The solder bath temperature shall be measured in the center of the pot at a depth of at least .500 inch (12.7 mm), but no deeper than 1 inch (25.4 mm) below the surface of the solder.

2.2 Heat sinks or shielding. The use of heat sinks or shielding is prohibited except when it is a part of the component. When applicable, heat sinks or shielding shall be specified in the individual specification, including all of the details, such as materials, dimensions, method of attachment, and location of the necessary protection.

2.3 Fixtures. Fixtures, when required, shall be made of a non-solderable material designed so that they will make minimum contact (i.e., minimum heat sink) with the component. Further, they shall not place undue stress on the component when fixtured.

Mounting board. A mounting board, in accordance with NEMA grade FR-4 of IPC-4101, 9 square inches (i.e., 3 x 3, 1 x 9, etc.), minimum area, .062 inch ±.0075 inch (1.57 mm ±.191 mm) thick, shall be used, unless otherwise specified. Component lead holes shall be drilled such that the diametrical clearance between the hole and component terminals shall not exceed .015 inch (0.38 mm). Metal eyelets or feed-throughs shall not be used. Surface mount boards, when specified in the individual specification, shall have pads of sufficient size and number to accommodate the component being tested.

2.5 Solder iron. A solder iron, capable of maintaining a temperature of 350°C ±10°C, shall be used.

2.6 Reflow chambers. The reflow chambers or equivalent (Vapor Phase Reflow (VPR) chamber, Infrared Reflow (IRR) oven, air circulating oven, etc.) shall be of sufficient size to accommodate the mounting board and components to be tested. The chamber shall be capable of generating the specified heating rate, temperatures, and environments.

2.7 Temperature measurement. Low mass thermocouples that do not affect the heating rate of the sample shall be used. A temperature recording device is recommended. The equipment shall be capable of maintaining an accuracy of ±1°C at the temperature range of interest.

3. MATERIALS.

3.1 Solder. The solder or solder paste shall be tin-lead alloy with a nominal tin content of 50 percent to 70 percent in accordance with ANSI/J-STD-006, “Requirements for Electronic Grade Solder Alloys and Fluxed and Non-Fluxed Solid Solders for Electronic Soldering Applications” or ANSI/J-STD-005, “Requirements for Soldering Pastes”. When specified in the individual specification, other solders can be used provided they are molten at the specified temperature.

3.2 Flux. When flux is used, it shall conform to type A of ANSI/J-STD-004, “Requirements for Soldering Fluxes”, or as specified in the individual specification.

3.3 VPR fluid. A perfluorocarbon fluid that has a boiling point of 215°C shall be used.

4. PROCEDURE.

4.1 Special preparation of specimens. Any special preparation of specimens prior to testing shall be as specified in the individual specification. This could include specific instructions such as bending or any other relocation of terminations, cleaning, application of flux, pretinning, or attachment of heat sinks or protective shielding (see 2.2), prior to the solder immersion.

4.2 Preparation of solder bath. The molten solder shall be agitated to assure that the temperature is uniform. The surface of the solder shall be kept clean and bright.

4.3 Application of flux. When flux is used, the terminations to be tested shall be immersed in the flux (see 3.2), which is at room ambient temperature, to the depth specified for the solder dip. The duration of the immersion shall be from 5 seconds to 10 seconds.

4.4 Test conditions. Unless otherwise specified in the individual specification, the test shall be performed on all solder terminations attached to the component part. There are six types of soldering techniques covered by these test conditions. The test conditions are outlined below and in table I.

Test condition A: Solder iron - Hand soldering of solder cups, through hole components, tab and post terminations, solder eyelet terminations.

Test condition B: Solder dip - Simulates hot solder dipping (tinning) of leaded components.

Test condition C: Wave solder - Simulates wave solder of topside board mount product.

Test condition D: Wave solder - Simulates wave solder of bottom side board mount product.

Test condition H: VPR - VPR environment without preheat.

Test conditions I, J, K: Infrared/Convection reflow - Simulates IRR, natural convection, and forced air convection reflow environments.

4.4.1 Test condition A: Solder iron.

a. When testing a solder cup, tab and post termination, or solder eyelet termination, the applicable wire size, properly prepared for the solder termination, shall be attached in the appropriate manner.

When testing a board mount component, the component shall be placed on a mounting board (see 2.4).

b. When specified, the components shall be fluxed (see 4.3).

c. Unless otherwise specified, a solder iron in accordance with 2.5 shall be used.

d. The solder iron shall be heated to 350°C ±10°C and applied to the termination for a duration of 4 seconds to 5 seconds as specified in table I. The solder and iron shall be applied to the area of the assembly closest to the component body that the product is likely to experience. For surface mount components, the iron shall be placed on the pad only.

e. Remove the iron and allow the component to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

The component shall be visually examined under 10X magnification.

4.4.2 Test condition B: Solder dip.

a. Place the component in an appropriate fixture (see 2.3).

b. When specified, the leads shall be fluxed (see 4.3).

c. The specific combination of temperature, immersion and emersion rate, immersion duration, and number of heats shall be as specified in table I. Unless otherwise specified, terminations shall be immersed to within .050 inch (1.27 mm) of the component body. Terminations shall be immersed simultaneously, if the geometry of the component permits.

d. After the solder dip, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

e. The component shall be visually examined under 10X magnification.

4.4.3 Test condition C: Wave solder - topside board mount component.

a. The component under test shall be mounted on a mounting board (see 2.4).

Wire leads: Wire leads shall be brought through the board holes and bent at least 30 degrees from a line perpendicular to the board. Leads shall extend from .050 inch to .100 inch (1.27 mm to 2.54 mm) from the bottom of the board. Axial leads shall be bent at a 90° angle at a point between .06 inch and .08 inch (1.5 mm and 2.1 mm) from the body, eyelet fillet or weld unless otherwise specified (see figure 210-1).

Pin leads: Where the component is designed with rigid pin leads, the full length of the termination shall be retained. Pin leads shall not be cut or bent (see figure 210-1).

b. When specified, the leads shall be fluxed (see 4.3).

c. The specific combination of temperature, duration, and number of heats shall be as specified in table I.

d. The components, mounted on the board, shall be immersed in the solder pot so that the bottom of the board floats on the molten solder.

e. After the float, the components shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the components shall be cleaned using an appropriate cleaning solution.

f. The components shall be visually examined under 10X magnification.

4.4.4 Test condition D: Wave solder – bottom side board mount product.

a. Place the component in an appropriate fixture (see 2.3).

b. When specified, the terminations shall be fluxed (see 4.3).

c. The specific combination of temperature, preheat conditions, immersion and emersion rates, immersion duration, and number of heats shall be as specified in table I.

d. The component shall be preheated and fully immersed in the solder bath in accordance with 4.4.4c.

e. After the immersion, the component shall be allowed to cool and stabilize at room ambient conditions. If flux was used, the component shall be cleaned using an appropriate cleaning solution.

f. The component shall be visually examined under 10X magnification.

4.4.5 Test condition H: Vapor phase reflow soldering.

a. Components shall be mounted on a mounting board (see 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber (see 2.6) shall be used which is large enough to suspend the mounting board without touching the sides or the solution. The VPR fluid shall be placed in the test chamber and shall be heated until it is boiling. The solution shall be allowed to boil for 5 minutes prior to suspending the mounting board.

c. The specific combination of temperature, duration of exposure, and number of heats shall be as specified in table I.

d. After chamber equalization, the mounting board shall be suspended into the vapor in a horizontal plane. The mounting board shall not touch the solution.

e. After the heat, the components shall be allowed to cool and stabilize at room ambient conditions. If a solder paste was used, the component shall be cleaned using an appropriate solution.

f. The components shall be visually examined under 10X magnification.

4.4.6 Test conditions I, J, K: Infared/convection reflow soldering.

a. Components shall be mounted on a mounting board (see 2.4). Through-hole mounted components shall have their terminals inserted into the termination holes. Surface mount components shall be placed on top of the board.

b. A test chamber as specified in 2.6 shall be used.

c. A low mass thermocouple shall be attached tightly to the component at an appropriate position away from the edges.

d. The specific combination of temperature, preheat, duration, and number of heats shall be as specified by test condition I, J, or K in table I and the individual procurement document.

e. The board shall be placed into the test chamber and the temperature of the component ramped at a rate of 1°C/s to 4°C/s as measured by the thermocouple. The assembly shall be above 183°C for 90 seconds to 120 seconds and held at the final temperature and time designated by the test condition. The assembly shall then be allowed to cool to room ambient temperature. This constitutes one heat cycle. The assembly shall be exposed to three heat cycles.

f. The components shall be visually examined under 10X magnification.

5. EXAMINATIONS AND MEASUREMENTS. Examinations and measurements to be made before and after the test, as applicable, shall be as specified in the individual specification. After the procedure, the specimens shall be allowed to cool and stabilize at room ambient conditions, for the time specified in the individual specification.

5.1 Internal examination. When specified, internal examination of the part shall be made after the test to check for solder reflow or heat damage.

6. SUMMARY. The following details are to be specified in the individual specification:

The use of heat sinks or shielding is prohibited except when they are part of the component (see 2.2).

Mounting board, if different from that specified (see 2.4).

c. Solder, if different from that specified (see 3.1).

d. Flux, if applicable and if different from that specified (see 3.2, 4.1, and 4.3).

e. Solder terminations that are not to be tested, if applicable (see 4.4).

f. Special preparation of specimens if applicable (see 4.1).

g. Depth of immersion in the molten solder, if different from that specified (see 4.4.2).

h. Test condition letter (see 4.4).

i. Cooling time prior to final examinations and measurements (see 4.4 and 5).

j. Examinations and measurements before and after test, as applicable (see 5).

k. Method of internal inspection, if required (see 5.1).

TABLE I. Test conditions.

Solder technique simulation	Test condition	Temperature (°C)	Time (s)	Temperature ramp/ immersion and emersion rate	Number of heat cycles
Solder iron	A	350 ±10 (solder iron temp)	4 - 5		1
Dip	B	260 ±5 (solder temp)	10 ±1	25mm/s ±6 mm/s	1
Wave: Topside board-mount product	C	260 ±5 (solder temp)	20 ±1		1
Wave: Bottomside board-mount product	D	260 ±5 (solder temp)	10 ±1	Preheat 1°C/s-4°C/s to within 100°C of solder temp. 25 mm/s ± 6 mm/s	1
	E	CANCELLED			
	F	CANCELLED			
	G	CANCELLED			
Vapor phase reflow	H	215 ±5 (vapor temp)	60 ±5		1
IR/convection reflow	I	215 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3
	J	235 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3
	K	250 ±5 (component temp)	30 ±5	1°C/s-4°C/s; time above 183°C, 90 s - 120 s	3

Test condition E is cancelled; use test condition C.
Test condition F is cancelled; use test condition B.
Test condition G is cancelled.

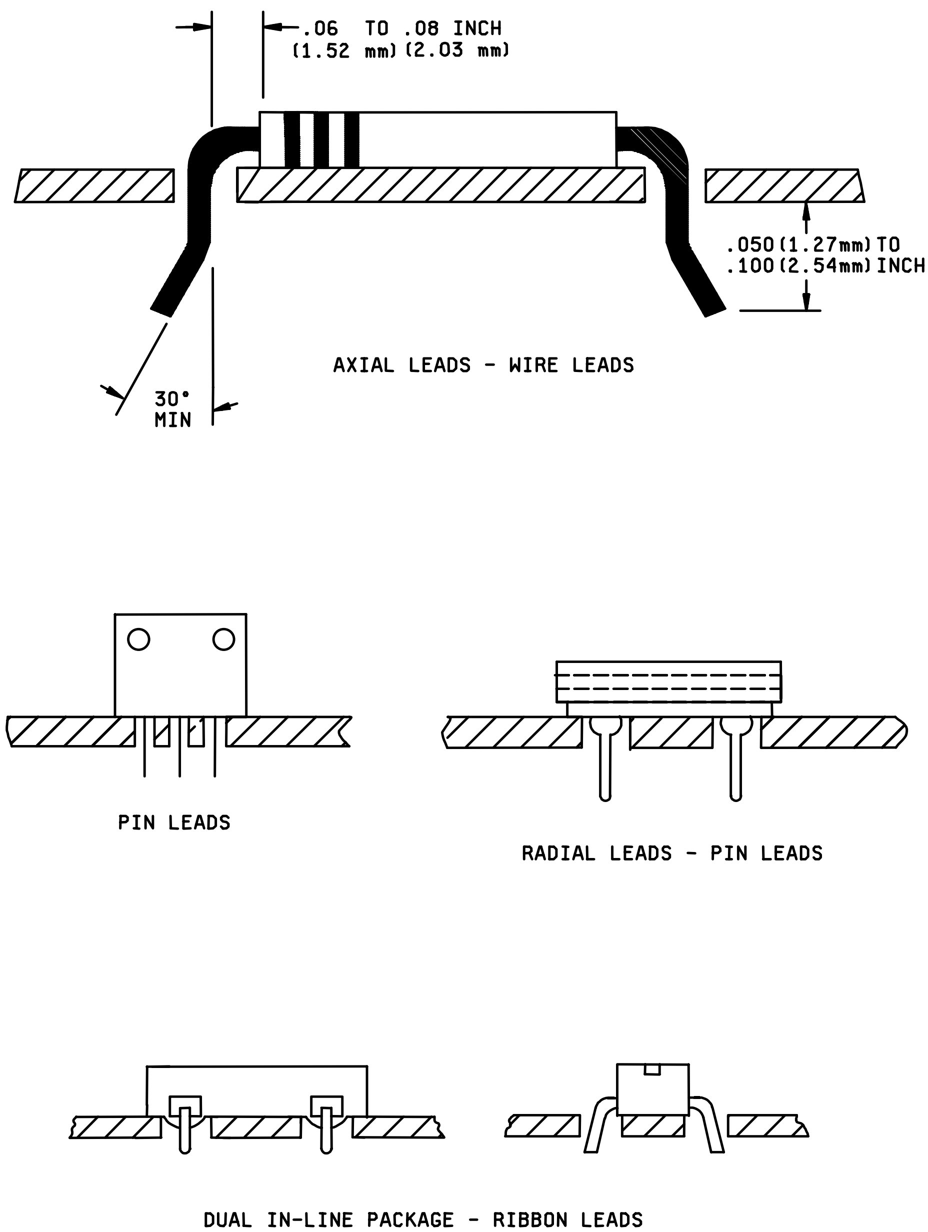

FIGURE 1. Component lead and mounting examples.

Attachment 4

Package Family Grouping Proposal

1. Case mounted cans	condition A & C
2. Lead mounted cans	condition A & C
3. Axial leaded Glass (tungsten) class I bond	condition A & C
4. Glass surface mount (tungsten) class I bond	condition A, C & H
5. Glass surface mount (dumet) class II & III bond	condition A, C, H, & I
6. Axial leaded Glass (dumet) class II & III bond	condition A & C
7. Case mounted packages with ceramic seals	condition A & C
8. Dual In line packages	condition A & C
9. Flat packs	condition A & C
10. UA and UB	condition A, C, H & I
11. U1 thru U4 Also known as SMD1, 2, .5 and .22	conditions A, C, H & I
12. Studs are exempt from any soldering heat testing	

A- Soldering iron
C- Topside wave solder
H- Vapor phase
I- Infrared