

ENGINEERING PRACTICES STUDY

TITLE: PROPOSAL TO ADD A LEAD/CARRIER BOARD OPTION FOR SURFACE
MOUNT DEVICES IN MIL-PRF-19500 SLASH SHEETS

30 July 2015

STUDY PROJECT (SEE ATTACHMENT 1)

FINAL REPORT

Study Conducted by DLA LAND AND MARITIME

Project Number: 5961-2015-067

Prepared by:

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I. **OBJECTIVES:** DLA Land and Maritime-VAC conducted an engineering practice study to review a proposal to add an option to order applicable surface mount devices with leads or carrier boards added by the original manufacturer. The purpose of this study was to determine whether the following proposal is an acceptable solution for adding this option to specification sheets.

II. **BACKGROUND:** Users have requested that we add an option to be able to order select surface mount devices with leads or carrier boards added by the manufacturer. This option aids in installation and enhances thermal characteristics for some types of mounting configurations. At the time of this study there was no provision to order these types of configurations in MIL-PRF-19500 specification sheets. At this time these device configurations are being ordered as needed using requirements created by the user. Adding this option to the specification sheet will standardize the requirements for these configurations for MIL-PRF-19500 devices.

1. **Proposal.** This new proposal will standardize the screening and qualification requirements to be performed on applicable surface mount devices with lead/carrier added. See attachment 1 for a slash sheet containing the proposed format highlighted in **yellow**.

2. **Marking.** The proposal states the marking of the lead/carrier configuration shall be marked on the device or the packaging. This is to allow manufacturers to add leads, or carrier boards, to devices that they have currently in their existing inventory which would already be marked with the standard surface mount PIN (ie, JANS2N7524U2). In these instances when using devices in stock, remarking the device with the additional "L" (Flat leads) or "S" (Carrier board) suffix may not be easily performed.

III. **RESULTS:** The comments received by DLA Land and Maritime have been reviewed and indicate that the lead and carrier board proposal for specification sheets is acceptable. In addition, further clarification of the power rating, thermal rating, and SOA rating should be added. These ratings for the devices that use the lead/carrier shall be specified or a note shall be added to indicate the ratings are the same as the standard version without the lead/carrier.

IV. **CONCLUSIONS:** Based on the comments received we will use the highlighted portion of the attached slash sheet as the boiler plate for adding a lead/carrier board option to specification sheets.

V. **RECOMMENDATIONS:** DLA Land and Maritime recommends that this attached format, along with further clarification of the thermal and power ratings of the device be utilized for all future MIL-PRF-19500 specification sheets that include a manufacturer added lead/carrier board.

Attachment 1

NOTE: This draft, dated 20 January 2014, was prepared by DLA - CC, has not been approved and is subject to modification. **DO NOT USE PRIOR TO APPROVAL.** Project 5967-201-0333. COMMENTS DUE BY 30 Apr 2014. P.O.C. Robert Perry, 614-32-5516



INCH-POUND
MIL-PRF-19500/733D
DRAFT
SUPERSEDING
MIL-PRF-19500/733C
18 April 2014

PERFORMANCE SPECIFICATION SHEET

* **TRANSISTOR, FIELD EFFECT RADIATION HARDENED
P-CHANNEL, SILICON DEVICE, TYPES 2N7523T1, 2N7523U2, 2N7524T1, AND 2N7524U2,
JANTXVR, F AND JANSR, F**

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and MIL-PRF-19500.

1. SCOPE

1.1 Scope. This specification covers the performance requirements for an P-channel, enhancement-mode, MOSFET, radiation hardened (total dose and single event effects (SEE)), power transistor. Two levels of product assurance (JANTXV and JANS) are provided for each device type as specified in MIL-PRF-19500, with avalanche energy maximum rating (E_{AS}) and maximum avalanche current (I_{AS}) for use in particular power-switching applications. See 6.5 for JANHC and JANKC die versions.

* 1.2 Package outlines. The device package outlines are as follows: TO-254AA in accordance with figure 1 and SMD2 TO-276AC (U2) in accordance with figure 2, and 3, for all encapsulated device types. The dimensions and topography for JANHC and JANKC unencapsulated die are as listed in slash sheet MIL-PRF-19500/741.

1.3 Maximum ratings. Unless otherwise specified, T_A = +25°C.

Type	P _T (1) T _C = +25°C	P _T T _A = +25°C (free air)	R _{θJC} (2)	V _{DS}	V _{DG}	V _{GS}	I _{D1} (3) (4) T _C = +25°C	I _{D2} (3) (4) T _C = +100°C	I _S	I _{DM} (5)	T _J and T _{STG}
	<u>W</u>	<u>W</u>	<u>°C/W</u>	<u>V dc</u>	<u>V dc</u>	<u>V dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A dc</u>	<u>A(pk)</u>	<u>°C</u>
2N7523T1	208	2.60	0.60	-30	-30	±20	-45	-45	-45	-180	
2N7523U2	250	1.60	0.50	-30	-30	±20	-56	-56	-56	-224	-55
2N7524T1	208	2.60	0.60	-60	-60	±20	-45	-45	-45	-180	to
2N7524U2	250	1.60	0.50	-60	-60	±20	-56	-56	-56	-224	+150

- (1) Derate linearly by 2.00 W/°C (U2) or 1.67 W/°C (T1) for T_C > +25°C.
- (2) See figure 4, thermal impedance curves.
- (3) The following formula derives the maximum theoretical I_D limit. I_D is limited by package design and device construction, to 45 A for T1 or to 56 A for U2.

$$I_D = \sqrt{\frac{T_{JM} - T_C}{(R_{\theta JC}) \times (R_{DS(on)} \text{ at } T_{JM})}}$$

- (4) See figure 5, maximum drain current graph.
- (5) I_{DM} = 4 X I_{D1}, as defined in note (3).

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to Semiconductor@dla.mil. Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

* 1.4 Primary electrical characteristics at $T_c = +25^\circ\text{C}$.

Type	Min $V_{(BR)DSS}$ $V_{GS} = 0$ $I_D = 1.0$ mA dc	$V_{GS(TH)}$ $V_{DS} \geq V_{GS}$ $I_D = 1.0$ mA dc		Max I_{DSS1} $V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS}	Max $r_{DS(ON)}$ (1) $V_{GS} = 12$ V dc		EAS at I_{D1}	IAS
					$T_J = +25^\circ\text{C}$ at I_{D2}	$T_J = +150^\circ\text{C}$ at I_{D2}		
					<u>V dc</u>	<u>V dc</u>		
		Min	Max					
2N7523T1	-30	-2.0	-4.0	-10	0.014	0.016	1250	-45
2N7523U2	-30	-2.0	-4.0	-10	0.013	0.015	1116	-56
2N7524T1	-60	-2.0	-4.0	-10	0.018	0.027	890	-45
2N7524U2	-60	-2.0	-4.0	-10	0.016	0.026	725	-56

(1) Pulsed (see 4.5.1).

* 1.5 Part or Identifying Number (PIN). The PIN is in accordance with MIL-PRF-19500, and as specified herein. See 6.4 for PIN construction example and 6.5 for a list of available PINs.

* 1.5.1 JAN certification mark and quality level for encapsulated devices. The quality level designators for encapsulated devices that are applicable for this specification sheet from the lowest to the highest level are as follows: "JANTXV" and "JANS".

* 1.5.2 JAN brand and quality level designators for unencapsulated devices (die). See 6.7 for unencapsulated devices.

* 1.5.3 Radiation hardness assurance (RHA) designator. The RHA levels that are applicable for this specification sheet from lowest to highest for JANTXV and JANS quality levels are as follows: "M", "D", "P", "L", and "R".

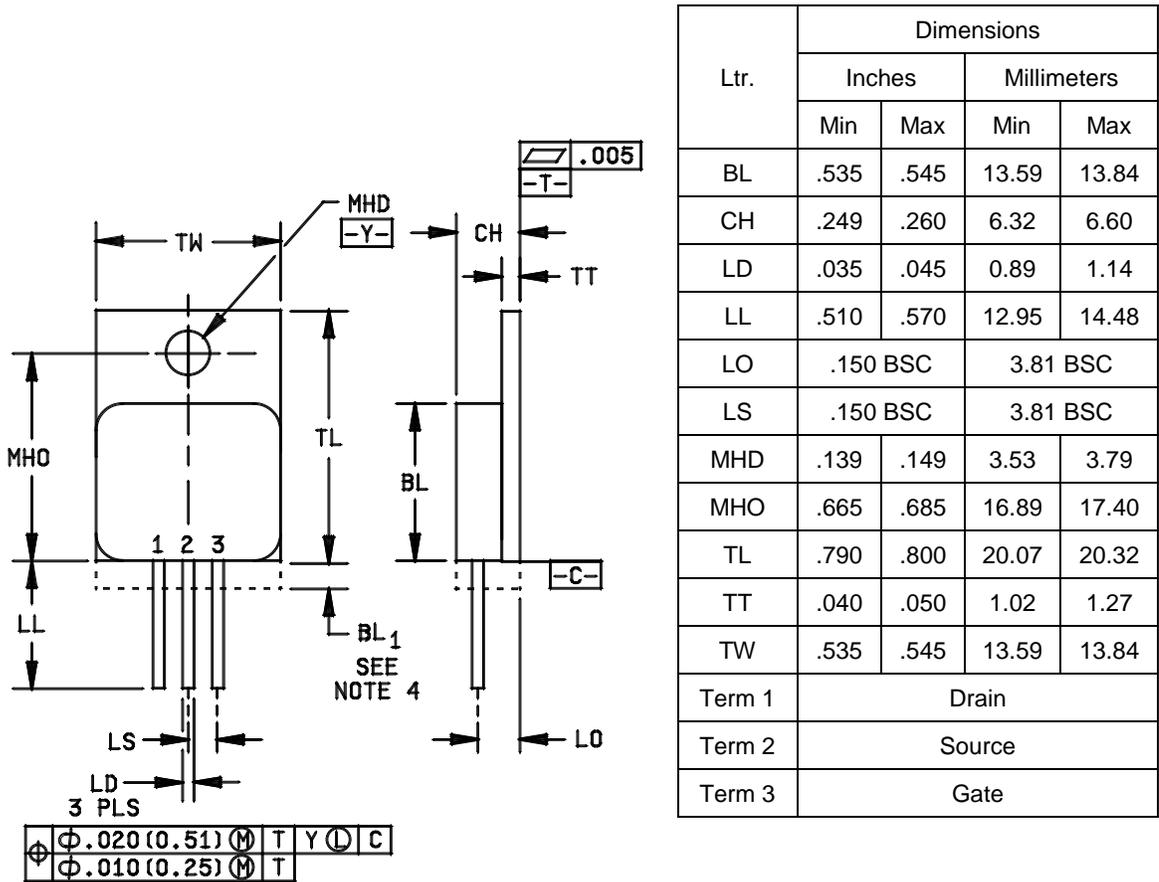
* 1.5.4 Device type. The designation system for the device types of transistors covered by this specification sheet are as follows.

* 1.5.4.1 First number and first letter symbols. The transistors of this specification sheet are identified by the first number and letter symbols "2N".

* 1.5.4.2 Second number symbols. The second number symbols for the transistor covered by this specification sheet are as follows: "7523" and "7524".

* 1.5.4.3 Suffix letters. The suffix letters "T1" are used on devices that are packaged in the TO-254AA package of figure 1. The suffix letters "U2" are used on devices that are packaged in the SMD2 TO-276AC package of figure 2. The suffix letters "U2L" are used on devices that are packaged in the SMD2 TO-276AC package and have additional flat leads added, see figure 3. The suffix letters "U2S" are used on devices that are packaged in the SMD2 TO-276AC package mounted to a carrier board, see figure 3.

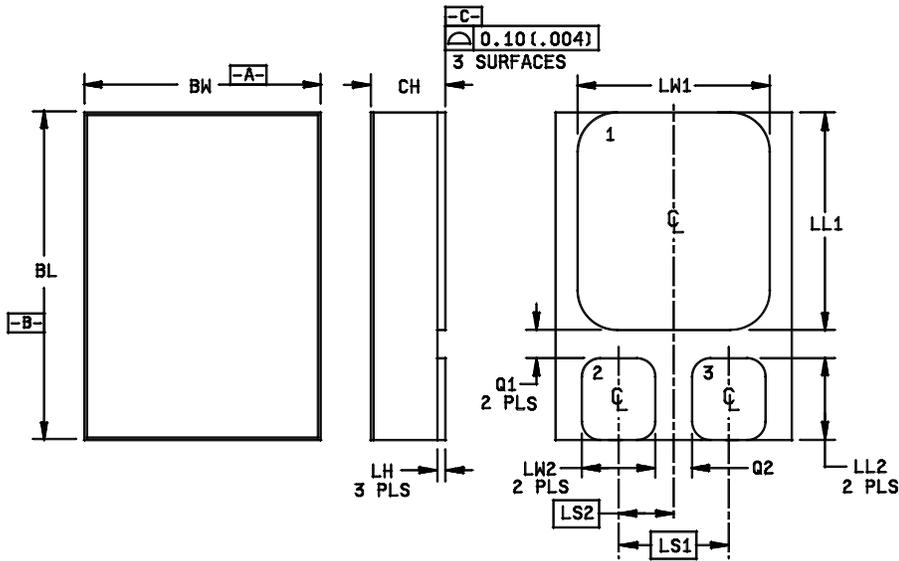
* 1.5.5 Lead finish. The lead finishes applicable to this specification sheet are listed on QML-19500.



NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. All terminals are isolated from the case.
4. This area is for the lead feed-thru eyelets (configuration is optional, but will not extend beyond this zone).
5. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 1. Physical dimensions for TO-254AA (2N7523T1 and 2N7524T1).



Symbol	Dimensions			
	Inches		Millimeters	
	Min	Max	Min	Max
BL	.685	.695	17.40	17.65
BW	.520	.530	13.21	13.46
CH		.142		3.61
LH	.010	.020	0.25	0.51
LW1	.435	.445	11.05	11.30
LW2	.135	.145	3.43	3.68
LL1	.470	.480	11.94	12.19
LL2	.152	.162	3.86	4.12
LS1	.240 BSC		6.10 BSC	
LS2	.120 BSC		3.05 BSC	
Q1	.035		0.89	
Q2	.050		1.27	
TERM 1	Drain			
TERM 2	Gate			
TERM 3	Source			

NOTES:

1. Dimensions are in inches.
2. Millimeters are given for general information only.
3. The lid shall be electrically isolated from the drain, gate and source.
4. In accordance with ASME Y14.5M, diameters are equivalent to ϕ x symbology.

FIGURE 2. Physical dimensions for SMD2 TO-276AC (2N7523U2 and 2N7524U2).

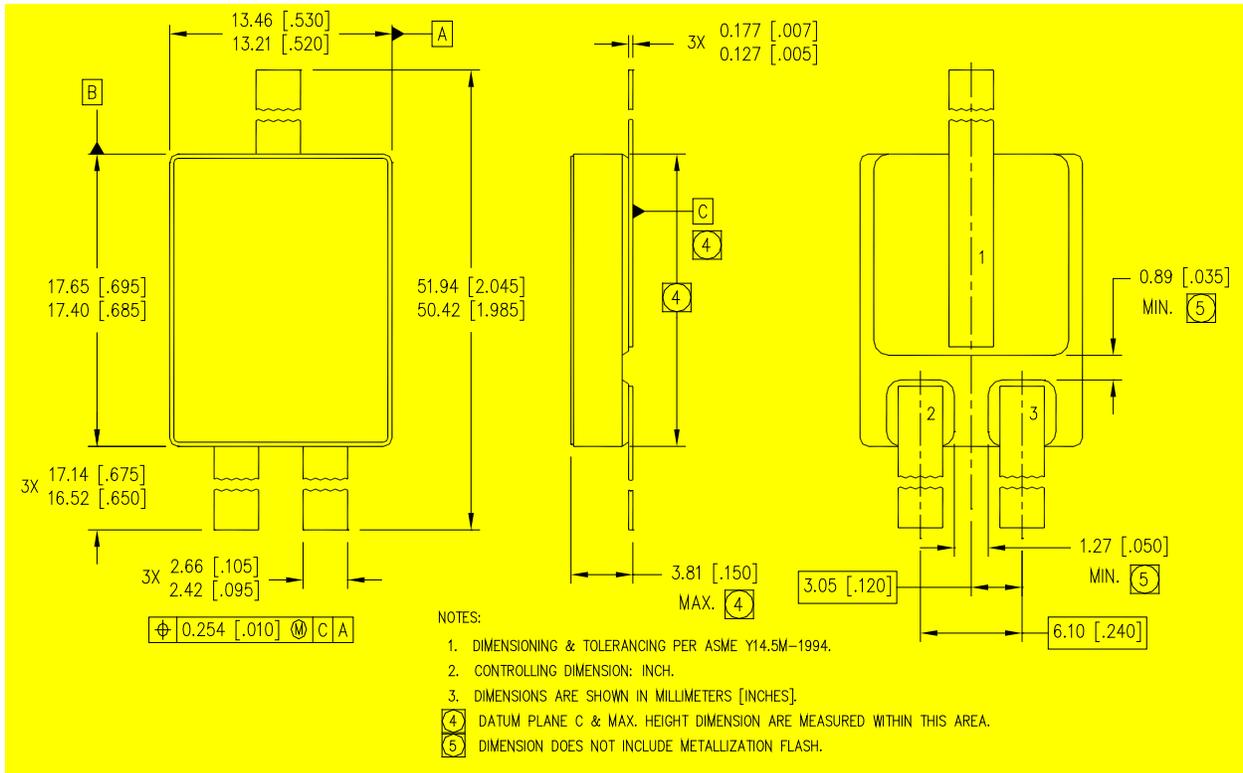


Figure 3. Physical dimensions, U2 with leaded option (U2L).

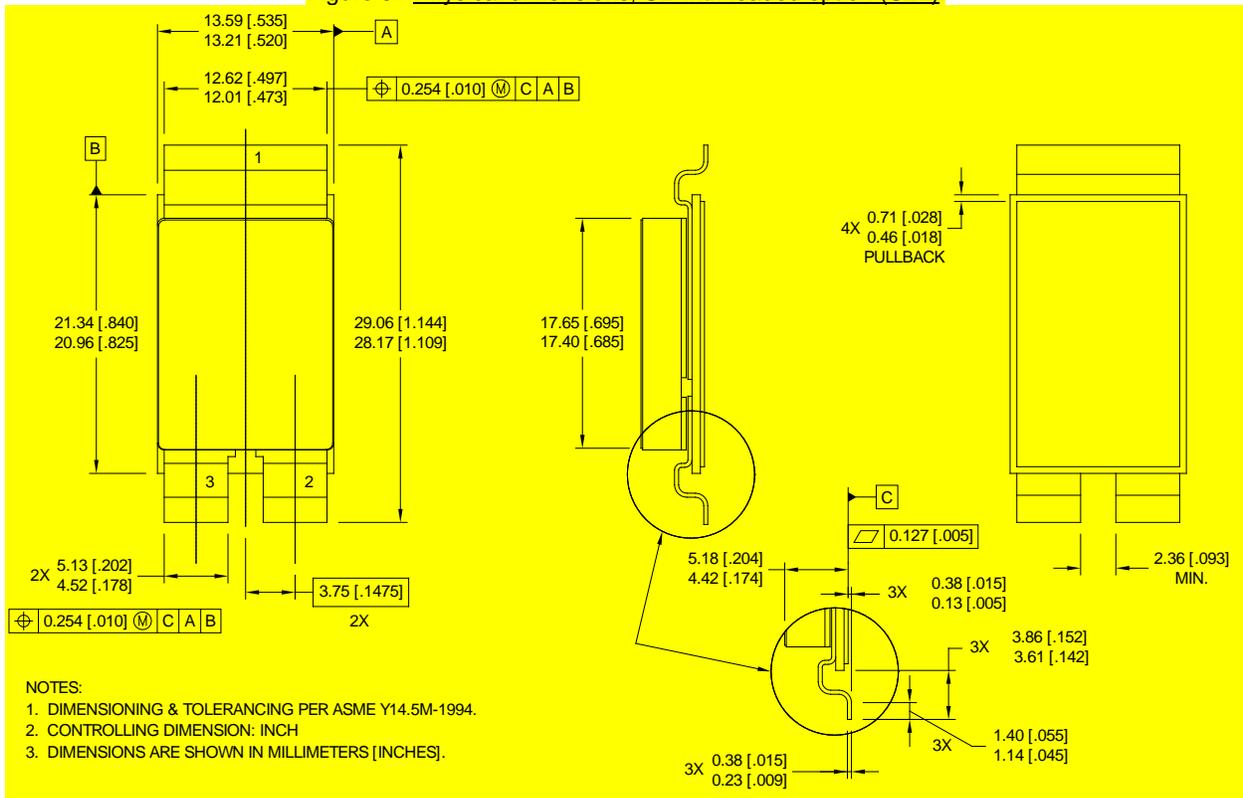


Figure 3. Physical dimensions, U2 with carrier board option (U2S).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 and 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 and 4 of this specification, whether or not they are listed.

2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-19500](#) – Semiconductor Devices, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

[MIL-STD-750](#) – Test Methods for Semiconductor Devices.

(Copies of these documents are available online at <http://quicksearch.dla.mil/>.)

2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 General. The individual item requirements shall be as specified in MIL-PRF-19500 and as modified herein.

3.2 Qualification. Devices furnished under this specification shall be products that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturer's list (QML) before contract award (see 4.2 and 6.3).

3.3 Abbreviations, symbols, and definitions. Abbreviations, symbols, and definitions used herein shall be as specified in MIL-PRF-19500.

3.4 Interface and physical dimensions. The interface and physical dimensions shall be as specified in MIL-PRF-19500 and on figures 1 (T3, TO-254AA), 2 (U2, surface mount TO-276AC), and 3 (lead or carrier attach) herein.

3.4.1 Lead formation and finish. Lead finish shall be solderable in accordance with MIL-STD-750, MIL-PRF-19500 and herein. Where a choice of finish is desired, it shall be specified in the acquisition document (see 6.2). When lead formation is performed, as a minimum, the vendor shall perform 100 percent hermetic seal in accordance with screen 14 of MIL-PRF-19500 and 100 percent dc testing in accordance with table I, subgroup 2 herein.

3.4.2 Internal construction. Multiple chip construction shall not be permitted to meet the requirements of this specification.

3.4.3 Lead attach or Carrier package. Alternations to the device shall be performed on devices that have passed all screening and QCI required per MIL-PRF-19500 and listed herein. When leads or carrier attach is added to the US package, as a minimum, the vendor shall perform the tests specified in 4.3.5 herein.

3.5 Electrostatic discharge protection. The devices covered by this specification require electrostatic discharge protection.

3.5.1 Handling. MOS devices shall be handled with certain precautions to avoid damage due to the accumulation of static charge. However, the following handling practices are recommended (see 3.5).

- a. Devices should be handled on benches with conductive handling devices.
- b. Ground test equipment, tools, and personnel handling devices.
- c. Do not handle devices by the leads.
- d. Store devices in conductive foam or carriers.
- e. Avoid use of plastic, rubber, or silk in MOS areas.
- f. Maintain relative humidity above 50 percent if practical.
- g. Care should be exercised during test and troubleshooting to apply not more than maximum rated voltage to any lead.
- h. Gate shall be terminated to source, $R \leq 100 \text{ k}\Omega$, whenever bias voltage is to be applied drain to source.

3.6 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.7 Electrical test requirements. The electrical test requirements shall be as specified in table I.

3.8 Marking. Marking shall be in accordance with MIL-PRF-19500. At the option of the manufacturer, marking may be omitted from the body, but shall be retained on the initial container. Devices that have been altered with lead or carrier attached per the specification herein shall have the altered part number on the device or on the device packaging.

3.9 Workmanship. Semiconductor devices shall be processed in such a manner as to be uniform in quality and shall be free from other defects that will affect life, serviceability, or appearance.

4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Screening (see 4.3).
- c. Conformance inspection (see 4.4 and table I and II).

4.2 Qualification inspection. Qualification inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.2.1 Group E qualification. Group E inspection shall be performed for qualification or re-qualification only. In case qualification was awarded to a prior revision of the specification sheet that did not request the performance of [table III](#) tests, the tests specified in [table III](#) herein that were not performed in the prior revision shall be performed on the first inspection lot of this revision to maintain qualification.

* 4.2.1.1 Single event effects (SEE). SEE shall be performed at initial qualification and after process or design changes which may affect radiation hardness (see [table III](#) and [table IV](#)). Upon qualification, manufacturers shall provide the verification test conditions from section 5 of method 1080 of MIL-STD-750 that were used to qualify the device for inclusion into section 6 of the slash sheet. End-point measurements shall be in accordance with [table II](#). SEE characterization data shall be made available upon request of the qualifying or acquiring activity.

* 4.2.1.2 Lead or carrier attach. For devices that include a lead or carrier attach package configuration qualification shall be performed in accordance with [table IV](#) herein, at initial qualification and after process or design changes.

4.3 Screening (JANS and JANTXV levels only). Screening shall be in accordance with table E-IV of MIL-PRF-19500 and as specified herein. The following measurements shall be made in accordance with table I herein. Devices that exceed the limits of table I herein shall not be acceptable.

Screen (see table E-IV of MIL-PRF-19500) (1) (2)	Measurement	
	JANS level	JANTXV level
(3)	Gate stress test (see 4.3.1)	Gate stress test (see 4.3.1)
(3)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)	Method 3470 of MIL-STD-750, E _{AS} (see 4.3.2)
(3) 3c	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)	Method 3161 of MIL-STD-750, thermal impedance (see 4.3.3)
9	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1}	Not applicable
10	Method 1042 of MIL-STD-750, test condition B	Method 1042 of MIL-STD-750, test condition B
11	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1} ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater.	Subgroup 2 of table I herein; I _{GSSF1} , I _{GSSR1} , I _{DSS1} , r _{DS(on)1} , V _{GS(TH)1}
12	Method 1042 of MIL-STD-750, test condition A	Method 1042 of MIL-STD-750, test condition A
13	Subgroups 2 and 3 of table I herein; ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.	Subgroup 2 of table I herein; ΔI _{GSSF1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{GSSR1} = ±20 nA dc or ±100 percent of initial value, whichever is greater. ΔI _{DSS1} = ±10 μA dc or ±100 percent of initial value, whichever is greater. Δr _{DS(on)1} = ±20 percent of initial value. ΔV _{GS(TH)1} = ±20 percent of initial value.
17	For TO-254 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein	For TO-254 packages: Method 1081 of MIL-STD-750 (see 4.3.4), Endpoints: Subgroup 2 of table I herein

- (1) At the end of the test program, I_{GSSF1}, I_{GSSR1}, and I_{DSS1} are measured.
- (2) An out-of-family program to characterize I_{GSSF1}, I_{GSSR1}, I_{DSS1}, and V_{GS(th)1} shall be invoked.
- (3) Shall be performed anytime after temperature cycling, screen 3a; JANTX and JANTXV levels do not need to be repeated in screening requirements.

4.3.1 Gate stress test. Apply $V_{GS} = 24$ V, minimum for $t = 250$ μ s, minimum.

4.3.2 Single pulse avalanche energy (E_{AS}).

- a. Peak current $I_{AS} = I_{D1}$.
- b. Inductance $L = \left[\frac{2E_{AS}}{(I_{D1})^2} \right] \left[\frac{V_{BR} - V_{DD}}{V_{BR}} \right]$ mH minimum.
- c. Gate to source resistor R_{GS} $25 \Omega \leq R_{GS} \leq 200 \Omega$.
- d. Supply voltage $V_{DD} \leq 30$ V dc.
- e. Initial case temperature $T_C = +25^\circ$ C, -5° C, $+10^\circ$ C.
- f. Gate voltage $V_{GS} = 12$ V dc.
- g. Number of pulses to be applied 1 pulse minimum.

4.3.3 Thermal impedance. The thermal impedance measurements shall be performed in accordance with method 3161 of MIL-STD-750 using the guidelines in that method for determining I_M , I_H , t_H , t_{SW} , (and V_H where appropriate). Measurement delay time (t_{MD}) = 70 μ s max. See [table III](#), group E, subgroup 4 herein.

4.3.4 Dielectric withstanding voltage.

- a. Magnitude of test voltage 900 V dc.
- b. Duration of application of test voltage 15 seconds (min).
- c. Points of application of test voltage All leads to case (bunch connection).
- d. Method of connection Mechanical.
- e. Kilovolt-ampere rating of high voltage source 1,200 V/1.0 mA (min).
- f. Maximum leakage current 1.0 mA.
- g. Voltage ramp up time 500 V/second

* 4.3.5 Lead or carrier attach screening (All quality levels). All surface mount devices with added leads or carrier boards shall be screened as specified herein.

Screen	MIL-STD-750 Method	Conditions
1. Hermetic Seal 1/ a. Fine Leak b. Gross Leak	1071	
2. Thermal Response (see 4.3.3) A2 dc Electrical 2/ 3/	3161	Read and Record.
3. X-Radiography	2076	The solder material coverage at the package lead pad/SMD carrier sub interfaces shall be 85% minimum
4. External Visual Examination	2071	Cracks or separation of materials shall not be evident on any device after the SMD lead attach assembly operation. Pad and Isolation areas shall be free from foreign matter and extraneous solder. Solder fillet coverage at the lead/package lead pad interfaces, along all visible sides, minimum of 75% solder fillet coverage.
5a. Physical dimensions	2066	6 piece sample, each device shall meet the requirements specified in figure 3.
5b. Terminal Strength	2036	3 piece sample.

1/ Evaluation of surface sorption in accordance with method 1071 shall be performed.

2/ Only DC electrical test specified herein.

4.4 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-19500 and as specified herein.

4.4.1 Group A inspection. Group A inspection shall be conducted in accordance with table E-V of MIL-PRF-19500 and [table I](#) herein.

* 4.4.2 Group B inspection. Group B inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VIA (JANS) and table E-VIB (JANTXV) of MIL-PRF-19500, and as follows.

4.4.2.1 Group B inspection, table E-VIA (JANS) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B3	1051	Test condition G, 100 cycles.
B3	2077	Scanning electron microscope (SEM) qualification may be performed anytime prior to lot formation.
B4	1042	Condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.
B5	1042	Accelerated steady-state gate bias, condition B, $V_{GS} =$ rated; $T_A = +175^{\circ}\text{C}$, $t = 24$ hours minimum; or $T_A = +150^{\circ}\text{C}$, $t = 48$ hours minimum.
B5	1042	Accelerated steady-state reverse bias, condition A, $V_{DS} =$ rated; $T_A = +175^{\circ}\text{C}$, $t = 120$ hours minimum; or $T_A = +150^{\circ}\text{C}$, $t = 240$ hours minimum.

4.4.2.2 Group B inspection, table E-VIB (JANTXV) of MIL-PRF-19500.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
B3	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

- * 4.4.3 Group C inspection. Group C inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-VII of MIL-PRF-19500 and as follows.

<u>Subgroup</u>	<u>Method</u>	<u>Condition</u>
B2	1051	Test condition G, 25 cycles.
C2	2036	Test condition A; weight = 10 pounds; $t = 15$ s. (Not applicable to U2).
C5	3161	Thermal resistance, see 4.3.3, $R_{\theta JC(max)} = 0.60$ °C/W (T1) or 0.50 °C/W (U2).
C6	1042	Intermittent operation life, condition D. No heat sink or forced-air cooling on the device shall be permitted during the on cycle. $t_{on} = 30$ seconds minimum.

4.4.4 Group D inspection. Group D inspection shall be conducted in accordance with table E-VIII of MIL-PRF-19500 and [table II](#) herein.

4.4.5 Group E inspection. Group E inspection shall be conducted in accordance with the conditions specified for subgroup testing in table E-IX of MIL-PRF-19500 and as specified in [table III](#) herein. Electrical measurements (end-points) shall be in accordance with [table I](#), subgroup 2 herein.

4.5 Methods of inspection. Methods of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Pulse measurements. Conditions for pulse measurement shall be as specified in section 4 of MIL-STD-750.

*

TABLE I. Group A inspection.

Inspection 1/	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 1</u>						
Visual and mechanical inspection	2071					
<u>Subgroup 2</u>						
Thermal impedance 2/	3161	See 4.3.3	Z _{θJC}			°C/W
Breakdown voltage, drain to source 2N7523T1 and U2 2N7524T1 and U2	3407	V _{GS} = 0 V dc, I _D = -1 mA dc, bias condition C	V(BR)DSS	-30 -60		V dc V dc
Gate to source voltage (threshold)	3403	V _{DS} ≥ V _{GS} , I _D = -1 mA dc	V _{GS} (TH)1	-2.0	-4.0	V dc
Gate reverse current	3411	V _{GS} = +20 V dc, bias condition C, V _{DS} = 0	I _{GSS} F1		+100	nA dc
Gate reverse current	3411	V _{GS} = -20 V dc, bias condition C, V _{DS} = 0	I _{GSS} R1		-100	nA dc
Drain current	3413	V _{GS} = 0 V dc, bias condition C, V _{DS} = 80 percent of rated V _{DS}	I _{DSS} 1		-10	μA dc
Static drain to source on-state resistance 2N7523T1 2N7523U2 2N7524T1 2N7524U2	3421	V _{GS} = -12 V dc, condition A, pulsed (see 4.5.1), I _D = I _{D2}	r _{DS(on)} 1		0.014 0.013 0.017 0.016	Ω Ω Ω Ω
* Forward voltage	4011	Condition A, I _D = I _{D1} , V _{GS} = 0 V dc	V _{SD}		-5.0	V
<u>Subgroup 3</u>						
High-temperature operation:	3411	T _C = T _J = +125°C				
Gate reverse current	3413	V _{GS} = -20 V dc and +20 V dc, bias condition C, V _{DS} = 0	I _{GSS} 2		± 200	nA dc
Drain current	3413	V _{GS} = 0 V dc, bias condition C, V _{DS} = 80 percent of rated V _{DS}	I _{DSS} 2		-25	μA dc

See footnotes at end of table.

*

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 3</u> - continued						
High-temperature operation:		$T_C = T_J = +125^\circ\text{C}$				
Static drain to source on-state resistance	3421	$V_{GS} = -12\text{ V dc}$, pulsed (see 4.5.1), $I_D = I_{D2}$	$r_{DS(on)3}$			
2N7523T1					0.015	Ω
2N7523U2					0.014	Ω
2N7524T1					0.026	Ω
2N7524U2					0.024	Ω
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -1\text{ mA dc}$	$V_{GS(th)2}$	-1.0		V dc
Low-temperature operation:		$T_C = T_J = -55^\circ\text{C}$				
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$, $I_D = -1\text{ mA dc}$	$V_{GS(th)3}$		-5.0	V dc
<u>Subgroup 4</u>						
Forward transconductance	3475	$I_D = \text{rated } I_{D2}$, $V_{DD} = -15\text{ V}$ (see 4.5.1)	gFS			
2N7523T1 & 2N7524T1				39		S
2N7523U2 & 2N7524U2				40		S
Switching time test	3472	$I_D = \text{rated } I_{D1}$, $V_{GS} = -12\text{ V dc}$, $R_G = 2.35\ \Omega$ (U2), $V_{DD} = 50$ percent of rated V_{DS}				
Turn-on delay time			$t_{d(on)}$		35	ns
Rise time			t_r			
2N7523T1-U2					175	ns
2N7524T1-U2					150	ns
Turn-off delay time			$t_{d(off)}$		100	ns
Fall time			t_f			
2N7523T1-U2					80	ns
2N7524T1-U2					35	ns

See footnotes at end of table.

TABLE I. Group A inspection - Continued.

Inspection <u>1/</u>	MIL-STD-750		Symbol	Limits		Unit
	Method	Conditions		Min	Max	
<u>Subgroup 5</u>						
Safe operating area test (high voltage)	3474	See figure 6 ; $t_p = 10 \text{ ms}$, $V_{DS} = 80 \text{ percent of rated } V_{DS}$				
Electrical measurements		See table I , subgroup 2 herein.				
<u>Subgroup 6</u>						
Not applicable						
<u>Subgroup 7</u>						
Gate charge	3471	Condition B	Q _{G(on)}			
2N7523T1					160	nC
2N7523U2					240	nC
2N7524T1					160	nC
2N7524U2					200	nC
On-state gate charge			Q _{GS}			
2N7523T1					60	nC
2N7523U2					60	nC
2N7524T1					60	nC
2N7524U2					65	nC
Gate to drain charge			Q _{GD}			
2N7523T1					65	nC
2N7523U2					55	nC
2N7524T1					65	nC
2N7524U2					60	nC
Reverse recovery time	3473	$di/dt \leq 100A/\mu s$, $I_D = I_{D1}$, $V_{DD} \leq \text{Rated } V_{DS}$	t_{rr}			
2N7523T1					150	ns
2N7523U2					140	ns
2N7524T1					110	ns
2N7524U2					200	ns

1/ For sampling plan, see MIL-PRF-19500.

2/ This test required for the following end-point measurements only:

- Group B, subgroups 3 and 4 (JANS).
- Group B, subgroups 2 and 3 (JANTXV).
- Group C, subgroup 2 and 6.
- Group E, subgroup 1.

TABLE II. Group D inspection.

Inspection 1/ 2/ 3/	MIL-STD-750		Symbo l	Pre-Irradiation limits		Post- Irradiation limits		Post- Irradiation limits		Unit
	Metho d	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
<u>Subgroup 1</u>										
Not applicable										
<u>Subgroup 2</u>		$T_C = +25^\circ\text{C}$								
Steady-state total dose irradiation (V_{GS} bias) 4/	1019	$V_{GS} = -12\text{V}$ $V_{DS} = 0$								
Steady-state total dose irradiation (V_{DS} bias) 4/	1019	$V_{GS} = 0$ $V_{DS} = 80$ percent of rated V_{DS} (pre- irradiation)								
End-point electricals:										
Breakdown voltage, drain to source	3407	$V_{GS} = 0$ $I_D = -1\text{ mA}$ bias cond. C	$V_{(BR)DS}$							
2N7523T1 and U2				-30		-30		-30		V dc
2N7524T1 and U2				-60		-60		-60		V dc
Gate to source voltage (threshold)	3403	$V_{DS} \geq V_{GS}$	$V_{GS(th)1}$	-2.0	-4.0	-2.0	-4.0	-2.0	-5.0	V dc
Gate reverse current	3411	$V_{GS} = -20\text{ V}$ $V_{DS} = 0$ bias cond. C	I_{GSSR1}		-100		-100		-100	nA dc
Gate forward current	3411	$V_{GS} = 20\text{ V}$ $V_{DS} = 0$ bias cond. C	I_{GSSF1}		100		100		100	nA dc
Drain current	3413	$V_{GS} = 0$ bias cond. C $V_{DS} = 80$ percent of rated V_{DS} (pre- irradiation)	I_{DSS1}		-10		-10		-10	μA dc

See footnotes at end of table.

TABLE II. Group D inspection - Continued.

Inspection <u>1/</u> <u>2/</u> <u>3/</u>	MIL-STD-750		Symbo l	Pre-Irradiation limits		Post-Irradiation limits		Post-Irradiation limits		Unit
	Metho d	Conditions		R, F		R		F		
				Min	Max	Min	Max	Min	Max	
Static drain to source on- state voltage	3405	$V_{GS} = -12$ V cond. A pulsed (see 4.5.1) $I_D = I_{D2}$	$V_{DS(on)1}$							
2N7523T1					0.630		0.630		0.630	V dc
2N7523U2					0.784		0.784		0.784	V dc
2N7524T1					0.765		0.765		0.765	V dc
2N7524U2					0.952		0.952		0.952	V dc
Forward voltage source to drain diode	4011	$V_{GS} = 0$, cond. A, $I_D = I_{D1}$	V_{SD}		-5.0		-5.0		-5.0	V dc

1/ For sampling plan, see MIL-PRF-19500.

2/ Group D qualification may be performed anytime prior to lot formation. Wafers qualified to these group D QCI requirements may be used for any other specification sheet utilizing the same die design.

3/ At the manufacturer's option, group D samples need not be subjected to the screening tests, and may be assembled in it's qualified package or in any qualified package that the manufacturer has data to correlate the performance to the designated package.

4/ Separate samples shall be pulled for each bias.

* TABLE III. Group E inspection (all quality levels) for qualification or re-qualification only.

Inspection	MIL-STD-750		Sample plan
	Method	Conditions	
<u>Subgroup 1</u>			45 devices c = 0
Temperature cycling	1051	Test condition G, 500 cycles.	
Hermetic seal Fine leak Gross leak	1071		
Electrical measurements		See table 1 , subgroup 2.	
<u>Subgroup 2</u> ^{1/}			45 devices c = 0
Steady state reverse bias	1042	Test condition A; 1,000 hours.	
Electrical measurements		See table 1 , subgroup 2.	
Steady-state gate bias	1042	Test condition B; 1,000 hours.	
Electrical measurements		See table 1 , subgroup 2.	
<u>Subgroup 4</u>			Sample size N/A
Thermal impedance curves		See MIL-PRF-19500.	
<u>Subgroup 10</u>			22 devices c = 0
Commutating diode for safe operating area test procedure for measuring dv/dt during reverse recovery of power MOSFET transistors or insulated gate bipolar transistors	3476	Test conditions shall be derived by the manufacturer.	
<u>Subgroup 11</u>			3 devices
SEE ^{2/} ^{3/}	1080	See method 1080 of MIL-STD-750 .	

^{1/} A separate sample for each test shall be pulled.

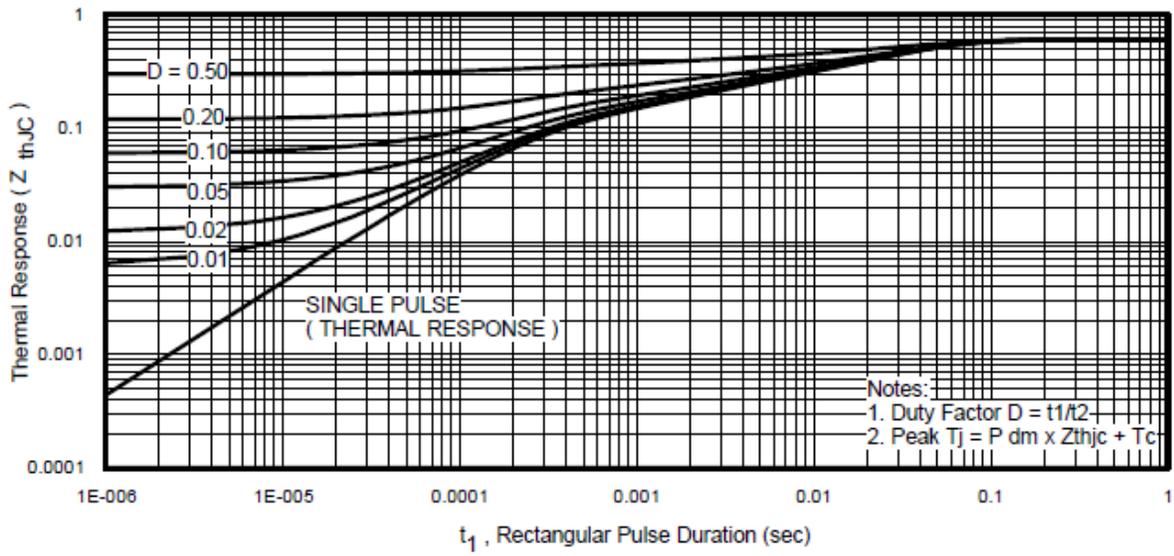
^{2/} Group E qualification of testing may be performed prior to lot formation. Qualification may be extended to other specification sheets utilizing the same structurally identical die design.

^{3/} The sampling plan applies to each bias condition.

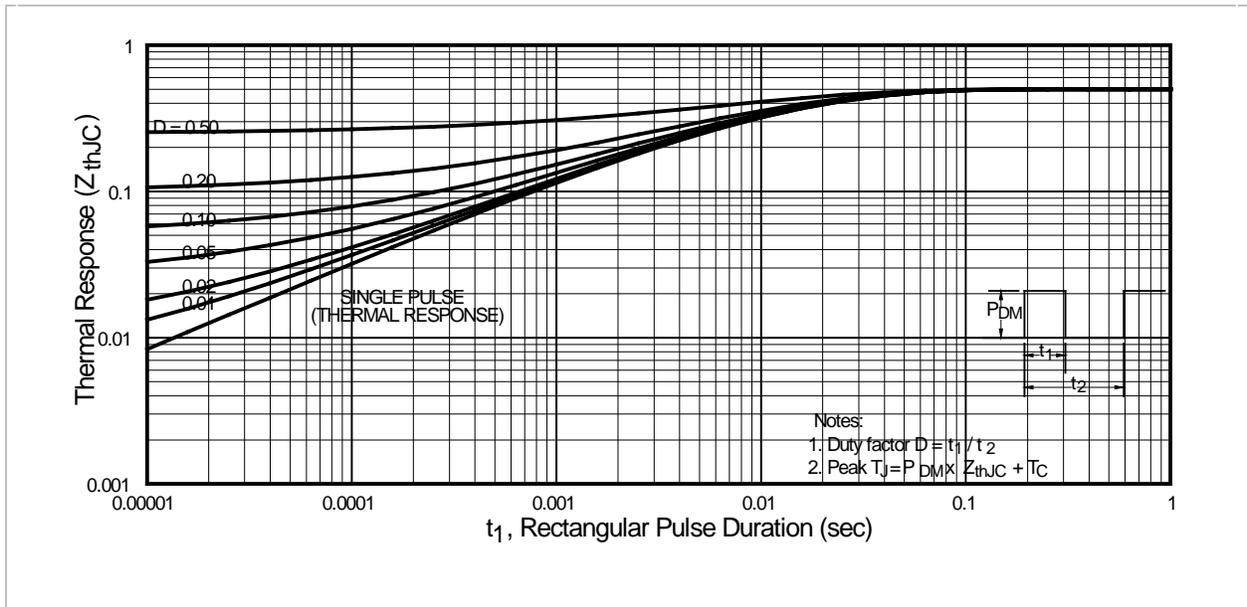
TABLE IV. Lead alternation Qualification inspection requirements.

Inspections ^{1/}	MIL-STD-750		Sample size
	Method	Conditions	
<u>Subgroup 1</u>			6 devices
Temperature Cycle	1051	100 Temp Cycles, test condition G or maximum storage temperature.	
Hermetic Seal	1071		
Fine Leak			
Gross Leak			
A2 dc Electrical		Read and record.	
Thermal Response	3161		
External Visual Examination	2071	Cracks or separation of materials shall not be evident on test samples.	
<u>Subgroup 2</u>			6 devices
Intermittent Operating Life	1042	Condition D; 6,000 cycles.	
A2 dc Electrical		Read and Record.	
Thermal Response	3161		
External Visual Examination	2071	Cracks or separation of materials shall not be evident on test samples.	
<u>Subgroup 3</u>			6 devices
Terminal Strength	2036	Tension; Condition A 10lbs for 10 seconds Fatigue; Condition E 3 arcs of 90 +/- 5 degrees each 8.0 oz.	
A2 dc Electrical		Read and Record.	
External Visual Examination	2071	Cracks or separation of materials shall not be evident on test samples.	

^{1/} Qualification samples performed on non-formed leaded devices.



2N7523T1 and 2N7524T1



2N7523U2 & 2N7524U2

FIGURE 4. Thermal impedance curves.

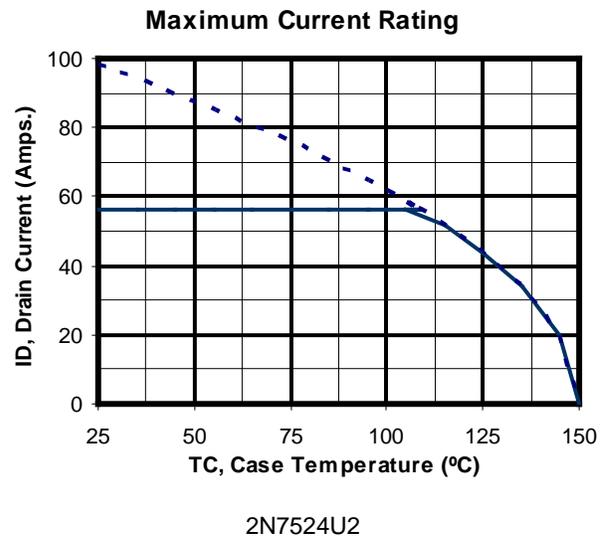
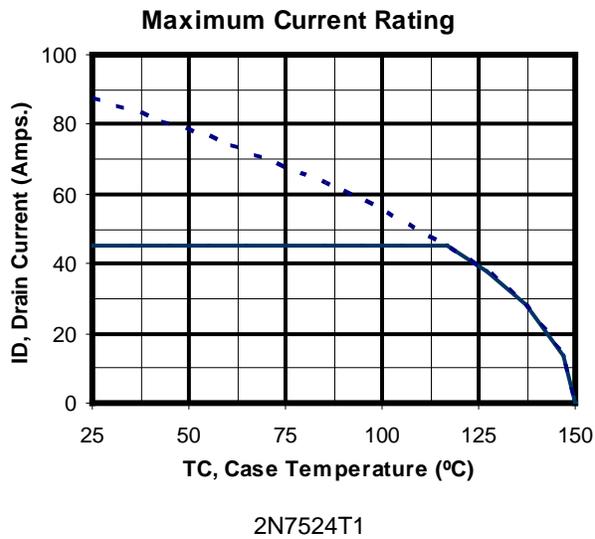
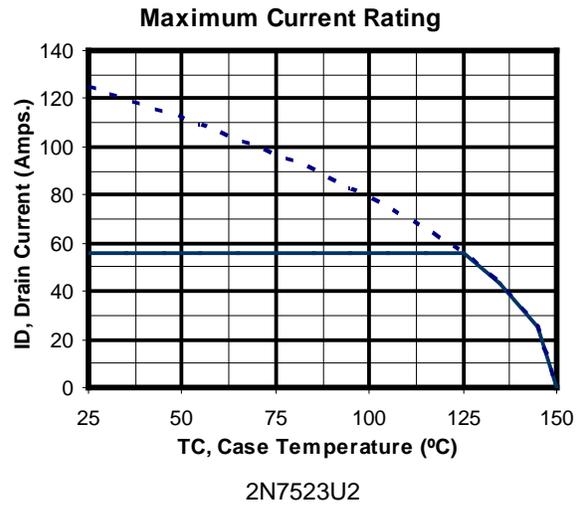
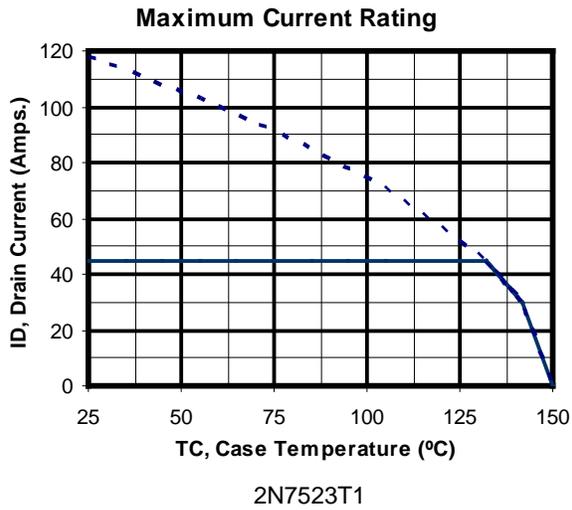


FIGURE 5. Maximum drain current vs case temperature graphs.

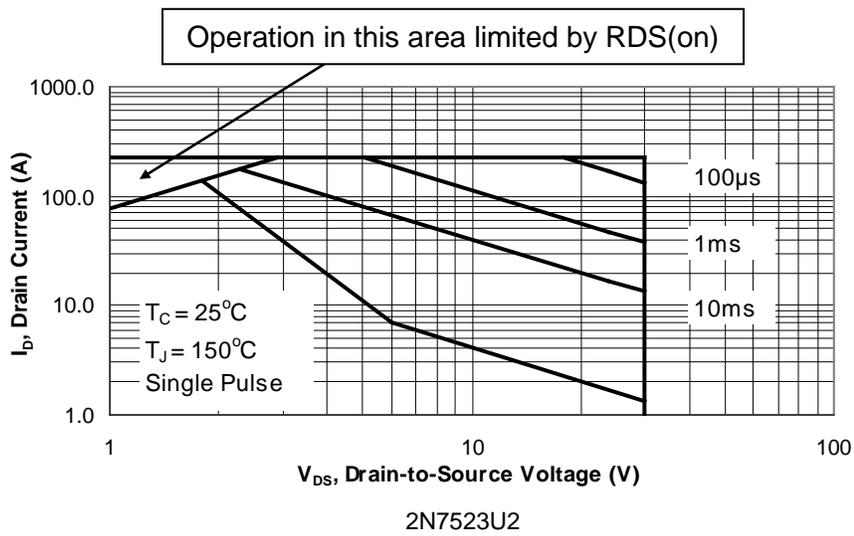
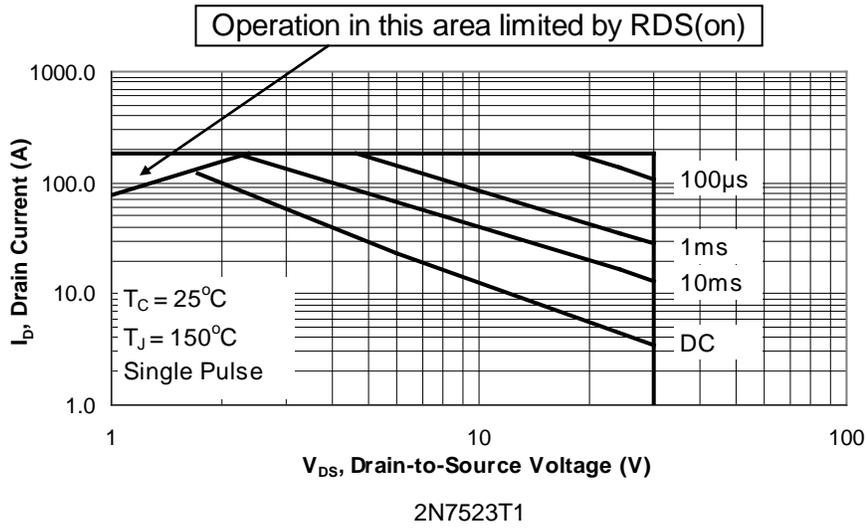


FIGURE 6. Safe operating area graphs.

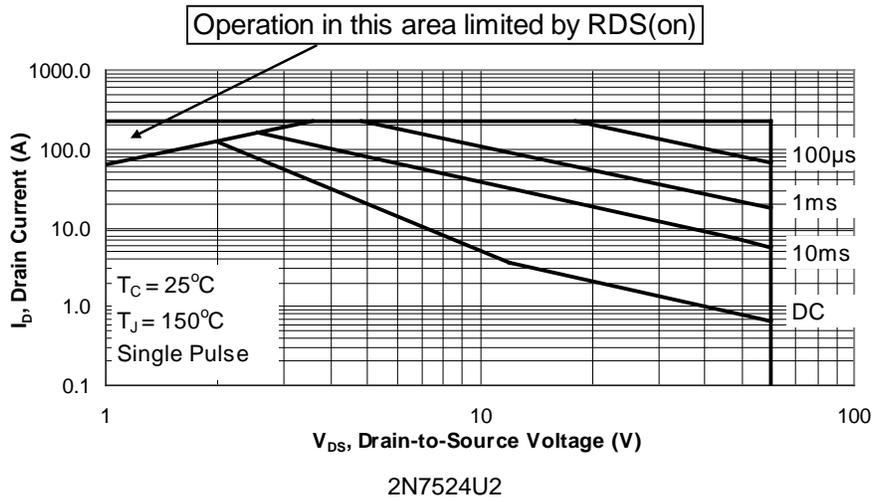
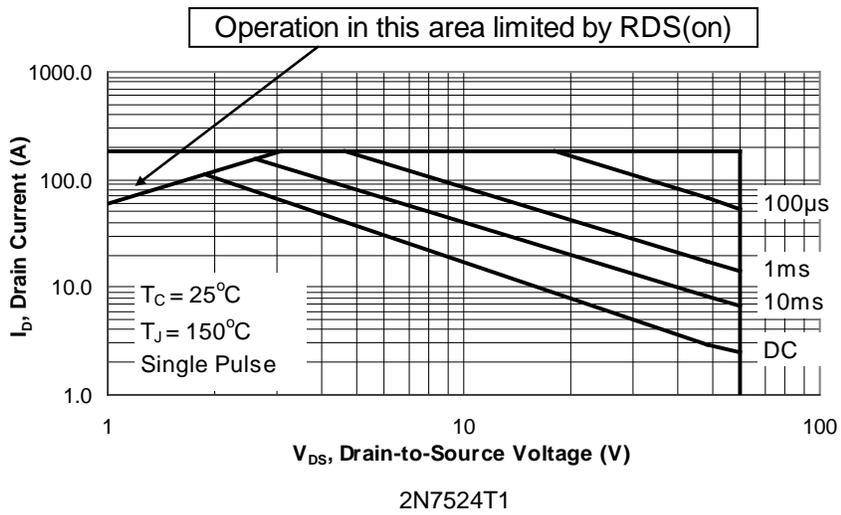


FIGURE 6. Safe operating area graphs - Continued.

5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory. The notes specified in MIL-PRF-19500 are applicable to this specification.)

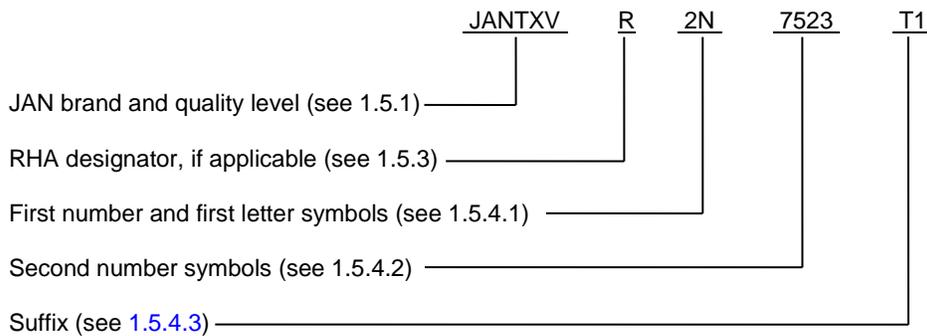
6.1 Intended use. Semiconductors conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, and date of this specification.
- b. Packaging requirements (see 5.1).
- c. Lead formation and finish (see 3.4.1).
- d. Product assurance level and type designator.
- e. For acquisition of RHA designated devices, [table II](#), subgroup 1 testing of group D herein is optional. If subgroup 1 is desired, it should be specified in the contract.
- f. If specific SEE characterization conditions are desired (see section 6.8 and [table IV](#)), manufacturer's cage code should be specified in the contract or order.
- g. If SEE testing data is desired, it should be specified in the contract or order.
- h. If the leaded or carrier board configuration is desired for U2 devices (see 3.4.3), it should be specified in the contract. For acquisition of U2 devices, the default configuration is delivered without the carrier board.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML 19500) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail vqe.chief@dla.mil. An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://assist.dla.mil>.

- * 6.4 PIN construction example. The PINs for encapsulated devices are construction using the following form.



- * 6.5 List of PINs. The following is a list of possible PINs available on this specification sheet.

PINs for devices of the "TXV" quality level	PINs for devices of the "TXV" quality level with RHA (1)	PINs for devices of the "S" quality level	PINs for devices of the "S" quality level with RHA (1)
JANTXV2N7523T1	JANTXV#2N7523T1	JANS2N7523T1	JANS#2N7523T1
JANTXV2N7523U2	JANTXV#2N7523U2	JANS2N7523U2	JANS#2N7523U2
JANTXV2N7523U2L	JANTXV#2N7523U2L	JANS2N7523U2L	JANS#2N7523U2L
JANTXV2N7523U2S	JANTXV#2N7523U2S	JANS2N7523U2S	JANS#2N7523U2S
JANTXV2N7524T1	JANTXV#2N7524T1	JANS2N7524T1	JANS#2N7524T1
JANTXV2N7524U2	JANTXV#2N7524U2	JANS2N7524U2	JANS#2N7524U2
JANTXV2N7524U2L	JANTXV#2N7524U2L	JANS2N7524U2L	JANS#2N7524U2L
JANTXV2N7524U2S	JANTXV#2N7524U2S	JANS2N7524U2S	JANS#2N7524U2S

(1) The number sign (#) represent one of five RHA designators available (M, D, P, L, or R).

- * 6.6 Cross-reference list. The following table shows the generic P/N and its associated military P/N (without JAN and RHA prefix). Devices covered by this specification are substitutable for the manufacturer's and user's Part or Identifying Number (PIN). This information in no way implies that manufacturer's PIN's are suitable for the military PIN.

Preferred types (military PIN)	Commercial PIN	
	TO-254AA	TO-276AC (SMD2)
2N7523T1	IRHMS59_Z60	
2N7523U2		IRHNA59_Z60
2N7524T1	IRHMS59_064	
2N7524U2		IRHNA59_064

6.7 JANC die versions. The JANHC and JANKC die versions of these devices are covered under specification sheet [MIL-PRF-19500/741](#).

6.8 Application data.

6.8.1 Manufacturer specific irradiation data. Each manufacturer qualified to this slash sheet has characterized its devices to the requirements of MIL-STD-750 method 1080 and as specified herein. Since each manufacturer's characterization conditions can be different and can vary by the version of method 1080 qualified to, the MIL-STD-750 method 1080 revision version date and conditions used by each manufacturer for characterization have

been listed here (see [table IV](#)) for information only. SEE conditions and figures listed in section 6 are current as of the date of this specification sheet, please contact the manufacturer for the most recent conditions.

TABLE IV. Manufacturers characterization conditions.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE <u>1/</u>	1080	See MIL-STD-750 method 1080	3 devices
	Electrical Measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table 1 , subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² , Flux = $2E3$ to $2E4$ ions/cm ² /sec, Temperature = 25 ± 5 °C Surface LET = $38 \text{ MeV}\cdot\text{cm}^2/\text{mg} \pm 5\%$, range = $35 \mu\text{m} \pm 7.5\%$, energy = $270 \text{ MeV} \pm 7.5\%$	
	2N7523T1, 2N7523U2		In situ bias conditions: $V_{DS} = -3$ (nominal 3.42 MeV/nucleon at Texas A & M Cyclotron)	
	2N7524T1, 2N7524U2		In situ bias conditions: $V_{DS} = -6$ (nominal 3.86 MeV/nucleon at Brookhaven National Lab Accelerator) Surface LET = $61 \text{ MeV}\cdot\text{cm}^2/\text{mg} \pm 5\%$, range = $31 \mu\text{m} \pm 10\%$, energy = $330 \text{ MeV} \pm 7.5\%$	
	2N7523T1, 2N7523U2		In situ bias conditions: $V_{DS} = -3$ $V_{DS} = -25 \text{ V}$ and $V_{GS} = 20 \text{ V}$ (nominal 2.53 MeV/nucleon at Texas A & M Cyclotron)	
2N7524T1, 2N7524U2		In situ bias conditions: $V_{DS} = -6$ $V_{DS} = -45 \text{ V}$ and $V_{GS} = 15 \text{ V}$ $V_{DS} = -25 \text{ V}$ and $V_{GS} = 20 \text{ V}$ (nominal 2.92 MeV/nucleon at Brookhaven National Lab Accelerator)		

See footnotes at end of table.

Table IV. Manufacturers characterization conditions – Continued.

Manufacturers CAGE	Inspection	MIL-STD-750		Sample plan
		Method	Conditions	
69210 (Applicable to devices with a date code of September 2009 and older)	SEE 1/	1080	See MIL-STD-750 method 1080	3 devices
	Electrical measurements		I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2	
	SEE irradiation:		Fluence = $3E5 \pm 20$ percent ions/cm ² , Flux = 2E3 to 2E4 ions/cm ² /sec, Temperature = 25 ± 5 °C	
	2N7523T1, 2N7523U2		In situ bias conditions: $V_{DS} = -3$ $V_{DS} = -25$ V and $V_{GS} = 15$ V (nominal 1.74 MeV/nucleon at Texas A & M Cyclotron)	
	2N7524T1, 2N7524U2		In situ bias conditions: $V_{DS} = -6$ (nominal 1.98 MeV/nucleon at Brookhaven National Lab Accelerator)	
Electrical measurements	I_{GSSF1} , I_{GSSR1} , and I_{DSS1} in accordance with table I, subgroup 2			
<div style="border: 1px solid black; padding: 5px; width: fit-content; margin: 0 auto;"> Upon qualification, all manufacturers will provide the verification test conditions to be added to this table. </div>				

1/ I_{GSSF1} , I_{GSSR1} , and I_{DSS1} was examined before and following SEE irradiation to determine acceptability for each bias conditions. Other test conditions in accordance with table I, subgroup 2, may be performed at the manufacturer's option.

6.9 Changes from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the previous issue.

Custodians:
Army - CR
Navy - EC
Air Force - 85
NASA - NA
DLA - CC

Preparing activity:
DLA - CC

(Project 5961-2015-033)

Review Activity:
Army - MI

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil/>.