

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make change to VTHUV test specified under table I. - ro	00-03-07	R. MONNIN
B	Add device type 02. - ro	01-07-26	R. MONNIN
C	Make changes to I _{LK} and +I _{IN} tests as specified in table I. - ro	01-12-14	R. MONNIN
D	Make change to the high side floating supply offset voltage limit for device type 02 as specified under 1.4. - ro	02-04-17	R. MONNIN
E	Add a new logic diagram for device type 02. - ro	03-04-15	R. MONNIN
F	Make correction to the title block. Make clarification to footnote 7/ under paragraph 1.5. Add pin description to figure 1. Make changes to correct figure 3, irradiation circuit. - ro	11-01-19	C. SAFFLE
G	Make correction to figure 3, irradiation circuit. - ro	11-04-05	C. SAFFLE
H	Add device type 03, Table IB, paragraphs 4.4.4.3 and 6.7. Delete irradiation circuits. - ro	12-08-02	C. SAFFLE
J	Delete references to device class M requirements. Update document paragraphs to current MIL-PRF-38535 requirements. - ro	16-10-05	C. SAFFLE



REV																				
SHEET																				
REV	J	J	J	J	J	J	J	J												
SHEET	15	16	17	18	19	20	21	22												
REV STATUS OF SHEETS	REV			J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J	J
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY RICK OFFICER	DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990 http://www.landandmaritime.dla.mil																	
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY RAJESH PITHADIA																		
	APPROVED BY RAYMOND MONNIN	MICROCIRCUIT, DIGITAL-LINEAR, RADIATION HARDENED, HIGH FREQUENCY HALF BRIDGE DRIVER, MONOLITHIC SILICON																	
	DRAWING APPROVAL DATE 99-06-29																		
	REVISION LEVEL J		SIZE A	CAGE CODE 67268	5962-99536														
		SHEET 1 OF 22																	

1.3 Absolute maximum ratings. 1/ 2/

High side floating supply voltage (VB):	
Device type 01	-0.3 V to 120 V
Device types 02 and 03	-0.3 V to 150 V
High side floating supply offset voltage (VS)	VB – 25 V to VB + 0.3 V
High side floating output voltage (VHO)	VS – 0.3 V to VB + 0.3 V
Low side fixed supply voltage (VCC)	-0.3 V to 25 V
Low side output voltage (VLO)	COM – 0.3 V to VCC + 0.3 V
Logic supply voltage (VDD)	VCC 3/
Logic input voltage (HIN, LIN, and SD pins)	VSS – 0.3 V to VDD +0.3 V
VS slew rate (dVS / dt):	
Device type 01	10 V / ns maximum
Device types 02 and 03	15 V / ns maximum
COM (low driver return) offset to VSS :	
Device type 01	-7 V to +7 V
Device types 02 and 03	-5 V to +5 V
Maximum power dissipation (Pd) (TA ≤ +25°C)	1.6 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (Tj)	+175°C
Storage temperature range	-55°C to +150°C
Thermal resistance, junction-to-case (θJC)	18°C/W
Thermal resistance, junction-to-ambient (θJA)	90°C/W

1.4 Recommended operating conditions.

High side floating supply absolute voltage (VB)	VS + 12 V to VS +20 V
High side floating supply offset voltage (VS):	
Device type 01	-4 V to 100 V 4/
Device types 02 and 03	-4 V to 130 V 4/
High side floating output voltage (VHO)	VS to VB
Low side fixed supply (VCC)	12 V to 20 V
Low side output voltage (VLO)	COM to VCC
Logic supply voltage (VDD)	VCC 3/

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ All voltage parameters are absolute voltages referenced to VSS.
- 3/ Logic is operational for VS of -4 V but VB must remain minimum 12 V above VSS (ground).
- 4/ This device is recommended for VDD = VCC and they should be tied together at the board level. VDD and VCC can have different values but both must remain within 12 V – 20 V range. Low side undervoltage monitors VDD to VSS differential.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 3

1.4 Recommended operating conditions – continued.

Logic supply return (VSS)	0 V
COM (low driver return) offset to VSS	-5 V to 5 V <u>5/</u>
Logic input voltage (VIN)	VSS to VDD <u>6/</u>
Ambient operating temperature range (TA)	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 - 300 rads(Si)/s):

Device types 01 and 02 classes M, Q, or V	300 krads(Si) <u>7/</u>
Device type 01 class T	100 krads(Si) <u>7/</u>
Device type 03	300 krads(Si) <u>8/</u>

Maximum total dose available (dose rate ≤ 0.01 rads(Si)/s):

Device type 03	50 krads(Si) <u>8/</u>
----------------------	------------------------

Single event phenomenon (SEP) for device types 02 and 03:

Destructive single event effects (SEE):

No SEL observed at effective linear energy transfer (LET) (see 4.4.4.3)	≤ 90 MeV/(mg/cm ²) <u>9/</u>
No SEB observed at effective (LET) (fluence = 1.0 x 10 ⁷ ions/cm ²)	< 90 MeV/(mg/cm ²) <u>9/</u>

Nondestructive single event effects (SEE):

No SET observed at effective LET (fluence 4 x 10 ⁶ and pulse perturbation = 1)	< 90 MeV/(mg/cm ²) <u>9/</u>
--	--

5/ VCC / VDD to COM must remain in 12 V to 20 V range.

6/ The input buffers are designed to accept 5 V logic level inputs while running VDD in 12 V – 20 V range.

7/ Device types 01 and 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si) for device classes V, Q, or M and 100 krads(Si) for device class T.

8/ Device type 03 radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300 krads(Si), and condition D to a maximum total dose of 50 krads(Si).

9/ Limits are characterized at initial qualification and after any design or process changes which may affect the SEP/SEE characteristics but are not production tested unless specified by the customer through the purchase order or contract. For more information on destructive SEE (SEB/SEGR) test results customers are requested to contact manufacturer.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 4

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at <http://www.astm.org> or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q, T and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q, T and V.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 5

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroup	Device type	Limits		Unit
					Min	Max	
Logic "1" input voltage	V _{IH}	<u>2/</u>	1,2,3	01,02, 03	3		V
Logic "0" input voltage	V _{IL}	<u>2/</u>	1,2,3	01,02, 03		0.8	V
High level output voltage	V _{OH}	I _{OUT} = 0 mA <u>2/</u> V _{BIAS} - V _{OH}	1,2,3	01,02, 03		0.1	V
Low level output voltage	V _{OL}	I _{OUT} = 0 mA <u>2/</u>	1,2,3	01,02, 03		0.1	V
Offset supply leakage current	I _{LK}	V _B = V _S = 100 V <u>2/</u>	1,2,3	01		50	μA
		V _B = V _S = 150 V <u>2/</u>		02,03		500	
Quiescent V _B supply current	I _{QB}	V _{IN} = 0 V or V _{DD} <u>2/</u>	1,2,3	01,02, 03		500	μA
Quiescent V _{CC} supply current	I _{QCC}	V _{IN} = 0 V or V _{DD} <u>2/</u>	1,2,3	01,02, 03		50	μA
Quiescent V _{DD} supply current (inputs low)	I _{QDD}	All inputs 0 V <u>2/</u>	1,2,3	01,02, 03		2900	μA
Logic "1" input bias current	+I _{IN}	V _{IN} = V _{DD} <u>2/</u>	1,2,3	01		60	μA
		V _{IN} = V _{DD} <u>2/</u>		02,03		75	
Logic "0" input bias current	-I _{IN}	V _{IN} = 0 V <u>2/</u>	1,2,3	01,02, 03	-10		μA
V _{DD} / V _{SS} under-voltage lockout threshold	V _{THUV}	<u>2/</u>	1,2,3	01,02, 03	8	12.0	V
V _{DD} / V _{SS} under-voltage lockout threshold Hystersis	V _{THUVs}	<u>2/</u>	1,2,3	02,03	250	2000	mV
Output high short circuit pulsed current	+I _{OUT}	V _{OUT} = 0 V, PW < 80 μs <u>2/</u>	1,2,3	01	0.6		A
				02,03	0.9		
	-I _{OUT}	V _{OUT} = 15 V, PW < 80 μs <u>2/</u>		01	0.6		
				02,03	0.9		

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 6

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Conditions <u>1/</u> -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low side turn-off propagation delay	TLoff	<u>3/</u>	9,10,11	01		300	ns
				02,03		360	
High side turn-off propagation delay	THoff	<u>3/</u>	9,10,11	01		420	ns
				02,03		360	
Low side turn-on propagation delay	TLon	<u>3/</u>	9,10,11	01		280	ns
				02,03		425	
High side turn-on propagation delay	THon	<u>3/</u>	9,10,11	01		360	ns
				02,03		425	
Low side shutdown propagation delay	TLsd	<u>3/</u>	9,10,11	01		270	ns
				02,03		400	
High side shutdown propagation delay	THsd	<u>3/</u>	9,10,11	01		380	ns
				02,03		400	
Either output rise/fall time	Tr, Tf	<u>3/</u>	9,10,11	01		60	ns
				02,03		40	
Dead time LO turn-off to HO turn-on	DHton	<u>3/ 4/</u>	9,10,11	01	-50		ns
				02,03	-20	75	
Dead time HO turn-off to LO turn-on	DLton	<u>3/ 4/</u>	9,10,11	01	-200		ns
				02,03	10	100	
Turn-on propagation delay matching	Mton	<u>3/ 5/</u>	9,10,11	01	-100	0	ns
				02,03	-20	60	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 7

TABLE IA. Electrical performance characteristics – Continued.

Test	Symbol	Test conditions ^{1/} -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A subgroup	Device type	Limits ^{2/}		Unit
					Min	Max	
Turn-off propagation delay matching	Mtoff	^{3/} ^{5/}	9,10,11	01	-150	0	ns
				02,03	-20	60	

^{1/} RHA device types 01 and 02 supplied to this drawing meet all levels M, D, P, L, R and F of irradiation for device classes M, Q, or V and levels M, D, P, L, and R for device class T. However, device types 01 and 02 for device classes M, Q, and V are only tested at the “F” level, and device type 01 for device class T is only tested at the “R” level) in accordance with MIL-STD-883 method 1019 condition A (see 1.5 herein). Device types 01 and 02 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects.

RHA device type 03 supplied to this drawing will meet all levels M, D, P, L, R, and F of irradiation for condition A and levels M, D, P, and L for condition D. However, device type 03 is only tested at the “F” level in accordance with MIL-STD-883, method 1019, condition A and tested at the “L” level in accordance with MIL-STD-883, method 1019, condition D (see 1.5 herein).

Pre and post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electricals measurements for any RHA level, T_A = +25°C.

^{2/} Unless otherwise specified, V_{BIAS} (V_{CC}, V_B, V_{DD}) = 15 V and V_{SS} = V_S = COM = 0 V. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic inputs. The V_O and I_O parameters are referenced to COM for low output (LO) and V_S for high output (HO).

^{3/} Unless otherwise specified, V_{BIAS} (V_{CC}, V_B, V_{DD}) = 15 V, V_{SS} = V_S = COM = 0 V, and C_L = 1000 pF. See figure 3.

^{4/} For device type 01: DHT_{on} = (TH_{on} - TL_{off} - TL_f) and DL_{ton} = (TL_{on} - TH_{off} - TH_f).
For device type 02: DHT_{on} = (TH_{on} - TL_{off}) and DL_{ton} = (TL_{on} - TH_{off}).

^{5/} M_{ton} = (TL_{on} - TH_{on}) and M_{toff} = (TL_{off} - TH_{off}).

TABLE IB. SEP test limits. ^{1/}

Device types	SEP/SEE	Temperature (T _C)	V _{DD}	Linear energy transfer (LET) [MeV/(mg/cm ²)]	Fluence / cross section
02, 03	No SEL	+125°C	20 V	Effective LET ≤ 90	
	No SEB	+25°C	20 V	Effective LET ≤ 90	Fluence = 1 x 10 ⁷ ions/cm ²
	SET	+25°C	20 V	Effective LET = 90	^{2/}

^{1/} For single event phenomena (SEP) test conditions, see 4.4.4.3 herein.

^{2/} Fluence = 4 x 10⁶ ions/cm², at V_{DD} = 20 V and cross section 2.56 x 10⁻⁴ mg/cm².

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 8

Device types	01, 02, 03	
Case outline	X	
Terminal number	Terminal symbol	Description
1	LO	Low side gate drive output.
2	COM	Low side return.
3	VCC	Low side supply.
4	NC	No connection.
5	NC	No connection.
6	VS	High side floating supply return.
7	VB	High side floating supply.
8	HO	High side gate drive output.
9	NC	No connection.
10	NC	No connection.
11	VDD	Logic supply.
12	HIN	Logic input for high side gate driver output (HO), in phase.
13	SD	Logic input for shutdown.
14	LIN	Logic input for low side gate driver output (LO), in phase.
15	VSS	Logic ground.
16	NC	No connection.

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 9

Device type 01

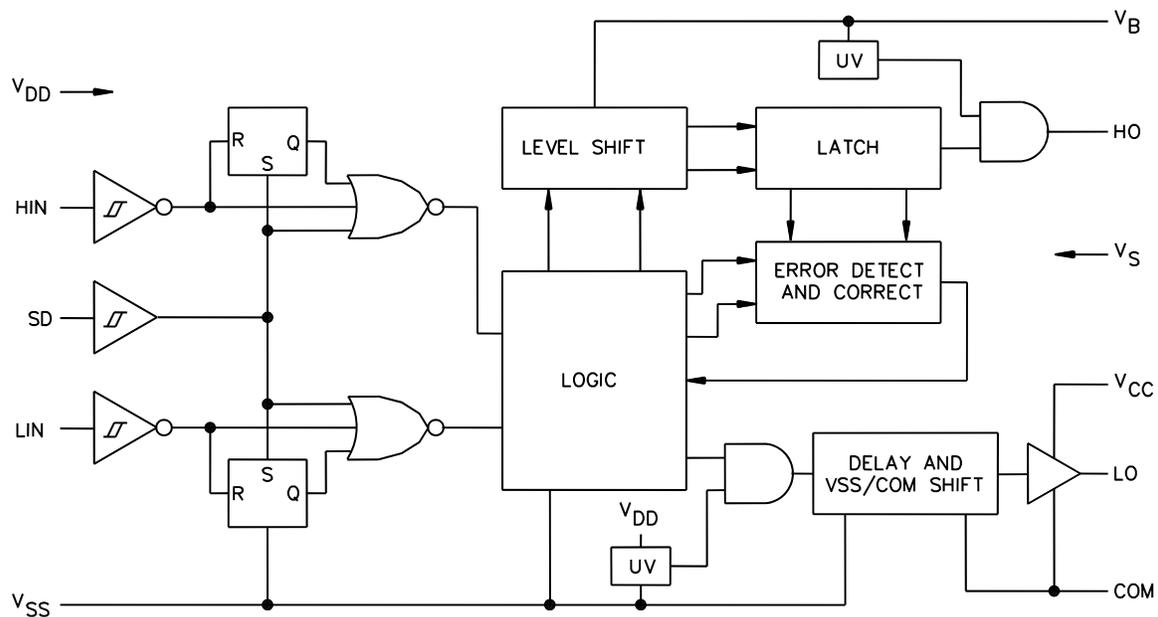


FIGURE 2. Logic diagram.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-99536

REVISION LEVEL
J

SHEET
10

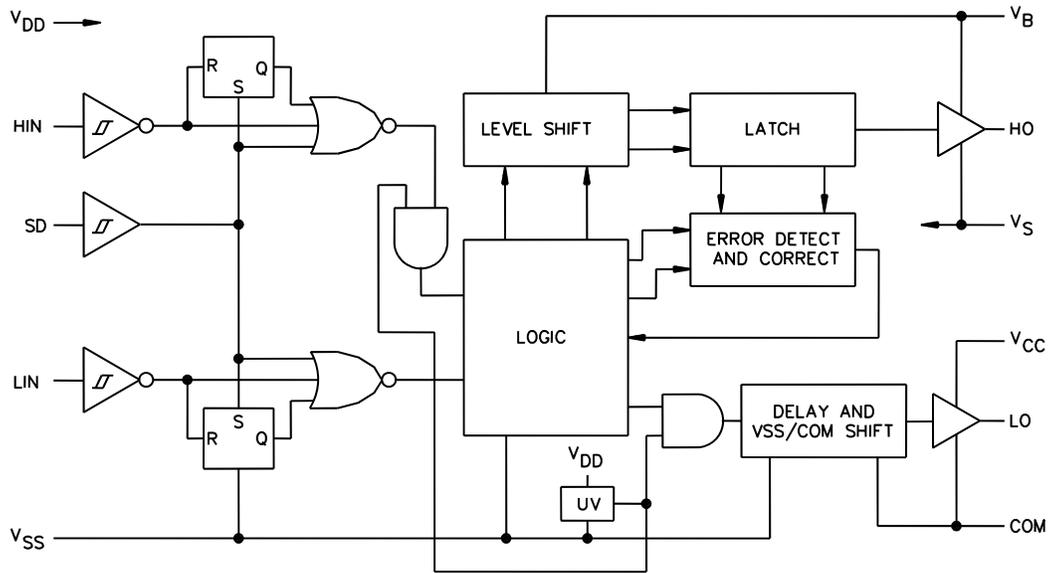


FIGURE 2. Logic diagram - continued.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

5962-99536

REVISION LEVEL
J

SHEET
11

Device types 01, 02 and 03

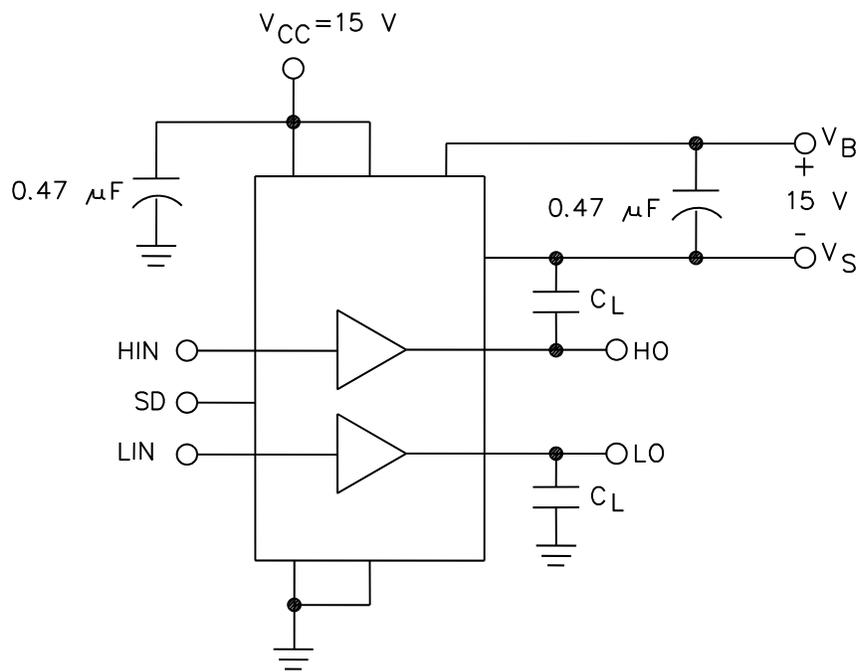


FIGURE 3. Switching time test circuit.

**STANDARD
MICROCIRCUIT DRAWING**
DLA LAND AND MARITIME
COLUMBUS, OHIO 43218-3990

SIZE
A

REVISION LEVEL
J

5962-99536

SHEET
12

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q, T and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q, T and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q, T and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q, T and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q, T and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan, including screening (4.2), qualification (4.3), and conformance inspection (4.4). The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class T, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 and the device manufacturer's QM plan including screening, qualification, and conformance inspection. The performance envelope and reliability information shall be as specified in the manufacturer's QM plan.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class T, screening shall be in accordance with the device manufacturer's Quality Management (QM) plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q, T and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. For device classes Q, T and V interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, Appendix B.

4.3 Qualification inspection for device classes Q, T and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Qualification inspection for device class T shall be in accordance with the device manufacturer's Quality Management (QM) plan. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 13

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class Q	Device class V	Device class T
Interim electrical parameters (see 4.2)	1,9	1,9	As specified in QM plan
Final electrical parameters (see 4.2)	1,2,3,9, <u>1/</u> 10,11	1,2,3,9, <u>2/ 3/</u> 10,11	As specified in QM plan
Group A test requirements (see 4.4)	1,2,3,9,10,11	1,2,3,9,10,11	As specified in QM plan
Group C end-point electrical parameters (see 4.4)	1,2,3,9,10,11	1,2,3,9, <u>3/</u> 10,11	As specified in QM plan
Group D end-point electrical parameters (see 4.4)	1,9	1,9	As specified in QM plan
Group E end-point electrical parameters (see 4.4)	1,9	1,9	As specified in QM plan

1/ PDA applies to subgroups 1.

2/ PDA applies to subgroups 1, 9, and Δ's.

3/ Delta limits as specified in table IIB herein shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters (see table I).

TABLE IIB. Burn-in and operating life test delta parameters. TA = +25°C.

Parameters <u>1/</u>	Device type 01	Device types 02 and 03
	Delta limits	
ILK	±5 μA	±150 μA
IQDD	±100 μA	±100 μA

1/ These parameters shall be recorded before and after the required burn-in and life test to determine delta limits.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 14

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein. Technology conformance inspection for class T shall be in accordance with the device manufacturer's Quality Management (QM) plan.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 4, 5, 6, 7, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q, T and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Group E inspection for device class T. For device class T, the RHA requirements shall be in accordance with the class T radiation requirements of MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.2 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein for device types 01, 02, and 03. In addition, for device type 03 a low dose rate test shall be performed in accordance with MIL-STD-883 method 1019, condition D and as specified herein.

4.4.4.3 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The recommended test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or $\geq 10^7$ ions/cm².
- c. The flux shall be between 10^2 and 10^5 ions/cm²/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 micron in silicon.
- e. The test temperature shall be $+125^\circ\text{C} \pm 10\%$ for SEL and $+25^\circ\text{C} \pm 10\%$ for SEB and SET.
- f. Bias conditions for VDD shall be as listed in Table IB for the latchup measurements.
- g. For SEL test limits, see Table IB herein.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 15

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q, T and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, T and V. Sources of supply for device classes Q, T and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When applicable, a copy of the following additional data shall be maintained and available from the device manufacturer:

- a. RHA upset levels.
- b. Test conditions (SEP).
- c. Number of latchups (SEL).
- d. Number of burnouts (SEB).
- d. Number of transients (SET).

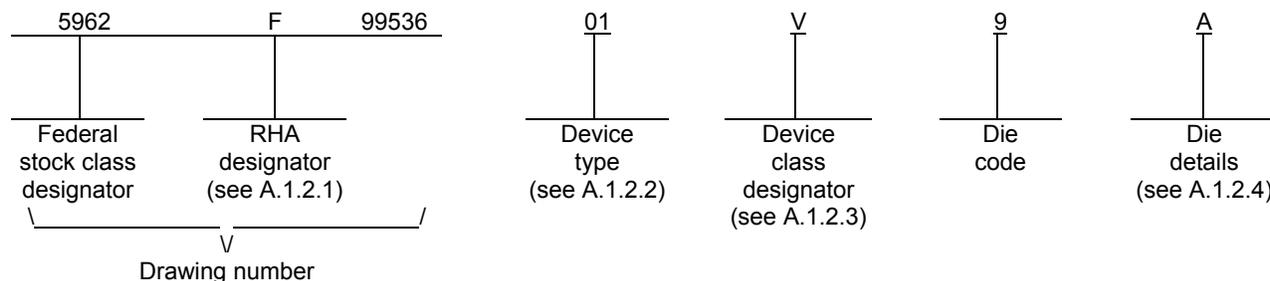
STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 16

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99536

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	HS-2100RH	120 V, radiation hardened, dielectric isolated high frequency half bridge driver
02	IS-2100ARH	150 V, radiation hardened, dielectric isolated high frequency half bridge driver
03	IS-2100AEH	150 V, radiation hardened, dielectric isolated high frequency half bridge driver

A.1.2.3 Device class designator.

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 17

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99536

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02, 03	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02, 03	A-2

A.1.2.4.3 Interface materials.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02, 03	A-2

A.1.2.4.4 Assembly related information.

<u>Die type</u>	<u>Figure number</u>
01	A-1
02, 03	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.1.5 Radiation features. See paragraph 1.5 herein for details.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A	5962-99536
	REVISION LEVEL J	SHEET 18

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99536

A.2 APPLICABLE DOCUMENTS.

A.2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.4 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 19

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99536

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

- a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.
- b. 100% wafer probe (see paragraph A.3.4 herein).
- c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4, 4.4.4.1, 4.4.4.2, and 4.4.4.3 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

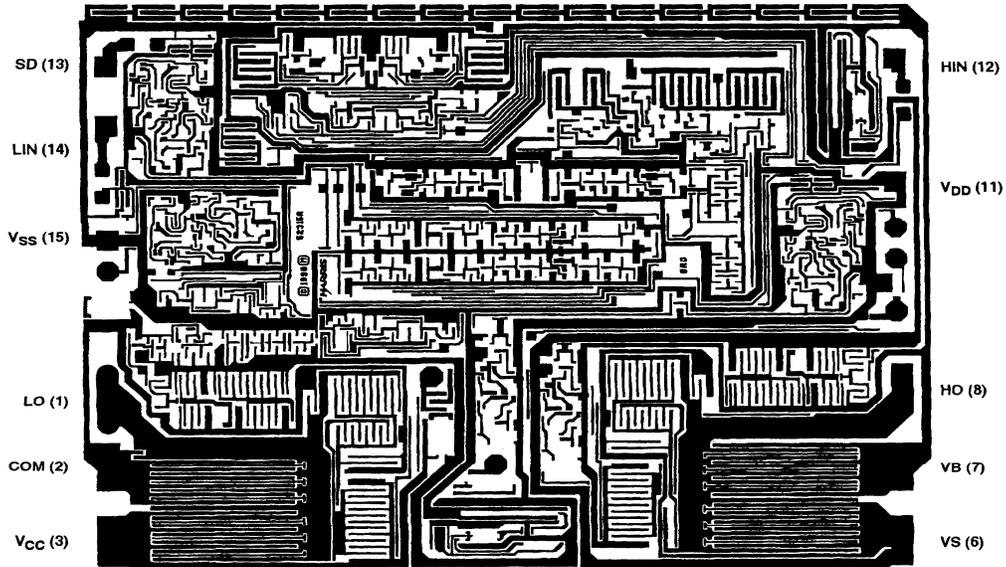
A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, Columbus, Ohio, 43218-3990 or telephone (614)-692-0540.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within MIL-HDBK-103 and QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 20

APPENDIX A
APPENDIX A FORMS A PART OF SMD 5962-99536



Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 4710 microns x 3570 microns
Die thickness: 19 mils \pm 1 mils

Interface materials.

Top metallization: Al Si Cu 16.0 kÅ \pm 2 kÅ
Backside metallization: None

Glassivation.

Type: PSG
Thickness: 8.0 kÅ \pm 1.0 kÅ

Substrate: Dielectric Isolation (DI)

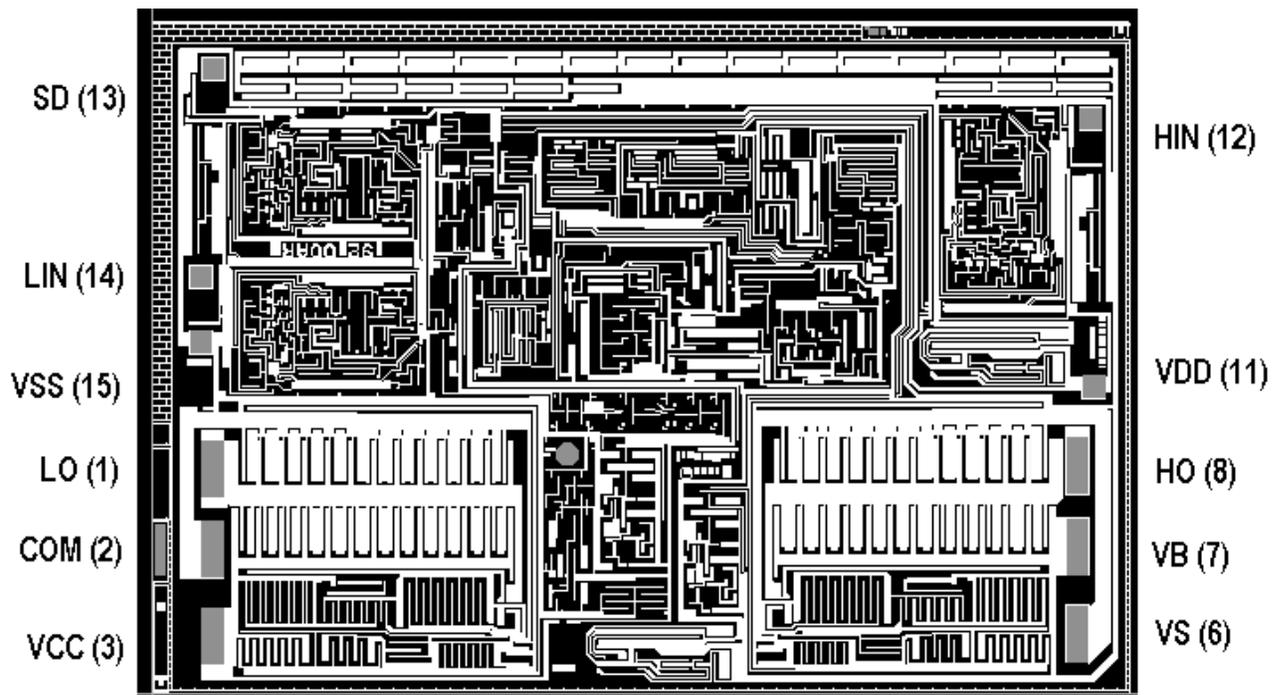
Assembly related information.

Substrate potential: Insulator

FIGURE A-1. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 21

APPENDIX A
 APPENDIX A FORMS A PART OF SMD 5962-99536



Die bonding pad locations and electrical functions

Die physical dimensions.

Die size: 4820 microns x 3300 microns

Die thickness: 19 mils ± 1 mils

Interface materials.

Top metallization: Al Si Cu 16.0 kÅ ±2 kÅ

Backside metallization: None

Glassivation.

Type: PSG

Thickness: 8.0 kÅ ±1.0 kÅ

Substrate: Dielectric Isolation (DI)

Assembly related information.

Substrate potential: Insulator

Special assembly instructions: None

FIGURE A-2. Die bonding pad locations and electrical functions.

STANDARD MICROCIRCUIT DRAWING DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE A		5962-99536
		REVISION LEVEL J	SHEET 22

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-10-05

Approved sources of supply for SMD 5962-99536 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/Programs/Smcr/>.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962F9953601QXC	<u>3/</u>	HS9-2100RH-8
5962R9953601TXC	<u>3/</u>	HS9-2100RH-T
5962F9953601VXC	<u>3/</u>	HS9-2100RH-Q
5962F9953601V9A	<u>3/</u>	HS0-2100RH-Q
5962F9953602QXC	34371	IS9-2100ARH-8
5962F9953602VXC	34371	IS9-2100ARH-Q
5962F9953602V9A	34371	IS0-2100ARH-Q
5962F9953603VXC	34371	IS9-2100AEH-Q
5962F9953603V9A	34371	IS0-2100AEH-Q

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE
number

34371

Vendor name
and address

Intersil Corporation
1650 Robert J. Conlan Blvd. NE
Palm Bay, FL 32905-3406

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.