

**REVISIONS**

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Modify the lead finish in section 1.2. Add new generic number in section 1.2.2. Add table IIB. Update boilerplate to current MIL-PRF-38535 requirements. - PHN	15-01-26	Thomas M. Hess
B	Modified the lead finish for device class Q. Update radiation features in section 1.5 and SEP table IB.- PHN.	15-02-11	Thomas M. Hess
C	Add device type 04 – 06. Add test conditions in Table IA. - PHN	16-10-17	Thomas M. Hess



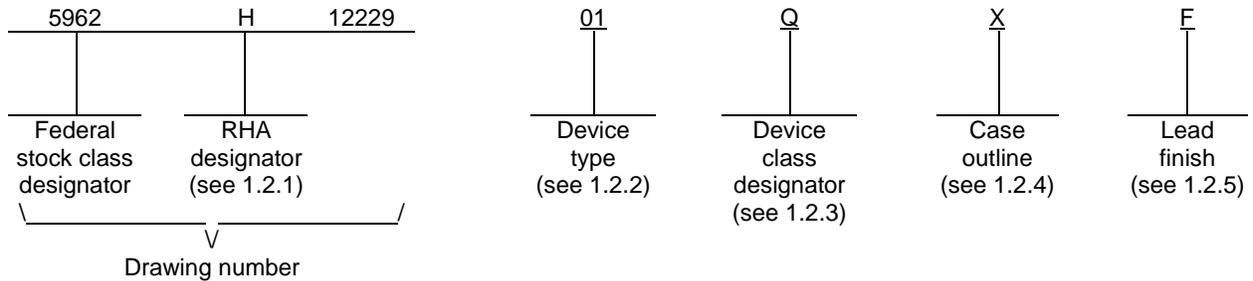
REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C								
SHEET	15	16	17	18	19	20	21	22	23	24	25	26								
REV STATUS OF SHEETS	REV			C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14			

PMIC N/A	PREPARED BY Phu H. Nguyen		<p align="center"><b>DLA LAND AND MARITIME</b>  <b>COLUMBUS, OHIO 43218-3990</b>  <a href="http://www.landandmaritime.dla.mil">http://www.landandmaritime.dla.mil</a></p>																	
<p align="center"><b>STANDARD MICROCIRCUIT DRAWING</b></p> <p>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE</p> <p align="center">AMSC N/A</p>	CHECKED BY Phu H. Nguyen																			
	APPROVED BY Thomas M. Hess		<p align="center">MICROCIRCUIT, DIGITAL, CMOS,  MICROPROCESSOR WITH DECOUPLING CAPACITORS, MONOLITHIC SILICON</p>																	
	DRAWING APPROVAL DATE 12-07-16																			
	REVISION LEVEL <b>C</b>		SIZE A	CAGE CODE <b>67268</b>	<b>5962-12229</b>															
		SHEET		1 OF 26																

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	8447257-1241, -1244	192 MHz microprocessor
02	8447257-1231, -1234	200 MHz microprocessor
03	8447257-1331, -1334	200 MHz microprocessor
04	8447257-2241, -2244	192 MHz microprocessor
05	8447257-2231, -2234	200 MHz microprocessor
06	8447257-2331, -2334	200 MHz microprocessor

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	See figure 1	255	Ceramic column grid array with thermal epoxy

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V. For column grid array (CGA) packages are supplied to this drawing with terminal lead finish mark "F". 1/

1/ Microcircuits devices for column grid array (CGA) packages are supplied to this drawing with terminal lead finish mark "F" or terminal lead finish "A" are a tin (Sn) and lead (Pb) alloy. The solder column material contains compositions of Sn= 90% and Pb=10%.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-12229</b>
		REVISION LEVEL <b>C</b>	SHEET <b>2</b>

1.3 Absolute maximum ratings. 1/ 2/

Core and PLL supply voltage range ( $V_{DD}$ ) .....	-0.4 V dc to +2.4 V dc
60X Bus supply voltage range ( $OV_{DD}$ ) .....	-0.6 V dc to +4.2 V dc
DC input voltage range ( $V_{IN}$ ) .....	-0.6 V dc to +4.2 V dc
Maximum power dissipation at ( $P_D$ ):	
Device type 01 and 04 .....	5.3 W
Device type 02 and 05 .....	5.0 W
Device type 03 and 06 .....	5.7 W
Storage temperature range ( $T_{STG}$ ) .....	-65°C to +150°C
Lead temperature (soldering, 45 seconds, maximum > +180°C).....	+220°C
Thermal resistance, junction-to-column ( $\theta_{JB}$ ) .....	1.5°C/W 3/

1.4 Recommended operating conditions. 4/ 5/

Core supply voltage range ( $V_{DD}$ ):	
Device types 01, 02, 04 and 05 .....	+1.710 V dc to +1.890 V dc
Device type 03 and 06 .....	+1.805 V dc to +1.995 V dc
60x Bus supply voltage range ( $OV_{DD}$ ).....	+3.0 V dc to +3.6 V dc
Logic low input voltage range ( $V_{IL}$ ).....	GND to 0.8 V dc
System clock input high voltage ( $CV_{IH}$ ).....	2.0 V dc to 3.6 V dc
System clock input low voltage ( $CV_{IL}$ ).....	GND to 0.4 V dc
Minimum high level output voltage ( $V_{OH}$ ) .....	2.4 V dc
Maximum low level output voltage ( $V_{OL}$ ) .....	0.4 V dc
Frequency of operation ( $f_{OP}$ ):	
Device type 01 and 04 .....	192 MHz
Device types 02, 03, 05 and 06.....	200 MHz
Case operating temperature range ( $T_C$ ).....	-55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50-300 rads(Si)/s).....	1 Mrad (Si)
Single event phenomenon (SEP):	
No SEL occurs at effective LET (see 4.4.4.4) .....	≤ 120 MeV-cm <sup>2</sup> /mg
Single event upset error rate(SER) .....	< 1 x 10 <sup>-10</sup> upsets/bit-day
Neutron irradiation .....	1 x 10 <sup>12</sup> neutrons/cm <sup>2</sup>
Prompt dose upset (RPRU) .....	> 1 x 10 <sup>9</sup> rad(Si)/sec
Dose rate survivability (RS) .....	> 1 x 10 <sup>11</sup> rad(Si)/sec

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ Value is theoretical,  $\theta_{JB}$  mounted to an infinite heatsink. This value assumes 5 W maximum power.
- 4/ The limits for the parameters specified herein shall apply over the full specified  $V_{DD}$  range and case temperature range of -55°C to +125°C unless otherwise noted.
- 5/ Power sequencing: Power shall be applied to the device only in the following sequences to prevent damage due to excessive currents.

Power-up sequence: GND,  $OV_{DD}$ ,  $V_{DD}$ , Inputs

Power-down sequence: Inputs,  $V_{DD}$ ,  $OV_{DD}$ , GND

All power sequencing is subject to limits in paragraph 1.3.

The sequencing of  $V_{DD}$ ,  $OV_{DD}$ , and can be modified as long as all requirements of notes X and Y are met.

The loss of the 1.8 V power supply (3.3 V power supply active) coupled with an external event (e.g. SEU hit on a critical I/O circuit) may result in a shorting condition. This combined event cannot exist for more than 10 seconds (cumulative time) without reliability impact. A safety margin is included in this analysis, contact the manufacturer is this limit has been exceeded. If there is no external event, the loss of the 1.8 V power supply alone will not result in any reliability impact.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-12229</b>
		REVISION LEVEL <b>C</b>	SHEET <b>3</b>

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### DEPARTMENT OF DEFENSE SPECIFICATION

- MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.
- MIL-PRF-123 - Capacitors, Fixed, Ceramic dielectric, (Temperature Stable and General Purpose), High Reliability, General Specification for.

### DEPARTMENT OF DEFENSE STANDARDS

- MIL-STD-883 - Test Method Standard Microcircuits.
- MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

### DEPARTMENT OF DEFENSE HANDBOOKS

- MIL-HDBK-103 - List of Standard Microcircuit Drawings.
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at <http://www.quicksearch.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

### ASTM INTERNATIONAL (ASTM)

- ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at <http://www.astm.org> or from ASTM International, P. O. Box C700, 100 Barr Harbor Drive, West Conshohocken, PA 19428-2959).

### IEEE - THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

- IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Copies of these documents are available online at <http://www.ieee.org> or from the IEEE Service Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331.

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
**4**

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figures 4 and 5.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.2.6 Solderability test for CGA packages: Solderability test for case outline X for CGA package has been verified during solder column attachment process qualification in accordance with method 2003 of MIL-STD-883.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 IEEE 1149.1 compliance interface. The boundary-scan interface of the device is a fully compliant implementation of the IEEE 1149.1 standard.

3.9 Internal decoupling capacitors. Discrete capacitor arrays are included under the lid of the package, but external to the die. Ceramic capacitors shall meet approved criteria (design, screening, and testing) in accordance with MIL-PRF-123 or as approved by the qualifying activity. The capacitor arrays are included to improve the capability of the device and are an integral part of the package design.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-12229**

REVISION LEVEL  
**C**

SHEET  
**5**

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device type	Group A Subgroups	Limits		Unit	
					Min	Max		
Input high voltage (all Inputs except SYSCLK)	V <sub>IH</sub>		All	1, 2, 3	2.0	3.6	V	
Input low voltage (all Inputs except SYSCLK)	V <sub>IL</sub>		All	1, 2, 3	0.0	0.8		
SYSCLK input high voltage	CV <sub>IH</sub>		All	1, 2, 3	2.0	3.6	V	
SYSCLK input low voltage	CV <sub>IL</sub>		All	1, 2, 3	0.0	0.4		
SCAN I <sub>DDQ</sub> low voltage	SCAN I <sub>DDQ</sub> LOV	T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.62 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	01, 02, 03	1	-	250	mA	
		T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.71 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1	-	350	mA	
		T <sub>C</sub> = -55°C V <sub>DD</sub> core = 1.71 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1	-	350	mA	
		T <sub>C</sub> = +125°C V <sub>DD</sub> core = 1.71 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1	-	450	mA	
		T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.805 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1	-	430	mA	
		T <sub>C</sub> = -55°C V <sub>DD</sub> core = 1.805 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1	-	430	mA	

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
**6**

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
SCAN I <sub>DDQ</sub> low voltage	SCAN I <sub>DDQ</sub> LOV	T <sub>C</sub> = +125°C V <sub>DD</sub> core = 1.805 V, V <sub>DD</sub> I/O = 3.0 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1	-	530	mA
		-			530		
SCAN I <sub>DDQ</sub> nominal voltage	SCAN I <sub>DDQ</sub> NOM	T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.8 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	01, 02, 03	1	-	350	mA
		-			350		
		T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.8 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1	-	420	mA
		-			420		
		T <sub>C</sub> = -55°C V <sub>DD</sub> core = 1.8 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1	-	420	mA
		-			420		
		T <sub>C</sub> = +125°C V <sub>DD</sub> core = 1.8 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1	-	520	mA
		-			520		
T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.9 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1	-	500	mA		
-			500				
T <sub>C</sub> = -55°C V <sub>DD</sub> core = 1.9 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1	-	500	mA		
-			500				
T <sub>C</sub> = +125°C V <sub>DD</sub> core = 1.9 V, V <sub>DD</sub> I/O = 3.3 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1	-	600	mA		
-			600				

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
**7**

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
SCAN I <sub>DDQ</sub> high voltage	SCAN I <sub>DDQ</sub> HIV	T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.995 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	01, 02, 03	1	-	500	mA
		T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.89 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H			04, 05	1	
		T <sub>C</sub> = -55°C V <sub>DD</sub> core = 1.89 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	04, 05	1			-
		T <sub>C</sub> = +125°C V <sub>DD</sub> core = 1.89 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H			04, 05	1	-
		T <sub>C</sub> = +25°C V <sub>DD</sub> core = 1.995 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1			-
		T <sub>C</sub> = -55°C V <sub>DD</sub> core = 1.995 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H			06	1	-
		T <sub>C</sub> = +125°C V <sub>DD</sub> core = 1.995 V, V <sub>DD</sub> I/O = 3.6 V, 80 ns, 001 LPAT, 004 Stop Addresses and Measurements M, D, P, L, R, F, G, H	06	1			-
Input high leakage current for all inputs except those used to control the test	I <sub>IN HI</sub>	V <sub>DD</sub> core = 1.995V, OV <sub>DD</sub> = 3.6V, V <sub>PIN</sub> = 3.6V M, D, P, L, R, F, G, H	All	1, 2, 3		40	μA
				1		40	

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
**8**

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions <u>1/</u> +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
Input low leakage current for all inputs except those used to control the test	I <sub>IN LO</sub>	V <sub>DD core</sub> = 1.995V, OV <sub>DD</sub> = 3.6V, V <sub>PIN</sub> = 0V M, D, P, L, R, F, G, H	All	1, 2, 3		-800	μA
				1		-800	
Output high voltage	V <sub>OH</sub>	I <sub>OH</sub> = -3 mA	All	1, 2, 3	2.4		V
Output low voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA	All	1, 2, 3		0.4	
Input leakage current <u>2/</u>	I <sub>IN</sub>	V <sub>IN</sub> = VO <sub>DD</sub> V <sub>IN</sub> = 0V, VO <sub>DD</sub> = 3.6V	All	1, 2, 3		40	μA
Input capacitance	C <sub>IN</sub>	<u>18/</u>	All	4		12	pF
Functional tests		See 4.4.1b	All	7, 8			
Power consumption		Full-On Mode	01, 04	1, 2, 3		5.3	W
			02, 05			5.5	
			03, 06			6.2	
		Doze Mode	01, 04			3.0	W
			02, 05			3.0	
			03, 06			3.2	
		Nap Mode	01, 04			830	mW
			02, 05			830	
			03, 06			580	
		Sleep Mode	01, 04		790	mW	
			02, 05		770		
			03, 06		540		

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
**9**

TABLE IA. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions <u>1/</u> +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
Clock AC timing specifications							
Processor frequency		<u>3/</u>	01, 04 02, 03, 05, 06	9, 10, 11	125 125	192 200	MHz
SYSClk (bus) frequency		<u>4/</u>	All	9, 10, 11	25	80	MHz
SYSClk cycle time	1	See figure 4.	All	9, 10, 11	12.5	40	ns
SYSClk rise and fall time	2, 3	See figure 4. <u>5/ 6/</u>	All	9, 10, 11		1.5	ns
SYSClk duty cycle measured at 1.4 V	4	See figure 4. <u>7/</u>	All	9, 10, 11	40.0	60.0	%
SYSClk jitter		<u>6/ 7/</u>	All	9, 10, 11		±150	ps
Device internal PLL relock time		<u>8/</u>	All	9, 10, 11		200	μs
60X Bus Input AC timing specifications (SYSClk = 80 MHz) <u>9/</u>							
Address/data/transfer attribute inputs valid to SYSClk (input setup)	10a	See figure 4. <u>10/ 11/</u>	All	9, 10, 11	4.8		ns
All other inputs valid to SYSClk (input setup)	10b	See figure 4. <u>11/ 12/</u>	All	9, 10, 11	5.6		ns
Mode select inputs valid to HRESET (input setup) (for DRTRY, QACK, and TLBISYNC )	10c	See figure 4. <u>11/ 13/ 14/ 15/</u>	All	9, 10, 11	8.0 x t <sub>SYSClk</sub>		ns
SYSClk to address/data/transfer attribute inputs invalid (input hold)	11a	See figure 4. <u>10/ 11/</u>	All	9, 10, 11	1.0		ns
SYSClk to all other inputs invalid (input hold)	11b	See figure 4. <u>11/ 12/</u>	All	9, 10, 11	0.3		ns
HRESET to mode select inputs invalid (input hold) (for DRTRY, QACK, and TLBISYNC )	11c	See figure 4. <u>11/ 13/ 15/</u>	All	9, 10, 11	0.0		ns

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
**10**

TABLE IA. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions <sup>1/</sup> +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device Type	Group A Subgroups	Limits		Unit
					Min	Max	
60X bus Output AC timing specifications (SYSCLK = 80 MHz) <sup>16/ 17/</sup>							
SYSCLK to output driven (output enable time)	12	<u>18/</u>	All	9, 10, 11	1.5		ns
SYSCLK to output valid (5.5 V to 0.8 V - <u>TS</u> , <u>ABB</u> , <u>ARTRY</u> , <u>DBB</u> )	13	<u>19/</u>	All	9, 10, 11		8.0	ns
SYSCLK to output valid (5.5 V to 0.8 V - all except <u>TS</u> , <u>ABB</u> , <u>ARTRY</u> , <u>DBB</u> )	14	<u>18/</u>	All	9, 10, 11		8.4	ns
SYSCLK to output invalid (output hold)	15	<u>18/ 20/</u>	All	9, 10, 11	1.5		ns
SYSCLK to output high impedance (all except <u>ARTRY</u> , <u>ABB</u> , <u>DBB</u> )	16	<u>18/</u>	All	9, 10, 11		8.4	ns
SYSCLK to <u>ABB</u> , <u>DBB</u> high impedance after precharge	17	<u>18/ 21/ 22/</u>	All	9, 10, 11		1.0 x t <sub>SYSCLK</sub>	ns
SYSCLK to <u>ARTRY</u> high impedance before precharge	18	<u>18/</u>	All	9, 10, 11		7.7	ns
SYSCLK to <u>ARTRY</u> precharge enable	19	<u>18/ 21/ 23/ 24/</u>	All	9, 10, 11	2.3		ns
Maximum delay to <u>ARTRY</u> precharge	20	<u>18/ 21/ 24/</u>	All	9, 10, 11		1.0 x t <sub>SYSCLK</sub>	ns
SYSCLK to <u>ARTRY</u> high impedance after precharge	21	<u>18/ 21/ 24/</u>	All	9, 10, 11		2.0 x t <sub>SYSCLK</sub>	ns

See footnotes at end of table.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
11

TABLE IA. Electrical performance characteristics - Continued.

Test	Test no.	Test conditions <sup>1/</sup> +1.62 V ≤ V <sub>DD</sub> ≤ +1.995 V, +3.0 V ≤ OV <sub>DD</sub> ≤ +3.6 V, -55°C ≤ T <sub>C</sub> ≤ +125°C, unless otherwise specified	Device type	Group A Subgroups	Limits		Unit
					Min	Max	
JTAG AC timing specifications (independent of SYSCLK)							
TCK frequency of operation		<u>25/</u>	All	9, 10, 11	0.0	12.5	MHz
TCK cycle time	1	See figure 5. <u>25/</u>	All	9, 10, 11	80	-	ns
TCK clock pulse width measured at 1.4 V	2	See figure 5. <u>18/</u>	All	9, 10, 11	15	-	ns
TCK rise and fall times	3	See figure 5. <u>18/</u>	All	9, 10, 11	0	1.5	ns
$\overline{\text{TRST}}$ assert time	5	See figure 5. <u>26/</u>	All	9, 10, 11	80	-	ns
Boundary scan input data setup time	6	See figure 5. <u>18/ 27/</u>	All	9, 10, 11	0	-	ns
Boundary scan input data hold time	7	See figure 5. <u>18/ 27/</u>	All	9, 10, 11	25	-	ns
TCK to output data valid	8	See figure 5. <u>18/ 28/</u>	All	9, 10, 11	4	25	ns
TCK to output high impedance	9	See figure 5. <u>18/ 28/</u>	All	9, 10, 11	4	25	ns
TMS, TDI data setup time	10	See figure 5. <u>18/</u>	All	9, 10, 11	0	-	ns
TMS, TDI data hold time	11	See figure 5. <u>18/</u>	All	9, 10, 11	15	-	ns
TCK to TDO data valid	12	See figure 5.	All	9, 10, 11	10	20	ns
TCK to TDO high impedance	13	See figure 5. <u>18/</u>	All	9, 10, 11	10	20	ns

<sup>1/</sup> RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F, G and H of irradiation. However, this device is only tested at the "H" level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T<sub>A</sub> = +25°C.

<sup>2/</sup> Excludes test signals (LSSD\_MODE, L1\_TSTCLK, L2\_TSTCLK, and JTAG signals).

<sup>3/</sup> Under certain conditions, operation at core frequencies below those stated is possible.

<sup>4/</sup> Caution: The SYSCLK frequency and PLL\_CFG0-PLL\_CFG3 settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies.

<sup>5/</sup> Rise and fall times for the SYSCLK input are measured from 0.4 V to 2.4 V.

<sup>6/</sup> Timing is guaranteed by design and characterization, and is not tested.

<sup>7/</sup> The total input jitter (short term and long term combined) must be under +150 ps.

**STANDARD  
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
12

TABLE IA. Electrical performance characteristics - Continued.

- 8/ Relock timing is guaranteed by design and characterization, and is not tested. PLL-relock time is the maximum amount of time required for PLL lock after a stable VDD and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRESET must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.
- 9/ Input specifications are measured from the midpoint voltage (Vm) of the signal in question to Vm of the rising edge of the input SYSCLK. Both input and output timings are measured at the pin.
- 10/ Address/data/transfer attribute input signals are composed of the following: A0-A31, AP0-AP3, TT0-TT4,  $\overline{\text{TBST}}$ , TSIZ0-TSIZ2,  $\overline{\text{GBL}}$ , DH0-DH31, DL0-DL31, DP0-DP7.
- 11/ These values are guaranteed by design, and are not tested.
- 12/ All other input signals are composed of the following:  $\overline{\text{TS}}$ ,  $\overline{\text{ABB}}$ ,  $\overline{\text{DBB}}$ ,  $\overline{\text{ARTRY}}$ ,  $\overline{\text{BG}}$ ,  $\overline{\text{AACK}}$ ,  $\overline{\text{DBG}}$ ,  $\overline{\text{DBWO}}$ ,  $\overline{\text{TA}}$ ,  $\overline{\text{DRTRY}}$ ,  $\overline{\text{TEA}}$ ,  $\overline{\text{DBDIS}}$ ,  $\overline{\text{HRESET}}$ ,  $\overline{\text{SRESET}}$ ,  $\overline{\text{INT}}$ ,  $\overline{\text{SMI}}$ ,  $\overline{\text{MCP}}$ ,  $\overline{\text{TBEN}}$ ,  $\overline{\text{QACK}}$ ,  $\overline{\text{TLBISYNC}}$ .
- 13/ The setup and hold time is with respect to the rising edge of  $\overline{\text{HRESET}}$ .
- 14/ tSYSCLK is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
- 15/ This specification is for configuration mode select only. Also note that the  $\overline{\text{HRESET}}$  must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
- 16/ All output specifications are measured from the midpoint voltage (Vm) of the rising edge of SYSCLK to Vm of the signal in question. Both input and output timings are measured at the pin.
- 17/ All maximum timing specifications assume  $C_L = 75 \text{ pF}$ .
- 18/ Guaranteed by design, and not tested
- 19/ Output signal transitions from GND to 2.0 V or VDD to 0.8 V.
- 20/ Connecting L2\_TSTCLK to GND does not provide additional Output Hold. L2\_TSTCLK should be pulled up to OVDD.
- 21/ tsys is the period of the external bus clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
- 22/ Nominal precharge width for  $\overline{\text{ABB}}$  and  $\overline{\text{DBB}}$  is  $0.5 t_{\text{sysclk}}$ .
- 23/ This minimum timing parameter assumes  $C_L = 75 \text{ pF}$ .
- 24/ Nominal precharge width for  $\overline{\text{ARTRY}}$  is  $1.0 t_{\text{sysclk}}$ .
- 25/ Testing is done at 33 MHz (30 ns).
- 26/  $\overline{\text{TRST}}$  is an asynchronous signal. The setup time is for test purposes only.
- 27/ Non-test signal input timing with respect to TCK.
- 28/ Non-test signal output timing with respect to TCK.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>	<b>5962-12229</b>
	REVISION LEVEL <b>C</b>	SHEET 13

TABLE IB. SEP test limits. 1/ 2/

Device types	V <sub>DD</sub> = 1.62 V		Bias V <sub>DD</sub> = 1.995 V for SEL test No SEL at effective LET 3/ 4/
	SER Adam 90% environment	Maximum device cross section	
All	1 x 10 <sup>-10</sup> upsets/bit-day 5/	2 x 10 <sup>-8</sup> cm <sup>2</sup> /bit	LET ≤ 120 MeV-cm <sup>2</sup> /mg

- 1/ For SEP test conditions, see 4.4.4.4 herein.
- 2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
- 3/ Tested to case temperature T<sub>A</sub> = +125°C ±10°C
- 4/ Tested to an LET of ≥ 120 MeV/(mg/cm<sup>2</sup>), with no latch-up (SEL).
- 5/ CRÈME 96 using 1024x1024 FFT test algorithm and resulting Weibull parameter fit to the data.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

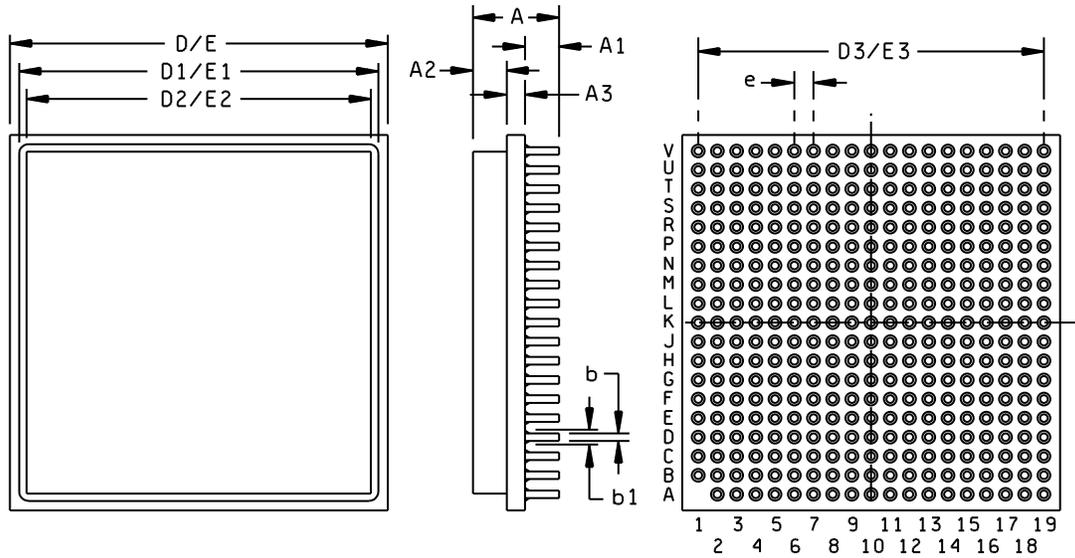
SIZE  
**A**

**5962-12229**

REVISION LEVEL  
**C**

SHEET  
14

Case X



Case	X			
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	---	6.2	---	0.244
A1	2.03	2.39	0.080	0.094
A2	2.04	2.40	0.080	0.094
A3	1.02	1.38	0.040	0.054
b	0.454	0.606	0.018	0.024
b1	0.81	0.91	0.032	0.036
D/E	24.8	25.2	0.976	0.992
D1/E1	22.37	22.63	0.881	0.891
D2/E2	20.37	20.63	0.802	0.812
D3/E3	22.58	23.14	0.889	0.911
e	1.27 NOM		0.050 NOM	

Note: Dimensions are in millimeters. Inches equivalents are for general information only.

FIGURE 1. Case outline.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-12229**

REVISION LEVEL  
**C**

SHEET  
**15**

## Case X

Column Name	Signal Name						
A13	A00	L07	ABB	V06	DH16	V10	DL17
D02	A01	C04	AP0	U08	DH17	W08	DL18
H11	A02	C05	AP1	V09	DH18	T11	DL19
C01	A03	C06	AP2	T07	DH19	U11	DL20
B13	A04	C07	AP3	U07	DH20	V12	DL21
F02	A05	L06	ARTRY	R07	DH21	V08	DL22
C13	A06	A08	AVDD	U06	DH22	T01	DL23
E05	A07	H01	BG	W05	DH23	P01	DL24
D13	A08	E07	BR	U05	DH24	V01	DL25
G07	A09	D07	CHECKSTOP	W04	DH25	U01	DL26
F12	A10	C02	CI	P07	DH26	N01	DL27
G03	A11	B08	CKSTP	V05	DH27	R02	DL28
G06	A12	E03	CLKOUT	V04	DH28	V03	DL29
H02	A13	K05	DBB	W03	DH29	U03	DL30
E02	A14	G01	DBDIS	U04	DH30	W02	DL31
L03	A15	K01	DBG	R05	DH31	L01	DP0
G05	A16	D01	DBWO	M06	DL00	P02	DP1
L04	A17	W12	DH00	P03	DL01	M02	DP2
G04	A18	W11	DH01	N04	DL02	V02	DP3
J04	A19	V11	DH02	N05	DL03	M01	DP4
H07	A20	T09	DH03	R03	DL04	N02	DP5
E01	A21	W10	DH04	M07	DL05	T03	DP6
G02	A22	U09	DH05	T02	DL06	R01	DP7
F03	A23	U10	DH06	N06	DL07	H06	DRTRY
J07	A24	M11	DH07	U02	DL08	B01	GBL
M03	A25	M09	DH08	N07	DL09	B06	HRESET
H03	A26	P08	DH09	P11	DL10	C11	INT
J02	A27	W07	DH10	V13	DL11	F08	L1TSTCLK
J06	A28	P09	DH11	U12	DL12	L17	L2ADDR00
K03	A29	W09	DH12	P12	DL13	L18	L2ADDR01
K02	A30	R10	DH13	T13	DL14	L19	L2ADDR02
L02	A31	W06	DH14	W13	DL15	M19	L2ADDR03
N03	AACK	V07	DH15	U13	DL16	K18	L2ADDR04

FIGURE 2. Terminal connections.

**STANDARD  
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
16

## Case X

Column Name	Signal Name	Column Name	Signal Name	Column Name	Signal Name	Column Name	Signal Name
K17	L2ADDR05	R19	L2D18	B17	L2D52	W01	NC6
K15	L2ADDR06	R18	L2D19	A18	L2D53	K09	NC7
J19	L2ADDR07	R17	L2D20	A17	L2D54	A04	PLLCFG0
J18	L2ADDR08	R15	L2D21	A16	L2D55	A05	PLLCFG1
J17	L2ADDR09	P19	L2D22	B16	L2D56	A06	PLLCFG2
J16	L2ADDR10	P18	L2D23	C16	L2D57	A07	PLLCFG3
H18	L2ADDR11	P13	L2D24	A14	L2D58	B02	QACK
H17	L2ADDR12	N14	L2D25	A15	L2D59	J03	QREQ
J14	L2ADDR13	N13	L2D26	C15	L2D60	D03	RSRV
J13	L2ADDR14	N19	L2D27	B14	L2D61	A12	SMI
H19	L2ADDR15	N17	L2D28	C14	L2D62	E10	SRESET
G18	L2ADDR16	M17	L2D29	E13	L2D63	H09	SYSCLK
L13	L2AVDD	M13	L2D30	V14	L2DP0	F01	TA
P17	L2CE	M18	L2D31	U16	L2DP1	A02	TBEN
N15	L2CLKOUTA	H13	L2D32	T19	L2DP2	A11	TBST
L16	L2CLKOUTB	G19	L2D33	N18	L2DP3	B10	TCK
U14	L2D00	G16	L2D34	H14	L2DP4	B07	TDI
R13	L2D01	G15	L2D35	F17	L2DP5	D09	TDO
W14	L2D02	G14	L2D36	C19	L2DP6	J01	TEA
W15	L2D03	G13	L2D37	B15	L2DP7	A03	TLBISYNC
V15	L2D04	F19	L2D38	K19	L2EXP1	C08	TMS
U15	L2D05	F18	L2D39	K11	L2EXP2	A10	TRST
W16	L2D06	F13	L2D40	L14	L2SYNCIN	K07	TS
V16	L2D07	E19	L2D41	M14	L2SYNCOU T	A09	TSIZ0
W17	L2D08	E18	L2D42	F07	L2TSTCLK	B09	TSIZ1
V17	L2D09	E17	L2D43	N16	L2WE	C09	TSIZ2
U17	L2D10	E15	L2D44	G17	L2ZZ	C10	TT0
W18	L2D11	D19	L2D45	F09	LSSDMODE	D11	TT1
V18	L2D12	D18	L2D46	B11	MCP	B12	TT2
U18	L2D13	D17	L2D47	B03	NC2	C12	TT3
V19	L2D14	C18	L2D48	B04	NC2	F11	TT4
U19	L2D15	C17	L2D49	B05	NC3	C03	WT
T18	L2D16	B19	L2D50	A19	NC4		
T17	L2D17	B18	L2D51	W19	NC5		

FIGURE 2. Terminal connections - Continued.

**STANDARD  
MICROCIRCUIT DRAWING**

DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-12229**

REVISION LEVEL  
**C**

SHEET  
17

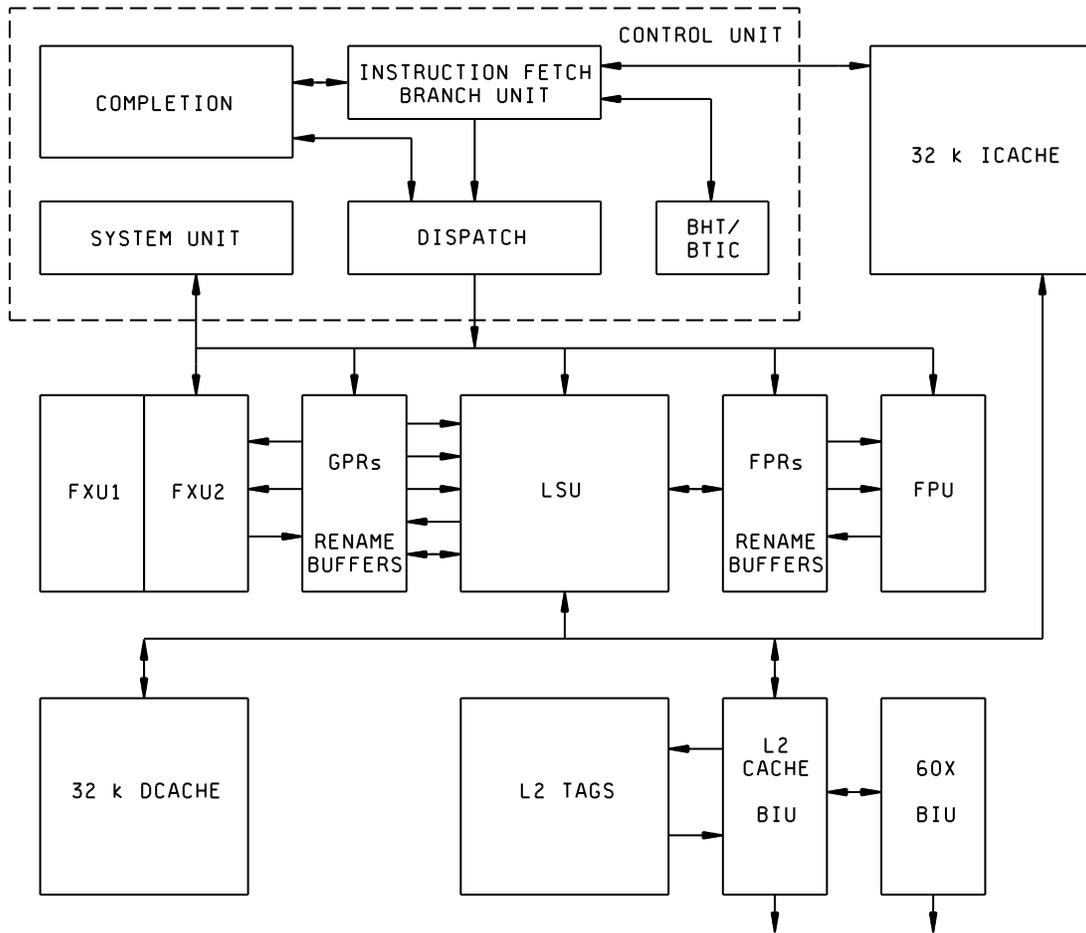


FIGURE 3. Block diagram.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

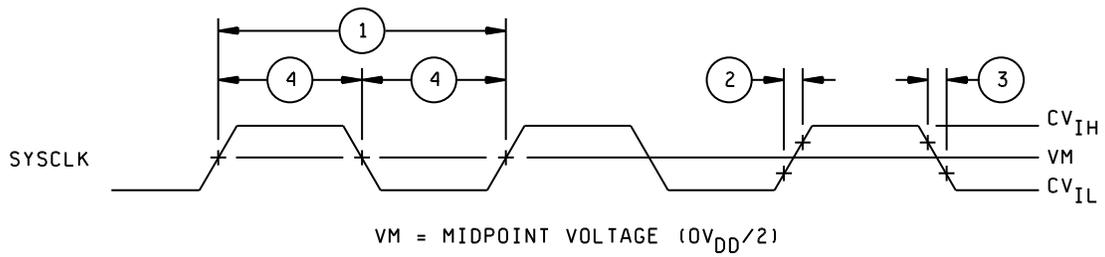
SIZE  
**A**

**5962-12229**

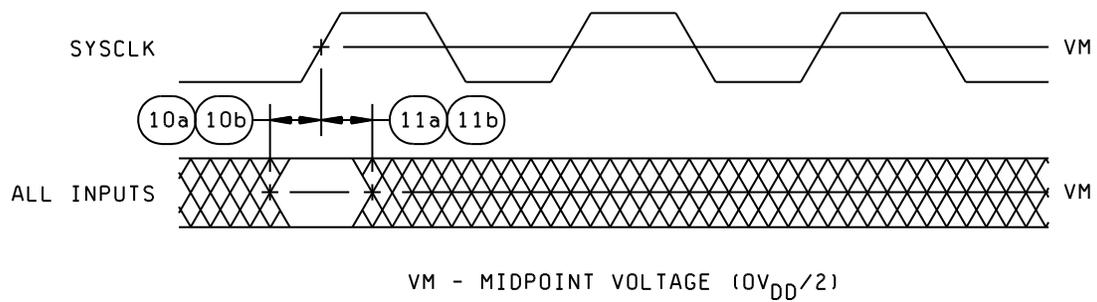
REVISION LEVEL  
**C**

SHEET  
18

SYSCLK Input Timing Diagram



Input Timing Diagram



Mode Select Input Timing Diagram

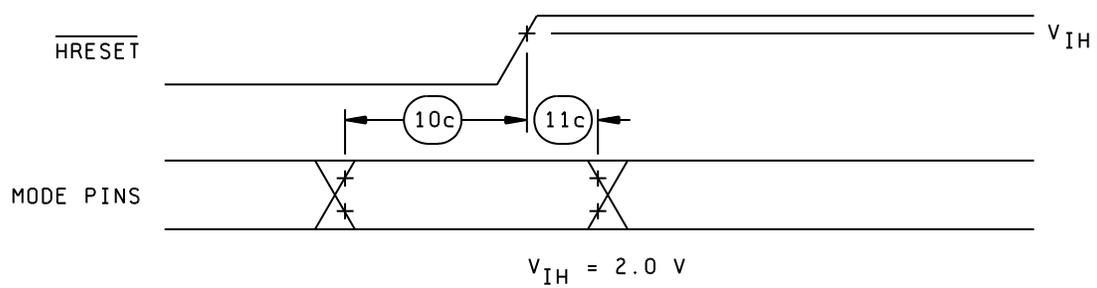


FIGURE 4. Timing waveforms.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
19

Output Timing diagram

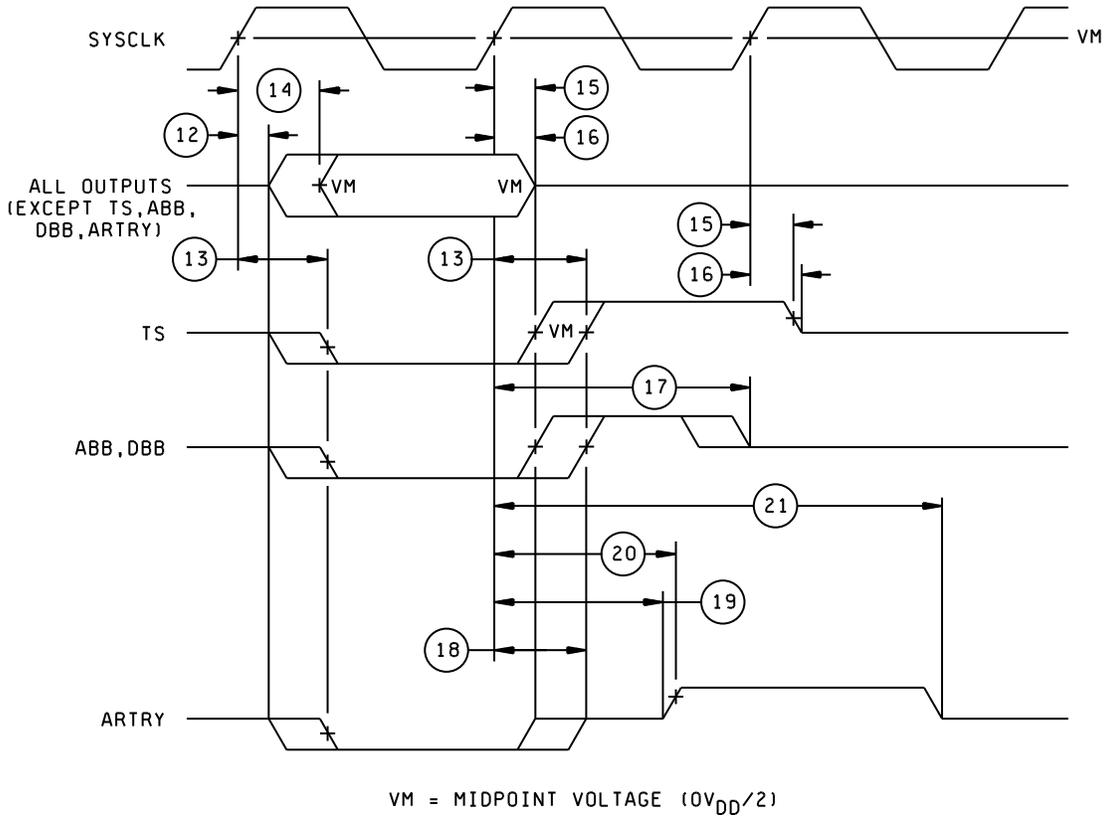


FIGURE 4. Timing waveforms - Continued.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

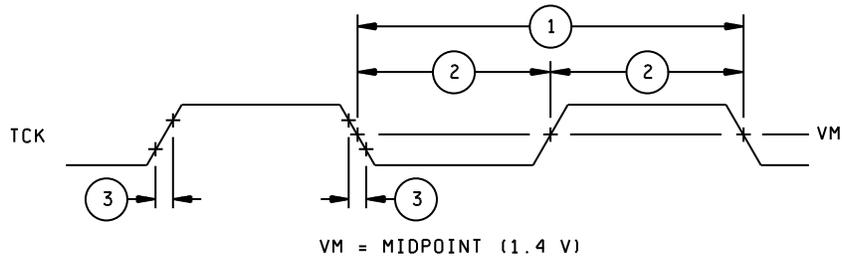
SIZE  
**A**

**5962-12229**

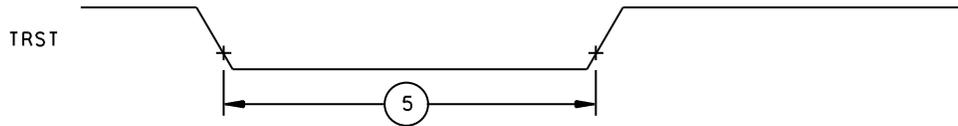
REVISION LEVEL  
**C**

SHEET  
**20**

JTAG Clock Input Timing Diagram



TRST Timing Diagram



Boundary-Scan Timing Diagram

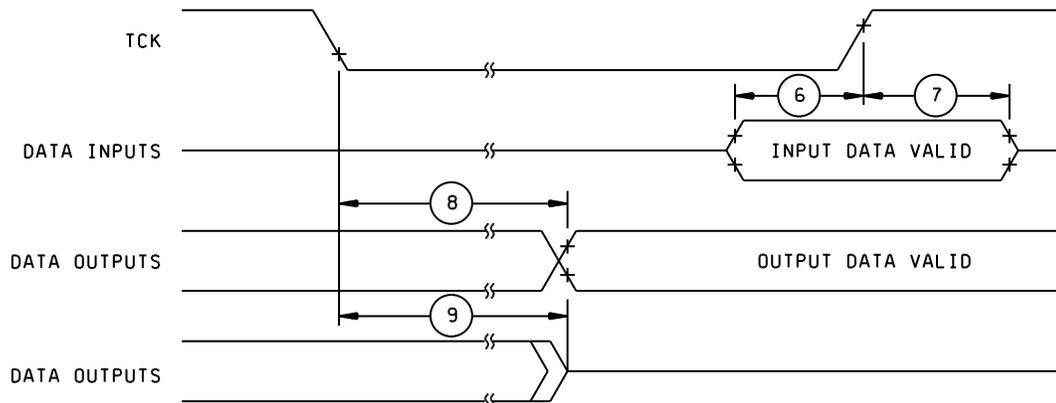


FIGURE 5. JTAG timing waveforms.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-12229**

REVISION LEVEL  
**C**

SHEET  
21

Test Access Port Timing Diagram

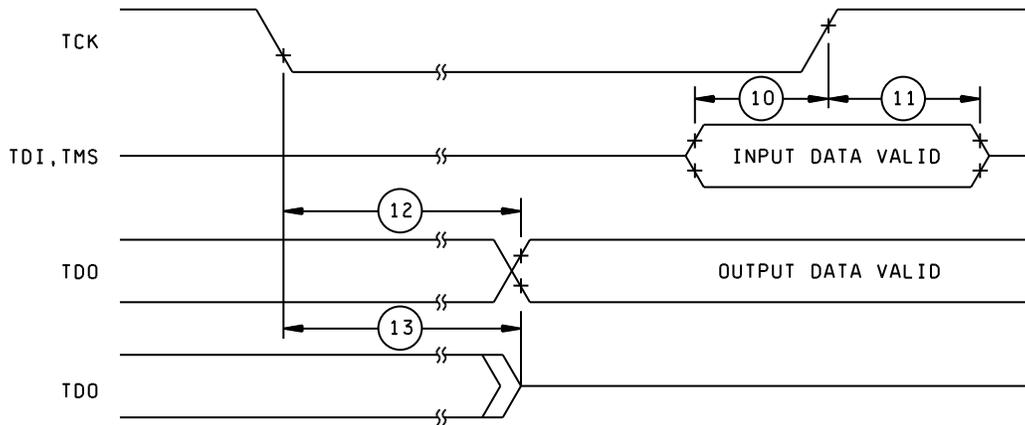


FIGURE 5. JTAG timing waveforms - Continued.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

**5962-12229**

REVISION LEVEL  
**C**

SHEET  
22

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
- d. Additional screening for device types 01 - 06 shall include:
  - (1) 100% X-ray per MIL-STD-883, method 2012
  - (2) Increased burn-in (240 hours) dynamic burn-in
  - (3) Optional interim room temperature electrical test
  - (4) 144 hours static burn-in with tightened class V PDA

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.
- c. Subgroup 4 (C<sub>IN</sub> measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minimum sample size of five devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-12229</b>
		REVISION LEVEL <b>C</b>	SHEET 23

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 <u>1/</u>	1, 2, 3, 7, 8, 9, 10, 11 <u>2/ 3/</u>
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4) <u>4/</u>	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Post-column attach electrical parameters test (see 4.2) <u>5/</u>	1	1

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

3/ Delta limit (see Table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters.

4/ For CGA package, Group D test shall be performed all applicable LGA level test and in addition column destructive pull test and salt atmosphere test method (TM 1009) is required.

5/ For CGA package solderability test shall be performed in accordance with test method 2003.

Table IIB. Delta limits at +25°C.

Parameter <u>1/</u>	Limits	Units
SCAN I <sub>DDQ</sub> NOM	± 10% of specified value in Table IA	mA

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T<sub>A</sub> = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

**STANDARD  
MICROCIRCUIT DRAWING**  
DLA LAND AND MARITIME  
COLUMBUS, OHIO 43218-3990

SIZE  
**A**

REVISION LEVEL  
**C**

**5962-12229**

SHEET  
24

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at +25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. When required by the customer, Neutron testing shall be performed in accordance with method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA, for the subgroups specified in table IIA herein at T<sub>A</sub> = +25°C ±5°C after an exposure of 2 x 10<sup>12</sup> neutrons/cm<sup>2</sup> (minimum).

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

- a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be performed on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latch-up characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° < angle < 60°). No shadowing of the ion beam due to fixturing or package related affects is allowed.
- b. The fluence shall be ≥ 100 errors or ≥ 10<sup>7</sup> ions/cm<sup>2</sup>.
- c. The flux shall be between 10<sup>2</sup> and 10<sup>5</sup> ions/cm<sup>2</sup>/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.
- d. The particle range shall be ≥ 20 microns in silicon.
- e. The upset test temperature shall be +25°C ±10°C and the latch-up test temperature shall be maximum rated operating temperature of +125°C ±10°C.
- f. Bias conditions shall be V<sub>DD</sub> = 1.62 V dc for the upset measurements and V<sub>DD</sub> = 1.995 V dc for the latch-up measurements.
- g. For SEP test limits, see table IB herein.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-12229</b>
		REVISION LEVEL <b>C</b>	SHEET 25

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime -VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime -VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied:

- a. RHA test conditions (SEP):
- b. Number of upsets (SEU).
- c. Number of transients (SET).
- d. Occurrence of latch-up (SEL).

6.8 CGA packages lead finish: Microcircuits devices for column grid array (CGA) packages are supplied to this drawing with terminal lead finish mark "F" or terminal lead finish A for devices listed on this drawing are a tin (Sn) and lead (Pb) alloy. The solder column material contains compositions of Sn= 90% and Pb=10%.

<b>STANDARD MICROCIRCUIT DRAWING</b> DLA LAND AND MARITIME COLUMBUS, OHIO 43218-3990	SIZE <b>A</b>		<b>5962-12229</b>
		REVISION LEVEL <b>C</b>	SHEET <b>26</b>

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 16-10-17

Approved sources of supply for SMD 5962-12229 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at <https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx>

Standard microcircuit drawing PIN <u>1/</u> <u>2/</u>	Vendor CAGE number	Vendor similar PIN <u>3/</u>
5962H1222901QXA	<u>4/</u>	8447257-1244
5962H1222902QXA	<u>4/</u>	8447257-1234
5962H1222903QXA	<u>4/</u>	8447257-1334
5962H1222901VXF	<u>4/</u>	8447257-1241
5962H1222902VXF	<u>4/</u>	8447257-1231
5962H1222903VXF	<u>4/</u>	8447257-1331
5962H1222904QXA	1RU44	8447257-2244
5962H1222905QXA	1RU44	8447257-2234
5962H1222906QXA	1RU44	8447257-2334
5962H1222904VXF	1RU44	8447257-2241
5962H1222905VXF	1RU44	8447257-2231
5962H1222906VXF	1RU44	8447257-2331

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
- 2/ Microcircuits devices for column grid array (CGA) packages are supplied to this drawing with terminal lead finish mark "F" or terminal lead finish "A " for devices listed on this drawing are a tin (Sn) and lead (Pb) alloy. The solder column material contains compositions of Sn= 90% and Pb=10%.
- 3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 4/ Not available from an approved source of supply. Device types 01, 02, and 03 are replaced by device types 04, 05 and 06 respectively.

Vendor CAGE  
number

1RU44

Vendor name  
and address

BAE Systems  
9300 Wellington Road  
Manassas, VA 20110-4122

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.